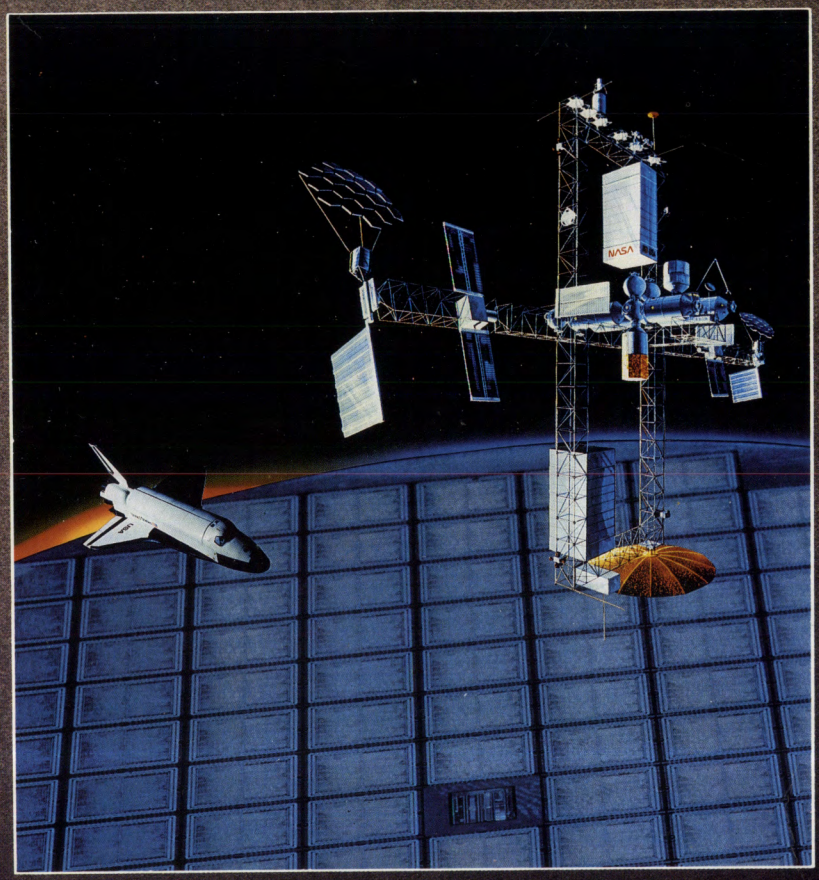

Rad-Hard/Hi-Rel
DATA BOOK
Military & Aerospace Division

HARRIS SEMICONDUCTOR

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Harris Semiconductor
Military & Aerospace Division (M&AD)

Harris Semiconductor has been an industry leader for more than two decades in radiation-hardened circuits which provide high performance and high reliability in severe operating environments. Harris technologies used to achieve radiation hardness include dielectric isolation (DI), Silicon-on-Saphire (SOS), and silicon-on-insulator (SOI). Harris' radiation-hardened products include CMOS CD4000, 54HCT/ACT logic devices, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices which provide the system designer with a full complement of products for radiation-hardened systems.

If you need more information on these and other Harris products please contact the nearest Harris Sales Office or representative.

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RAD-HARD HI-REL

MILITARY AND AEROSPACE APPLICATIONS

RAD-HARD 1

GENERAL INFORMATION

ALPHA NUMERIC PRODUCT INDEX

ALPHA NUMERIC PRODUCT INDEX (Continued)

ALPHA NUMERIC PRODUCT INDEX (Continued)

PRODUCT INDEX BY FAMILY

RAD-HARD 2

RADIATION EFFECTS ON CMOS

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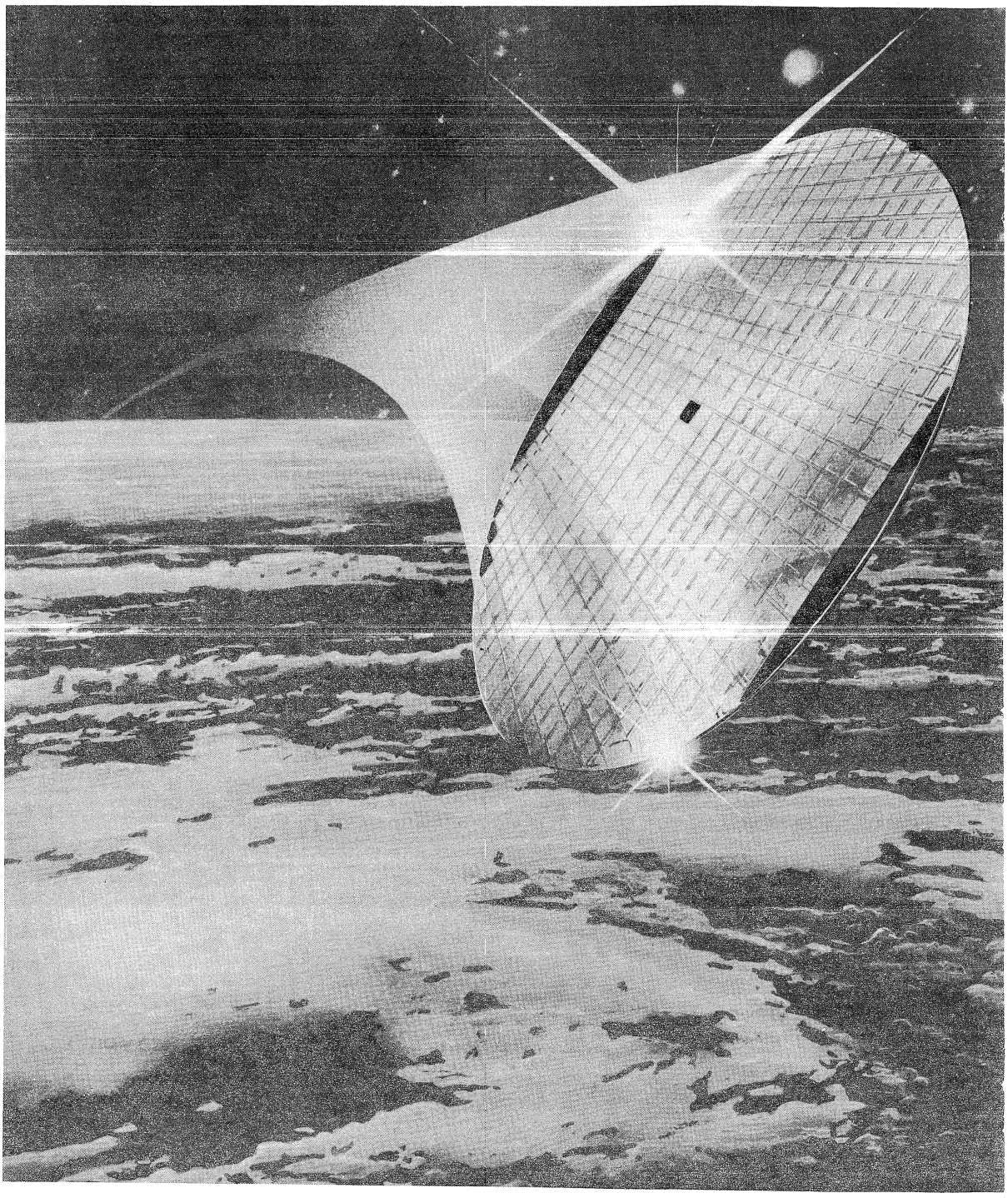


Introduction

Semiconductors are the backbone of most of today's high-tech systems for commercial, industrial, and defense applications. Whether they are found in land, air, satellite, or spaceprobe systems, such devices are often subjected to severe heat, cold, vibration, and shock. Various types of radiation, occurring either in nature or the result of man-made sources, also present critical environmental problems. In fact, it has been known for years that radiation can change the electrical properties of solid state devices, leading to possible system failure. In particular, Gamma Rays, X-Rays and neutron bombardment have proven most harmful. Radiation-hardened devices and circuits have been developed to minimize the impact of such forces. Moreover, radiation hardening now allows system designers to take full advantage of the benefits of CMOS technology in high performance, high reliability products destined for use in radiation environments.

State-of-the-art wafer fab clean room facilities at Harris are maintained up to a class 10 level.

Hardening For Radiation Environments

Military and space applications require radiation hardened CMOS to operate at total dose and transient radiation levels which are beyond the capabilities of non-hardened devices. Radiation, which in the past had prohibited the use of CMOS technology, is no longer a barrier. Proper design and processing techniques allow CMOS devices to operate in this extremely harsh environment. This process enables system designers to take advantage of the extremely low standby and operating power requirements of CMOS. This publication is a primer on the effects of radiation on CMOS. It will provide the reader with a general understanding of the sources, doses, dose rates, and basic mechanisms that occur during operation of CMOS integrated circuits in a radiation environment.

Natural radiation sources

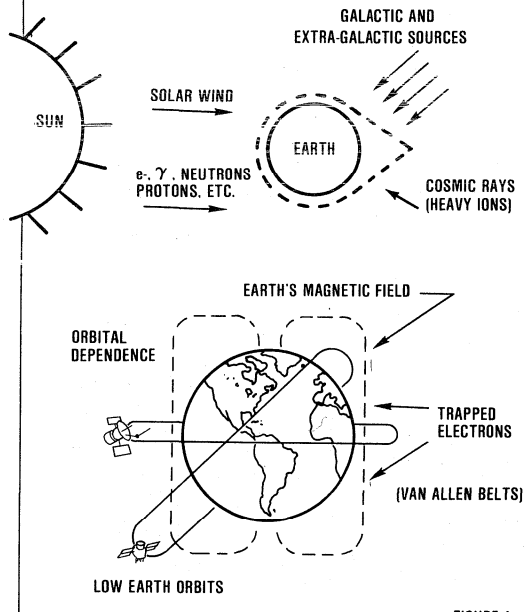


FIGURE 1.

Man made radiation sources

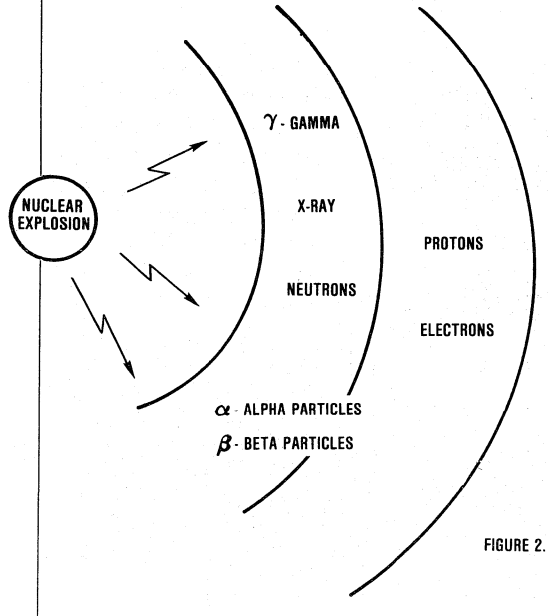


FIGURE 2.

An integrated circuit can be called radiation hardened if it is designed, built, and tested to ensure operation within specifications after exposure to a specified level of radiation. Radiation hardened (rad-hard) circuits are guaranteed to meet or exceed specified radiation levels that are one to two orders of magnitude greater than the levels attained with radiation tolerant devices. Radiation tolerance is usually based on typical performance and does not include guarantees of hardness levels.

Military Radiation Hardness Designators

MIL-M-38510 requires a Radiation Hardness Assurance (RHA) designator to be incorporated into JAN microcircuit part numbers which are listed in Table 1, Appendix A.

The purpose of the RHA designator is to express the reliability of rad-hard microcircuits subjected to various levels of radiation.

In general, hardened CMOS devices will not fail, even in typically high radiation environments. Semiconductor technology has been improved to enable devices to continue to function in much higher radiation levels than ten or even five years ago. Although all semiconductors have some intrinsic resistance or tolerance to radiation, Harris Semiconductor has been able to achieve much higher levels of hardness and high reliability in its rad hard CMOS devices. This has been accomplished through:

- Integrated circuits specifically designed for radiation hardness.
- Special radiation hardening fabrication processes.
- Continuous screening and quality control.

Sources of Radiation

Radiation can occur naturally or as the result of man-made sources, such as nuclear explosions and reactors.

As shown in Figure 1, space contains many sources of radiation not found on earth. The space environment is one of major concern for satellites, planetary travel and deep space probes.

Figure 2 identifies man-made radiation sources. A summary of the irradiating particles is given in Appendix A.

Radiation can be divided into three basic categories - photons, charged particles and neutrons.

Photons

Photons that have significant effects on packaged integrated circuits are Gamma Rays and X-Rays. The difference between Gamma Rays and X-Rays (and between light, radio waves, infrared radiation) is the energy of the photons. Gamma Rays and X-Rays are energetic enough to penetrate IC packaging materials and interact with the silicon and silicon dioxide layers in the circuit, and affect device performance. Even these high energy photons can be stopped by shielding. The best materials for shielding photons are those with high nuclear cross sections. Generally speaking, dense materials such as concrete or lead have high nuclear cross sections.

Charged Particles

A beta particle is an electron traveling at a large fraction of the speed of light. It is the same as an electron orbiting a nucleus, differing only in speed. The range of a beta particle is about 20 feet in air, and can be stopped by 1/16 inch sheet of aluminum.

An alpha particle is a helium nucleus; that is, a helium atom with the electrons stripped away. It also travels at a large fraction of the speed of light, and can be stopped by a sheet of paper.

Ions are charged particles formed when one or more electrons are stripped away or added to a previously neutral atom or molecule.

Neutrons

A neutron is a particle with no electric charge. Its mass is approximately the same as that of a proton. In nature, neutrons are bound in the nucleus of an atom. They can be knocked out in various types of nuclear interactions.

Interactions

As one would imagine, the interactions of a particle with a target will depend on the properties of each. This dependency can be listed as:

- Particle Properties
  1. Mass
  2. Charge
  3. Kinetic Energy
- Target Properties
  1. Mass
  2. Charge
  3. Density

The types of interactions that can occur with each particle type are given in Appendix B.

The interaction of particles and energies can actually be broken down into two main mechanisms which dominate the effect of radiation in materials in the environments with which we are concerned:

1. Displacement of atoms from their lattice structure (displacement damage).
2. Generation of electron-hole pairs (ionization). Both effects can cause temporary (transient) or permanent damage to semiconductors.

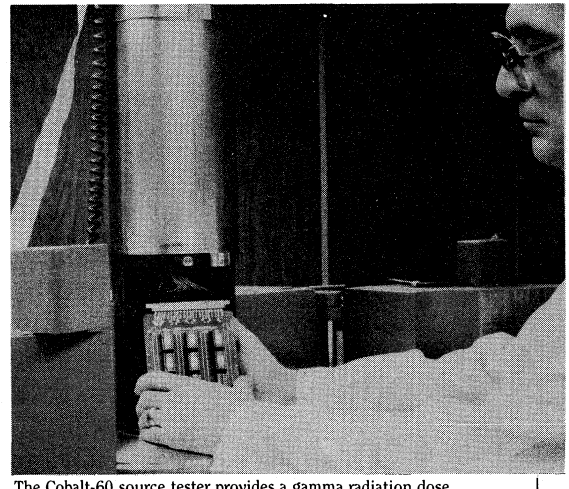
Energy Measured in RADs

The energy transferred to a material by ionizing radiation is measured in terms of RADs (radiation absorbed dose). One RAD is equal to the energy of 100 ergs per gram of material. The material must be specified, because this energy will differ with each material:

One rad (Si) = 100 ergs/gm (Si)
One gray (Gy) = 100 RADs

The ionizing dose rate is referenced in rad (Si)/sec. Particles are referred to in terms of concentration as well as the time integral of concentration:

Flux = Particles/(cm^2 x sec)
Fluence = Particles/cm^2



The Cobalt-60 source tester provides a gamma radiation dose.

Radiation levels

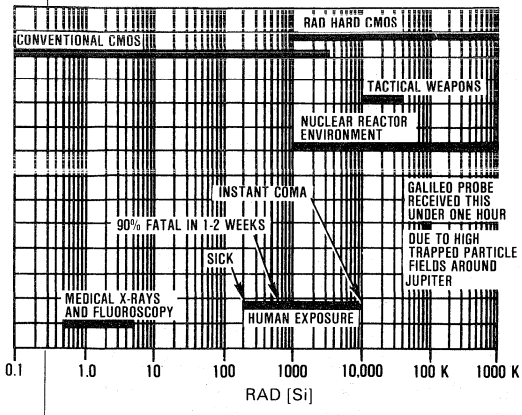


FIGURE 3.

N-channel transistor

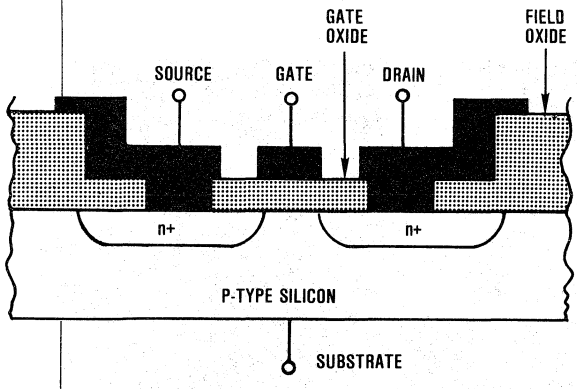


FIGURE 4.

Radiation Effects on CMOS Circuits

As mentioned earlier, radiation affects circuits primarily through two basic mechanisms, displacement damage and ionization.

Displacement damage is caused by heavy charged particles and neutrons. Neutrons are not considered to be a problem in CMOS, as they are in bipolar, until they reach a fluence of $10^{15}N/cm^2$ or greater. Heavily charged particles can cause single event upset. This topic will be discussed later.

Photon interactions, fast neutron interactions (E>1 MeV) and charged particles cause ionization, which is of major concern in CMOS. Photons (gamma) radiation is the primary source of this ionization radiation.

Various levels of radiation exist naturally and can also be generated by man. Figure 3 depicts these levels and also shows the levels where radiation-hardened CMOS is generally utilized. This should give the reader a better idea of the spectrum of radiation levels and the effects of radiation relative to man. Be sure to note the scale is a log scale.

Ionizing Radiation Effects in CMOS/VLSI

The definition of a rad was presented earlier but, how does this relate to an actual device? First we will look at pure silicon:

1 RAD (Si) = 100 ergs/gm x
1 electron-hole pair (e-h)
generated for 3.6ev absorbed in silicon

then 1 RAD = (100erg/gm) =

$$\left(\frac{10\text{-}^{7}eV}{1.6 \times 10\text{-}^{19}\ erg}\right) \times \left(\frac{2.3gm}{cm^3}\right) \times \left(\frac{1(e\text{-}h)}{3.6eV}\right)$$

1 RAD = 4×10^{13} (e-h)/cm^3 generated

It should be evident that as the dose increases, the number of carriers generated in silicon will also increase. In a space environment, the ionizing radiation that is absorbed by a device can be accumulated over a long period of time; for example, 100K RADs (Si) in 20 years. This is referred to as the Total Dose. However, in a weapons environment, a device may be subjected to an extremely large dose within a short period of time.

Doses can be on the order of 10^8 - 10^9 RADs (Si) for a few nanoseconds to hundreds of nanoseconds. This type of photon radiation is referred to as Transient Radiation, denoted by gamma dot ($\dot{\gamma}$)-the derivative of gamma with respect to time.

A typical N-channel transistor is shown in Figure 4.

A MOS transistor can be looked at as a capacitor with the metal and semiconductor as the plates and the gate oxide (silicon dioxide SiO_2) as the dielectric.

Ionizing radiation produces its effects in the gate oxide and also the field oxide regions. These effects are threshold voltage shifts and channel mobility degradation.

The ionization process is illustrated in Figure 5. At $t=0^-$ (Figure 5a), the condition prior to irradiation is shown. At $t = 0$ (Figure 5b), the ionizing energy is delivered to the SiO_2, and the electron-hole population is generated.

Immediately after ionization, the process of electron-hole recombination will occur, but so will electron transport. Electron mobility in SiO_2 at room temperature is approximately 20 cm^2/V-sec, while hole mobility is approximately 2 x $10^{-5}cm^2$/V-sec. Because of the applied voltage, any electrons that do not undergo recombination will be swept to the gate and removed in picoseconds, leaving behind the less mobile holes.

These holes will begin a transport process toward the Si-SiO_2 interface as shown in Figure 5e. Some holes will pass into the silicon, while others will become trapped at defect centers very near the interface of the gate oxide and the bulk silicon. (2,3)

Figure 6 depicts the shift in the C-V curve associated with the entire process and the resulting permanent shift due to the trapped charge buildup. In the case of the N-channel device shown in Figure 4, the trapped positive charge will continue to build up and, in effect, make it easier to create the N-channel (inversion layer). This will lower the threshold voltage. See Figure 7.

The reversal of the threshold shift is caused by saturation of the surface traps and interface state generation at the Si-SiO_2 interface that appear with higher levels of gamma radiation.

This mechanism of interface state generation is not well understood at this time. The simple fact that two different crystal structures meet, silicon and silicon dioxide, and interface will result with some irregularities. This number of irregularities increases with increased irradiation.

Carrier transport mechanism

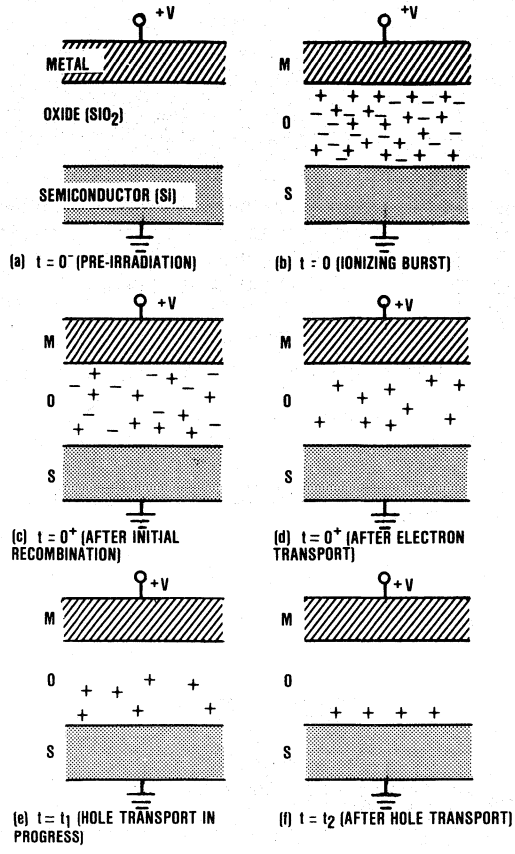


FIGURE 5. Illustration of recombination, transport, and trapping of carriers in SiO_2 films.

C-V curve

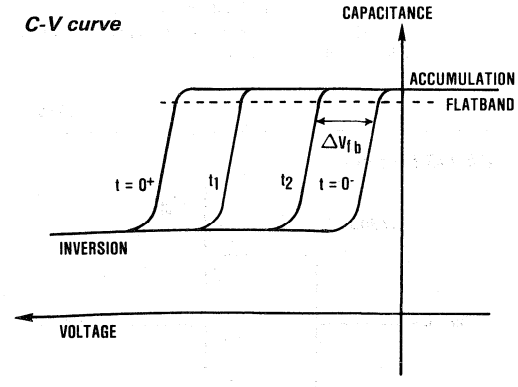


FIGURE 6. Capacitance-voltage curves corresponding to the conditions illustrated in Figure 5.

Total dose effects on P and N channel transistors

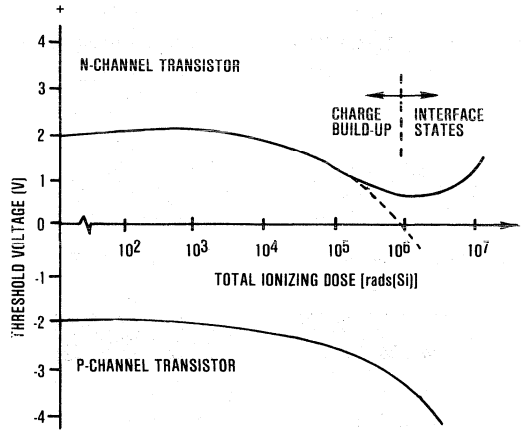


Illustration of the effect of positive charge buildup and interface state production on the threshold voltage in irradiated n- and p-channel MOS transistors.

FIGURE 7.

Carrier mobility degradation

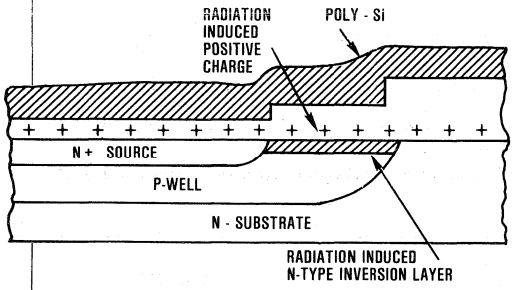


Illustration showing inversion layer which allows current to flow between N- substrate and N+ source.

FIGURE 8.

CMOS inverter

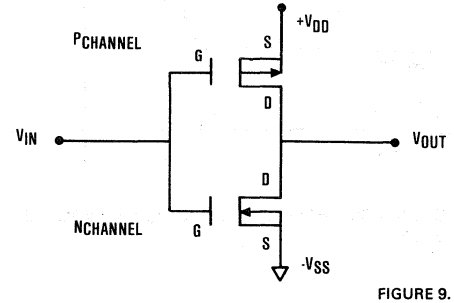


FIGURE 9.

In the case of the corresponding P-channel device, the buildup will make it more difficult to create an inversion layer in an enhancement mode P-channel transistor. The effect of gamma radiation on a P-channel threshold is shown in Figure 7.(2)

The net effect of gamma radiation on a CMOS device as a function of threshold shifts is:

1. N-channel devices are easier to turn on or can actually become depletion mode.
2. P-channel devices become more difficult to turn on.

Mobility

Carrier mobility degradation occurs because of the presence of trapped charge near the Si-SiO_2 interface and interface state generation. Interface state generation is the dominant of the two effects.

Interface state generation is negligible at lower levels of gamma radiation. As these radiation levels are increased above 10^6 rad (Si), mobility degradation will affect P and N channel device performance, with increased interface states being the primary cause of the degradation.

Another performance problem induced by the radiation is the increase in leakage current due to surface effects. The ionizing radiation produces excess carriers which can also form a channel between the N+ source and N– substrate (Figure 8.) This effect is dramatically reduced through processing techniques.

Annealing

Annealing is the time-dependent detrapping of trapped charge at the Si-SiO_2 interface. It is sometimes referred to as a self-healing effect, which is somewhat true. However, the time constant involved is on the order of minutes to over one year, depending on the level of radiation and the type of processing. The surface states generated are relatively permanent, but can be annealed with high temperatures (>125°C). Any lattice damage (interstitials, vacancies) is permanent.

CMOS Advantages

Since continuous operation in most systems is imperative, integrated circuits have been designed to operate within specifications after being subjected to high levels of radiation. Radiation-hardened CMOS has been developed because CMOS technology provides tremendous advantages over other hardened technologies.

A typical CMOS inverter is shown in Figure 9. It is called CMOS because it is comprised of two complimentary MOS devices. It is a voltage-dependent device, and does not require large current for operation as do NMOS or bipolar devices. The low current requirements, typically 1/5 that of NMOS, provides several benefits.

First, its state of operation is cooler. This allows an increased packing density and lower power requirements. NMOS exhibits an exponential increase in power required as the transistor count goes up.

The lower power requirements yield a cooler operating device. Now systems without heat sinks or cooling fans are easily achievable. The reduction in required current produces smaller and lighter power supplies.

Even more desirable for the system designer is the fact that CMOS lends itself to use in static design. That is, a processor or memory retains its data values even with its clock stopped. Current draw under this condition is under 500μA for typical CMOS circuits. Lighter, smaller, cooler operating devices are essential for space applications where lighter payloads combined with low power consumption and static designs make CMOS ideal for satellite, deep space probes, and battery-powered applications.

Another advantage of CMOS is its property of high noise immunity. Fluctuations in Vin must reach the threshold voltage to cause a change in a CMOS inverter output.

Hardened CMOS at Harris

Harris has been involved in understanding the effects of radiation on semiconductors since 1962, when Radiation Inc. was asked to develop highly reliable custom devices. Radiation Inc. merged with Harris in 1967. Today Harris Semiconductor offers an extensive line of radiation-hardened data sheet products.

Radiation hardening is accomplished in two ways. The first is through specific design and processing techniques while the second method relies soley on processing techniques.

Basic Processes

Several methods can be used to harden processes used to fabricate CMOS circuits. One of the first methods used at Harris was a modification of a self-aligned poly gate, junction isolated process by the insertion of a highly doped guardband around

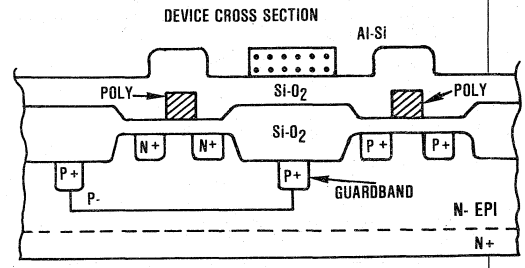


FIGURE 10A

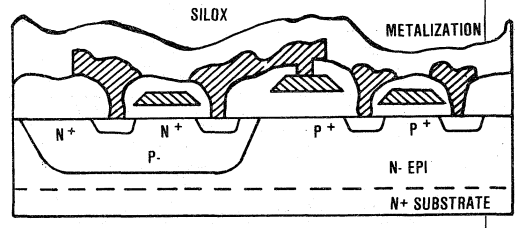


FIGURE 10B

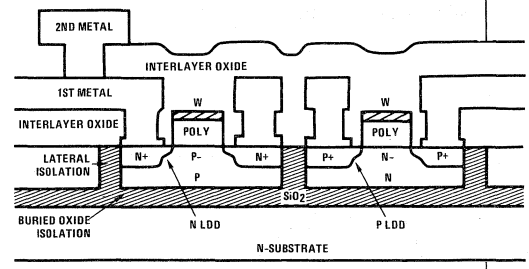


FIGURE 10C

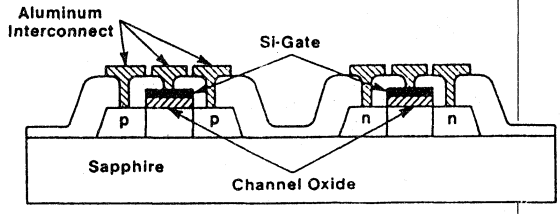
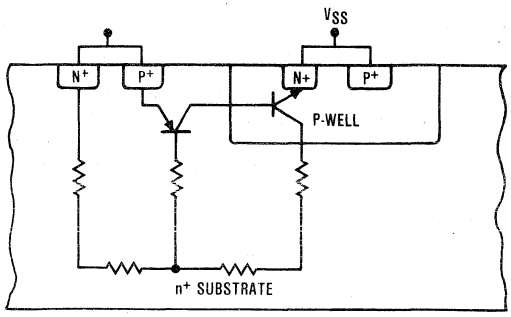
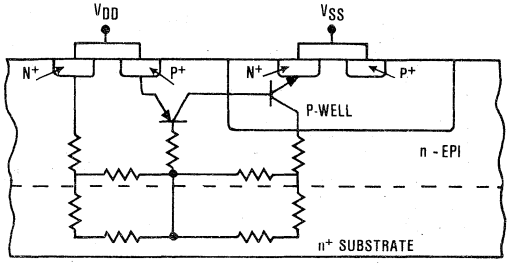


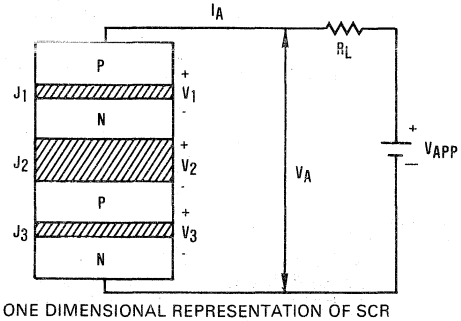
FIGURE 10D



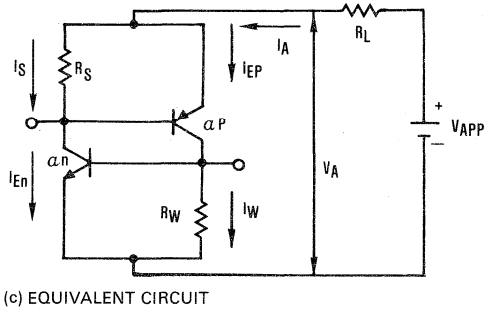
BULK CMOS STRUCTURE WITHOUT EPI LAYER



(a) BULK CMOS STRUCTURE WITH EPI LAYER



(b) ONE DIMENSIONAL REPRESENTATION OF SCR



(c) EQUIVALENT CIRCUIT

FIGURE 11.

the edge of the P well (Figure 10a). The presence of the guardband greatly increases the amount of charge trapped at the interface necessary to invert the silicon surface and allow leakage currents to flow. The disadvantage of this technique is that it consumes valuable chip real estate, increasing the chip size needed to implement a given function.

In order to minimize the chip size impact of hardening a circuit, another method was developed to prevent inversion of the P well surface. Instead of increasing the amount of trapped charge necessary for inversion (guardband process) a field oxide that minimized charge generation was developed. A process implementing hardened field oxides is shown in Figure 10b. Gate oxides were also hardened to minimize inverter threshold (VIL, VIH) shifts.

Hardened gate oxides can also be used on processes that use insulators instead of junctions for isolation. Harris SIMOX (silicon isolated by implanted oxygen, Figure 10c) and SOS (silicon on sapphire, Figure 10d) are examples of insulation isolated processes. In the SIMOX process, oxygen atoms are implanted beneath the silicon surface to create an insulating layer of silicon dioxide between the active circuit area and the wafer substrate. In the SOS process, an epitaxial silicon layer is grown over the insulating sapphire substrate. Silicon between the active transistor areas is etched away leaving each transistor on an insulated island. Both processes eliminate the silicon surfaces between transistors and the leakages associated with inversion of the surfaces.

Another significant advantage of insulator isolated processes is elimination of the possibility of latchup. The four layer SCR structure that is turned on when junction isolated circuits latch is not present in the SOS or SIMOX processes.

Latch-Up

A parasitic four layer Silicon Controlled Rectifier (SCR) structure exists in junction isolated CMOS processes (Figure 11). Events such as high dose rate pulses or heavy ion hits can activate the SCR, creating a low impedance path from V_{DD} to G_{nd} [5]. The susceptibility to latchup can be reduced by building these circuits on wafers with an epi layer. (It can also be eliminated by using SOS/SIMOX processes.) The epi layer is grown over a highly doped substrate; the substrate provides a low resistance path to V_{DD}, and shunts current away from

the base of the parasitic bipolar transistors (Figure 11). The lightly doped epi provides the correct doping level for the construction of high quality transistors. Optimization of the epi thickness can increase the latchup holding voltage to levels above the maximum specified supply voltage, rendering the circuits latchup free.

Single Event Phenomena

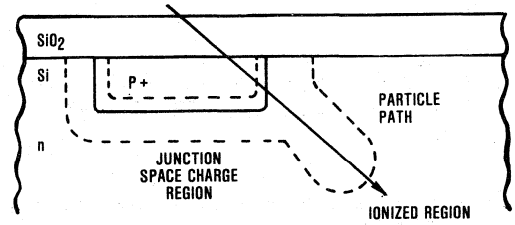
Electronics in most space environments are subject to bombardment by high speed heavy ions, known as cosmic rays, and protons. These particles leave ionized tracks as they penetrate silicon (Figure 12). The amount of charge generated is measured as Linear Energy Transfer (LET), expressed in Mev/mg/cm^2. A particle's LET depends on the particle type, its' kinetic energy, and the angle at which it strikes the silicon surface.

Charge collection in sensitive circuit nodes (such as the drain of an "off" N or P channel transistor) can result in a change of state of circuit memory elements. An example of a circuit that can be sensitive to this type of event (a single event upset or SEU) is shown in Figure 13a. If a particle with sufficient LET strikes the drain of one of the "off" transistors in the memory cell, the cell can change state. The current pulse in the reverse biased junction (resulting from the collection of the charge generated by the particle) will cause a perturbation in the output voltage of the affected inverter. This voltage is fed back to the input of the other inverter and the logic state stored has changed.

The amount of charge needed to change the memory cell's logic state can be greatly increased by the addition of cross coupling resistors shown in Figure 13b. These resistors greatly increase the RC time constant of path to the inverter inputs, therefore, voltage transients caused by the current pulse are much smaller than in the non resistor cell. Adding the resistors greatly increases the upset threshold. Harris RAMs using this technique have soft error thresholds in excess of 80 MeV/mg/cm^2 (6).

Another, more severe consequence of heavy ions is the triggering of latchup. A circuit's sensitivity can be minimized by the use of an epi layer or eliminated by the use of an insulation process, as discussed (such as SOS or SIMOX). The insulation isolated processes greatly reduce the ionized track length and charge collection, which makes them inherently insensitive to upset.

Soft error



CHARGE GENERATED DETERMINED BY:

SUBSTRATE DOPING
PATH
MASS OF PARTICLE — IRON GROUP (Fe, Ar, Kr) AT 100-150 MeV ARE WORST
ENERGY OF PARTICLE

FIGURE 12.

Memory cells

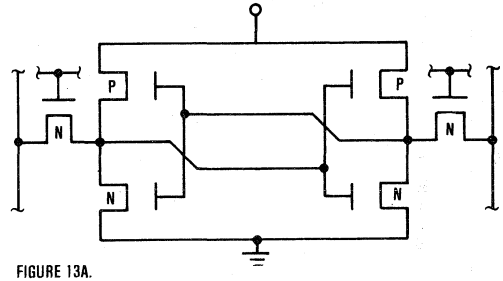


FIGURE 13A.

MODIFIED 6T CELL

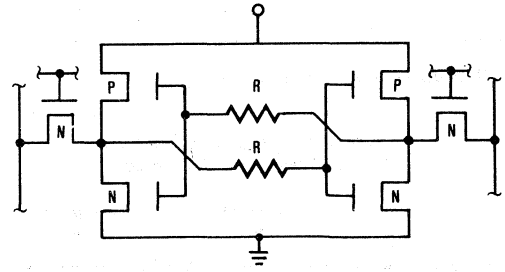
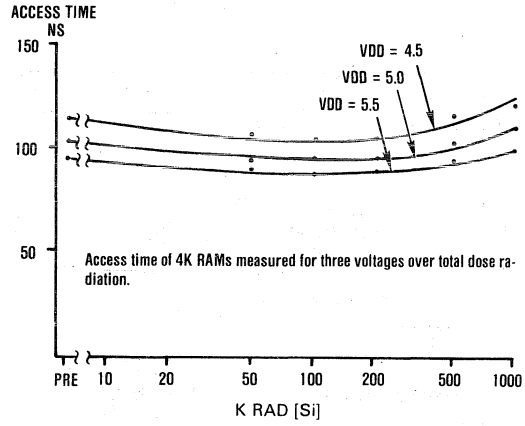


FIGURE 13B.



Access time of 4K RAMs measured for three voltages over total dose radiation.

FIGURE 14.

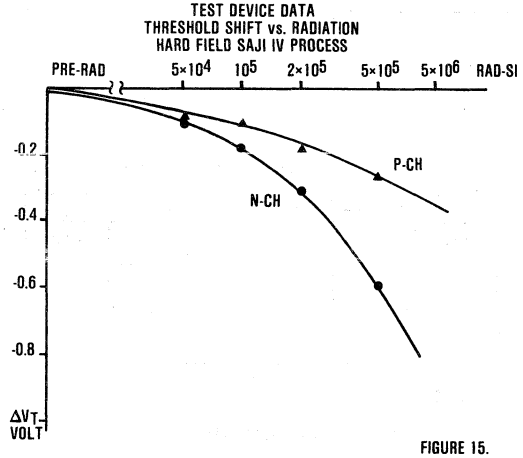


FIGURE 15.

Radiation effects summary

Bulk CMOS Integrated Circuits Can Typically Meet The Following Levels:

	Standard CMOS	Hardened CMOS
Neutrons	$>10^{15}$n/cm^2	
Total Dose	1K - 3K Rad-Si	10^5 - 10^6 Rad-Si
Latchup γ	$\sim 10^9$ Rad/Sec	None
Cosmic Ray	Kr and Ar	
Upset γ	5×10^7 Rads/Sec	3×10^8 Rads/Sec
Cosmic Ray	Kr and Ar	None (CROSS COUPLED RESISTORS)

FIGURE 16.

Hardened Circuit Parameter Shifts Over Total Dose Irradiation

Figure 14 show the response of the HS-6504RH to total dose irradiation. These shifts are typical of Rad Hard circuits produced by Harris. The RAM's access time initially improves with accumulated total dose as the N channel thresholds shift downward; with increasing dose, channel mobility degradation begins to dominate, and the circuit's access time begins to increase. At any point in the irradiation, access time is less than the 200ns spec. limit. The actual threshold voltage shifts for test transistors are shown in Figure 15.

A summary of radiation effects on standard vs. hardened CMOS is presented in Figure 16. From this figure, it is clear that hardened CMOS is superior to standard bulk CMOS in the critical areas of total dose hardness and immunity to latch-up.

Harris High Reliability

Reliability is a critical item, and often the limiting factor in systems that are unmanned or must remain on line in remote areas. It is an issue that has distinguished Harris Semiconductor as a leader in the design and manufacture of high-reliability parts from cardiac pacer circuits to radiation-hardened memories, microprocessors, op amps and full custom devices.

Harris maintains strict lot qualification, screening and testing procedures. A stringent radiation screening procedure is performed to assure continuous adherence to a circuit's respective data sheet.

In order to do this, samples are selected from wafers in a run. All wafers in a run will have been processed together through all high-temperature steps and metallization. The sample die are then assembled and tested for functionality.

The sample devices are subjected to the total dose radiation level guaranteed for each device, using Harris' own Gamma Cell 220 Cobalt 60 source. The test conditions for the device will be specified in its own data sheet.

The samples are then tested and accepted by the criteria identified in the respective data sheet.

Appendix A

Summary of irradiating particles:

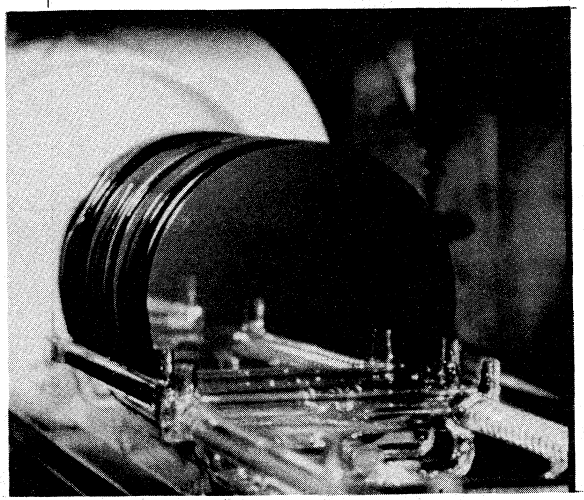
Neutrons
Gamma Rays
X-Rays
Electrons
Protons
Alpha Particles
Ions
Cosmic Rays
- Protons
- Electrons
- Alpha Particles
- Heavier Ions

These particles can be broken down into three categories:

A) Photons
- X-Rays
- Gamma Rays

B) Charged Particles
- Electrons
- Protons
- Alpha Particles
- Beta Particles
- Ions

C) Neutrons



Wafers enter a furnace for oxidation.

Table 1

Mil-M-38510 Radiation Hardness Assurance Designators

DESIGNATOR	TOTAL DOSE RAD (SI)	NEUTRON FLUENCE LEVEL n/cm^2
/	NO RHA	NO RHA
M	3000	2 x 10^{12}
D	104	2 x 10^{12}
R	105	2 x 10^{12}
H	106	2 x 10^{12}

Appendix B

Types of particle interaction:

Photons
- Photoelectric Effect
- Compton Scattering
- Pair Production

Charged Particles
- Rutherford Scattering
- Nuclear Interactions (Heavy Particles)

Neutrons
- Scattering
- Absorption

Photons

Photons are pure energy and are electrically neutral. Their effect on target atoms depends on their energy and also the atomic number (Z) of the target.

In all three cases, a free electron is generated. In the photoelectric effect, the photon is completely absorbed by the emitted electron. If there was sufficient energy to free a K shell electron, then an L shell electron will drop down to take its place. An x-ray or low-energy Auger electron will then be emitted, depending on Z. See Figures B1 and B2.

In Compton scattering, the photon has a greater amount of energy than is needed to free an electron from the target material. As a result, the photon is scattered, yielding an electron and a lower energy photon.

In pair production, the photon has a minimum of 1.02 MeV. At this energy, a photon striking a target of high Z is completely absorbed. A positron-electron pair is formed.

The relationship of photon energy and atomic number to interaction type is shown in Figure B3. It is clear from this graph that for silicon (Z = 14), pair

production dominates at energies above 20 MeV, and the photoelectric effect dominates at energies below 50 KeV. Compton scattering is the interaction of most concern in silicon (2).

Charged Particles

Rutherford scattering is the interaction of charged particles. It can cause both excitation and ionization of atomic electrons. If the particle has enough energy, it can displace atoms in the lattice or even undergo nuclear interactions similar to those exhibited by neutrons.

Neutrons

Nuclear interactions involving neutrons can be classed in two categories: scattering and absorption.

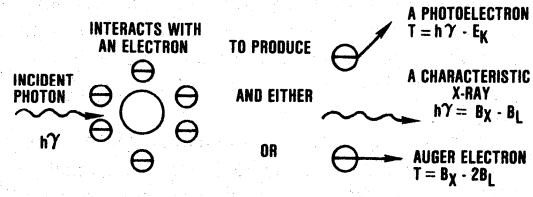
In scattering reactions the process is similar to photon scattering. The incident neutron remains free at a reduced energy, having transferred some of its energy to the target nuclei.

The absorption process is similar to the photoelectric effect of photon absorption, in that the neutron and its energy are absorbed and new particles are generated.

Neutron energies range from a few eV in thermally generated neutrons, to 1 MeV for fast neutrons (fission reactor neutrons), to 14 MeV for fusion neutrons. Neutrons can dislodge an atom from its lattice position.

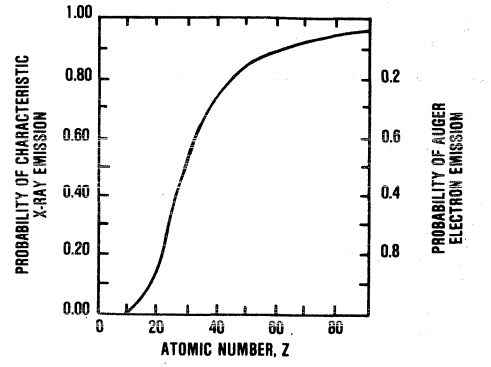
Displacement damage can also occur with high energy charged particles. Displacement of atoms from their lattice position leaves behind a vacancy. The displaced atom may come to rest in a non-lattice position. This non-lattice atom is referred to as an Interstitial.

These abnormalities in the crystal structure are called Defects (see Figure B4). Simple defects are called Point or Isolated Defects, while regions containing a large number of defects are known as Defect clusters.



Sequence of Events in Photoelectric Collisions, shown schematically above.

FIGURE B1.



Probabilities of Auger Electron and Characteristic X-Ray Emission Following the Ejection of a K-Shell Electron.

FIGURE B2.

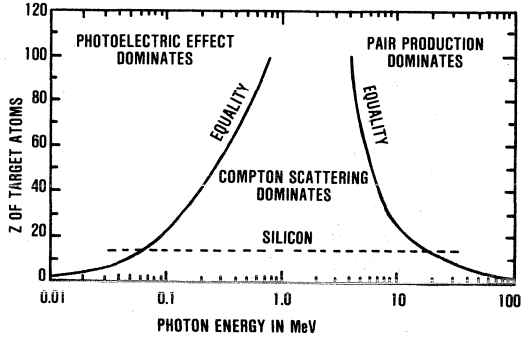
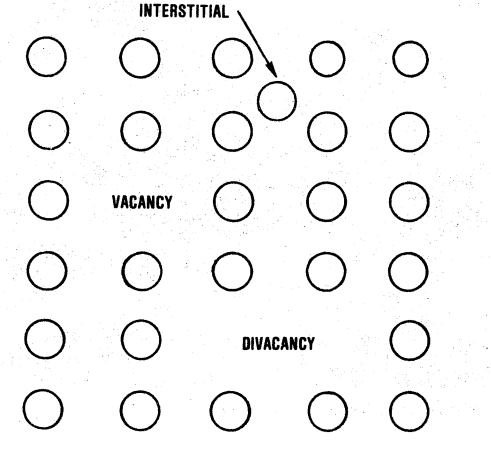


Illustration of the relative importance of the three photon interactions as a function of Z and photon energy. The solid lines correspond to equal interaction cross sections for the neighboring effects. The dashed line illustrates the situation for photon interactions with silicon.

FIGURE B3.



Schematic illustration of three types of simple defects in a lattice structure.

FIGURE B4.

A Total Solution Organization

With over two decades of problem solving experience ... Harris Semiconductor is a total solution organization. Major military program involvement and specialized product needs are met.

Harris offers a proven means of getting high performance, application-specific, custom, semicustom, standard cell and gate arrays. Strategic programs include Trident, Peacekeeper, B-1B, and SICBM. Tactical programs such as Copperhead, Hellfire, the F-16, and F-18, along with many others, are serviced by this group. Harris also has design and production facilities that are COMSEC cleared for classified communications programs.

Data-Sheet plug-in parts that replace non-hardened counterparts are available. Rad-hard bipolar and rad-hard CMOS products in analog, digital, or in combination are available. Advanced Schottky logic and high voltage analog, built to high-rel requirements in your choice of configurations are also available.

For custom and semicustom products, Harris Semiconductor provides a systems house approach to customer interfacing. A Program Manager is assigned to you at the very beginning. From design, masks, fabrication, assembly and testing ... your exact needs are met in product and timeframe. As little or as much as you want!

Steve Rivet is the Applications Engineer for Harris' Military and Aerospace Division. He can be reached at 407-724-7319 to provide application information for Harris' radiation hardened circuits.

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(2) J. Srour, "Basic Mechanisms of Radiation Effects on Electronic Materials, Devices, and Integrated Circuits," IEEE 1982 Annual Conference on Nuclear and Space Radiation Effects.
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(7) T.J. Sanders, "Silicon Gate CMOS on Bulk Silicon for Ionizing Radiation Environments," IEEE Transactions on Nuclear Science, Vol. NS-26, No. 6, p. 5056-5059, Dec. 1979.

RAD-HARD 3

DISCRETE DEVICES (POWER MOSFETs)

RHAP^{SM} Radiation Hardened Assurance Program

DISCRETE DEVICES (POWER MOSFETs) (Continued)

INTRODUCTION TO RAD HARD MOSFETS

TACTICAL APPLICATIONS:

— Radiation Hardness Assurance Program
— Rated at 10K Rads (Si)

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users which assures a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and treated for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

STRATEGIC APPLICATIONS:

— Rated at 100K and 1000K Rad(Si)

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 60 amperes, and on resistance as low as 25 milliohms. Total dose hardness is offered at 100K and 1000K RAD(-Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 rads/sec without current limiting and 2E12 rads/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

TACTICAL LEVEL SELECTIONS (RHAP)
RAD HARD MOS

N—CH or P—CH	Die Size	Voltage (V)	RHAP Number *			
			TO–3	TO–39	TO–254	TO–257
N	3	100	FRM130D	FRL130D	—	FRS130D
		200	FRM230D	FRL230D	—	FRS230D
		250	FRM234D	FRL234D	—	FRS234D
		500	FRM430D	FRL430D	—	FRS430D
N	4	100	FRM140D	—	—	FRS140D
		200	FRM240D	—	—	FRS240D
		250	FRM244D	—	—	FRS244D
		500	FRM440D	—	—	FRS440D
N	5	100	FRK150D	—	FRF150D	—
		200	FRK250D	—	FRF250D	—
		250	FRK254D	—	FRF254D	—
		500	FRM450D	—	FRF450D	—
N	6	100	FRK160D	—	**	—
		200	FRK260D	—	**	—
		250	FRK264D	—	**	—
		500	FRK460D	—	**	—
P	3	100	FRM9130D	FRL9130D	—	FRS9130D
		200	FRM9230D	FRL9230D	—	FRS9230D
		500	FRM9430D	FRL9430D	—	FRS9430D
P	4	100	FRM9140D	—	—	FRS9140D
		200	FRM9240D	—	—	FRS9240D
		500	FRM9440D	—	—	FRS9440D
P	5	100	FRK9150D	—	FRF9150D	—
		200	FRM9250D	—	FRF9250D	—
		500	FRM9450D	—	FRF9450D	—
P	6	100	FRK9160D	—	**	—
		200	FRK9260D	—	**	—
		500	FRK9460D	—	**	—

* NOTE— The reliability screening level code has been omitted for convenience. RHAP selections are available in all four screening levels.

** Could be offered in the TO-258 package.

N–CHANNEL RAD HARD POWER MOSFETS

PART NO.	DIE SIZE (MILS)	DIE SIZE	INITIAL RATINGS: MAX RATED BVDSS (VOLTS)	INITIAL RATINGS: MAX RATED IDS (AMPS)	INITIAL RATINGS: MAX RATED RDS(ON)	INITIAL RATINGS: VGS(TH) (Volts)	POST RAD: 10K RADS: BVDSS Volts	POST RAD: 10K RADS: VGS(TH) Volts	POST RAD: 10K RADS: RDS(ON) Ohms
FRM130	126 x 182	3	100	14	0.18	2—4	100	2—4	0.18
FRM230	126 x 182	3	200	8	0.50	2—4	200	2—4	0.50
FRM234	126 x 182	3	250	7	0.70	2—4	250	2—4	0.70
FRM430	126 x 182	3	500	3	2.50	2—4	500	2—4	2.50
FRL130	126 x 182	3	100	8	0.18	2—4	100	2—4	0.18
FRL230	126 x 182	3	200	6	0.50	2—4	200	2—4	0.50
FRL234	126 x 182	3	250	4	0.70	2—4	250	2—4	0.70
FRL430	126 x 182	3	500	2	2.50	2—4	500	2—4	2.50
FRM140	170 x 200	4	100	23	0.13	2—4	100	2—4	0.13
FRM240	170 x 200	4	200	16	0.24	2—4	200	2—4	0.24
FRM244	170 x 200	4	250	12	0.40	2—4	250	2—4	0.40
FRM440	170 x 200	4	500	6	1.40	2—4	500	2—4	1.40
FRK150	259 x 265	5	100	40	0.055	2—4	100	2—4	0.055
FRK250	259 x 265	5	200	27	0.10	2—4	200	2—4	0.10
FRK254	259 x 265	5	250	20	0.17	2—4	250	2—4	0.17
FRM450	259 x 265	5	500	10	0.60	2—4	500	2—4	0.60
FRK160	266 x 366	6	100	66	0.04	2—4	100	2—4	0.04
FRK260	266 x 366	6	200	46	0.07	2—4	200	2—4	0.07
FRK264	266 x 366	6	250	34	0.12	2—4	250	2—4	0.12
FRK460	266 x 366	6	500	17	0.40	2—4	500	2—4	0.40

P–CHANNEL RAD HARD POWER MOSFETS

PART NO.	DIE SIZE (MILS)	DIE SIZE	INITIAL RATINGS: MAX RATED BVDSS (VOLTS)	INITIAL RATINGS: MAX RATED IDS (AMPS)	INITIAL RATINGS: RATED RATED RDS(ON)	INITIAL RATINGS: VGS(TH) (Volts)	POST RAD: 10K RADS: BVDSS Volts	POST RAD: 10K RADS: VGS(TH) Volts	POST RAD: 10K RADS: RDS(ON) Ohms
FRM9130	126 x 182	3	100	6	0.55	2—4	100	2—4	0.55
FRM9230	126 x 182	3	200	4	1.30	2—4	200	2—4	1.30
FRL9130	126 x 182	3	100	5	0.55	2—4	100	2—4	0.55
FRL9230	126 x 182	3	200	3	1.30	2—4	200	2—4	1.30
FRM9140	170 x 200	4	100	11	0.30	2—4	100	2—4	0.30
FRM9240	170 x 200	4	200	7	0.72	2—4	200	2—4	0.72
FRK9150	258 x 264	5	100	26	0.125	2—4	100	2—4	0.125
FRM9250	258 x 264	5	200	17	0.30	2—4	200	2—4	0.30
FRK9160	266 x 366	6	100	40	0.086	2—4	100	2—4	0.085
FRK9260	266 x 366	6	200	26	0.20	2—4	200	2—4	0.20

STRATEGIC LEVEL SELECTIONS*
RAD HARD MOS (N-CHANNEL)

TA No.	TO-3		TO-39		TO-254		TO-257	
	Interim	Final	Interim	Final	Interim	Final	Interim	Final
17631	FRM130R	2N7271	FRL130R	2N7272	—	—	FRS130R	2N7273
	FRM130H		FRL130H		—		FRS130H	
17632	FRM230R	2N7274	FRL230R	2N7275	—	—	FRS230R	2N7276
	FRM230H		FRL230H		—		FRS230H	
17633	FRM234R	2N7277	FRL234R	2N7278	—	—	FRS234R	2N7279
	FRM234H		FRL234H		—		FRS234H	
17635	FRM430R	2N7280	FRL430R	2N7281	—	—	FRS430R	2N7282
	FRN430H		FRL430H		—		FRS430H	
17641	FRM140R	2N7283	—	—	—	—	FRS140R	2N7284
	FRM140H		—		—		FRS140H	
17642	FRM240R	2N7285	—	—	—	—	FRS240R	2N7286
	FRM240H		—		—		FRS240H	
17643	FRM244R	2N7287	—	—	—	—	FRS244R	2N7288
	FRM244H		—		—		FRS244H	
17645	FRM440R	2N7289	—	—	—	—	FRS440R	2N7290
	FRM440H		—		—		FRS440H	
17651	FRK150R	2N7291	—	—	FRF150R	2N7292	—	—
	FRK150H		—		FRF150H		—	
17652	FRK250R	2N7293	—	—	FRF250R	2N7294	—	—
	FRK250H		—		FRF250H		—	
17653	FRK254R	2N7295	—	—	FRF254R	2N7296	—	—
	FRK254H		—		FRF254H		—	
17655	FRM450R	2N7297	—	—	FRF450R	2N7298	—	—
	FRM450H		—		FRF450H		—	
17661	FRK160R	2N7299	—	—	—	**2N7300	—	—
	FRK160H		—		—		—	
17662	FRK260R	2N7301	—	—	—	**2N7302	—	—
	FRK260H		—		—		—	
17663	FRK264R	2N7303	—	—	—	**2N7304	—	—
	FRK264H		—		—		—	
17665	FRK460R	2N7305	—	—	—	**2N7306	—	—
	FRK460H		—		—		—	

* The reliability screening level code has been omitted for convenience. Strategic selections are available in all four screening levels.

** Will be registered in the TO-258 package.

N–CHANNEL RAD HARD POWER MOSFETS

TYPE NO.	INITIAL RATINGS				POST 100K RAD (Si)			POST 1M Rad (Si)		
	BVDSS Volts	IDS Amps	RDS (on) Ohms	VGS (th) Volts	BVDSS Volts	RDS (on) Ohms	VGS (th) Volts	BVDSS Volts	RDS (on) Ohms	VGS (th) Volts
2N7271	100	14	0.18	2 — 4	100	0.18	2 — 4	95	0.26	1.5 — 4.5
2N7272	100	8	0.18	2 — 4	100	0.18	2 — 4	95	0.26	1.5 — 4.5
2N7273	100	12	0.195	2 — 4	100	0.195	2 — 4	95	0.28	1.5 — 4.5
2N7274	200	8	0.50	2 — 4	200	0.50	2 — 4	190	0.70	1.5 — 4.5
2N7275	200	5	0.50	2 — 4	200	0.50	2 — 4	190	0.70	1.5 — 4.5
2N7276	200	7	0.515	2 — 4	200	0.515	2 — 4	190	0.72	1.5 — 4.5
2N7277	250	7	0.70	2 — 4	250	0.70	2 — 4	235	0.88	1.5 — 4.5
2N7278	250	4	0.70	2 — 4	250	0.70	2 — 4	235	0.88	1.5 — 4.5
2N7279	250	5	0.715	2 — 4	250	0.715	2 — 4	235	0.90	1.5 — 4.5
2N7280	500	3	2.50	2 — 4	500	2.50	2 — 4	TBD	2.75	1.5 — 4.5
2N7281	500	2	2.50	2 — 4	500	2.50	2 — 4	TBD	2.75	1.5 — 4.5
2N7282	500	3	2.52	2 — 4	500	2.52	2 — 4	TBD	2.77	1.5 — 4.5
2N7283	100	23	0.13	2 — 4	100	0.13	2 — 4	95	0.19	1.5 — 4.5
2N7284	100	17	0.145	2 — 4	100	0.145	2 — 4	95	0.21	1.5 — 4.5
2N7285	200	16	0.24	2 — 4	200	0.24	2 — 4	190	0.34	1.5 — 4.5
2N7286	200	12	0.255	2 — 4	200	0.255	2 — 4	190	0.36	1.5 — 4.5
2N7287	250	12	0.40	2 — 4	250	0.40	2 — 4	235	0.50	1.5 — 4.5
2N7288	250	9	0.415	2 — 4	250	0.415	2 — 4	235	0.52	1.5 — 4.5
2N7289	500	6	1.40	2 — 4	500	1.40	2 — 4	TBD	1.55	1.5 — 4.5
2N7290	500	5	1.42	2 — 4	500	1.42	2 — 4	TBD	1.57	1.5 — 4.5
2N7291	100	40	0.055	2 — 4	100	0.055	2 — 4	95	0.08	1.5 — 4.5
2N7292	100	25	0.07	2 — 4	100	0.07	2 — 4	95	0.10	1.5 — 4.5
2N7293	200	27	0.10	2 — 4	200	0.10	2 — 4	190	0.14	1.5 — 4.5
2N7294	200	23	0.115	2 — 4	200	0.115	2 — 4	190	0.16	1.5 — 4.5
2N7295	250	20	0.17	2 — 4	250	0.17	2 — 4	235	0.21	1.5 — 4.5
2N7296	250	17	0.185	2 — 4	250	0.185	2 — 4	235	0.23	1.5 — 4.5
2N7297	500	10	0.60	2 — 4	500	0.60	2 — 4	TBD	0.66	1.5 — 4.5
2N7298	500	9	0.615	2 — 4	500	0.615	2 — 4	TBD	0.68	1.5 — 4.5
2N7299	100	66	0.04	2 — 4	100	0.04	2 — 4	95	0.06	1.5 — 4.5
2N7301	200	46	0.07	2 — 4	200	0.07	2 — 4	190	0.10	1.5 — 4.5
2N7303	250	34	0.12	2 — 4	250	0.12	2 — 4	235	0.15	1.5 — 4.5
2N7305	500	17	0.40	2 — 4	500	0.40	2 — 4	5TBD	0.44	1.5 — 4.5

STRATEGIC LEVEL SELECTIONS*
RAD HARD MOS (P–CHANNEL)

TA No.	TO–3		TO–39		TO–254		TO–257	
	Interim	Final	Interim	Final	Interim	Final	Interim	Final
17731	FRM9130R	2N7307	FRL9130R	2N7308	—	—	FRS9130R	2N7309
	FRM9130H		FRL9130H		—		FRS9130H	
17732	FRM9230R	2N7310	FRL9230R	2N7311	—	—	FRS9230R	2N7312
	FRM9230H		FRL9230H		—		FRS9230H	
17735	FRM9430R	2N7313	FRL9430R	2N7314	—	—	FRS9430R	2N7315
	FRM9430H		FRL9430H		—		FRS9430H	
17741	FRM9140R	2N7316	—	—	—	—	FRS9140R	2N7317
	FRM9140H		—		—		FRS9140H	
17742	FRM9240R	2N7318	—	—	—	—	FRS9240R	2N7319
	FRM9240H		—		—		FRS9240H	
17745	FRM9440R	2N7320	—	—	—	—	FRS9440R	2N7321
	FRM9440H		—		—		FRS9440H	
17751	FRK9150R	2N7322	—	—	FRF9150R	2N7323	—	—
	FRK9150H		—		FRF9150H		—	
17752	FRM9250R	2N7324	—	—	FRF9250R	2N7325	—	—
	FRM9250H		—		FRF9250H		—	
17755	FRM9450R	2N7326	—	—	FRF9450R	2N7327	—	—
	FRM9450H		—		FRF9450H		—	
17761	FRK9160R	2N7328	—	—	—	**2N7329	—	—
	FRK9160H		—		—		—	
17762	FRK9260R	2N7330	—	—	—	**2N7331	—	—
	FRK9260H		—		—		—	
17765	FRK9460R	2N7332	—	—	—	**2N7333	—	—
	FRK9460H		—		—		—	

* The reliability screening level code has been omitted for convenience. Strategic selections are available in all four screening levels.

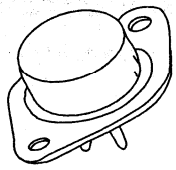
** Will be registered in the TO-258 package.

P–CHANNEL RAD HARD POWER MOSFETS

TYPE NO.	INITIAL RATINGS				POST 100K RAD (Si)			POST 1M RAD (Si)		
	BVDSS Volts	IDS Amps	RDS (on) Ohms	VGS (th) Volts	BVDSS Volts	RDS (on) Ohms	VGS (th) Volts	BVDSS Volts	RDS (on) hms	VGS (th) Volts
2N7307	100	6	0.55	2 — 4	100	0.55	2 — 4	95	0.80	2 — 6
2N7308	100	5	0.55	2 — 4	100	0.55	2 — 4	95	0.80	2 — 6
2N7309	100	6	0.565	2 — 4	100	0.565	2 — 4	95	0.82	2 — 6
2N7310	200	4	1.30	2 — 4	200	1.30	2 — 4	190	1.80	2 — 6
2N7311	200	3	1.30	2 — 4	200	1.30	2 — 4	190	1.80	2 — 6
2N7312	200	4	1.32	2 — 4	200	1.32	2 — 4	190	1.83	2 — 6
2N7316	100	11	0.30	2 — 4	100	0.30	2 — 4	95	0.44	2 — 6
2N7317	100	11	0.315	2 — 4	100	0.315	2 — 4	95	0.46	2 — 6
2N7318	200	7	0.72	2 — 4	200	0.72	2 — 4	190	1.00	2 — 6
2N7319	200	7	0.735	2 — 4	200	0.735	2 — 4	190	1.02	2 — 6
2N7322	100	26	0.125	2 — 4	100	0.125	2 — 4	95	0.18	2 — 6
2N7323	100	23	0.14	2 — 4	100	0.14	2 — 4	95	0.20	2 — 6
2N7324	200	16	0.30	2 — 4	200	0.30	2 — 4	190	0.42	2 — 6
2N7325	200	14	0.315	2 — 4	200	0.315	2 — 4	190	0.44	2 — 6
2N7328	100	40	0.085	2 — 4	100	0.085	2 — 4	95	0.12	2 — 6
2N7330	200	26	0.20	2 — 4	200	0.20	2 — 4	190	0.28	2 — 6

FRM130D

14A, 100V
RDS(on) = 0.18Ω



TO–204AA

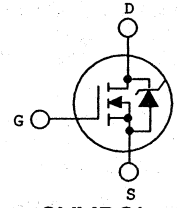
Radiation-Hardened N-Channel Power MOSFETs

FRM130D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 1.5nA per rad (Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
Continuous Drain Current, Id @Tc = 25°C	14	A
@Tc = 100°C	9	A
Pulsed Drain Current, I_{DM}	42	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	42	A
Continuous Source Current (Body diode), Is	14	A
Pulsed Source Current (Body diode), Ism	42	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

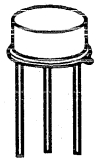
HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

FRL130D

8A, 100V

RDS (on) = 0.18Ω



JEDEC TO–205AF

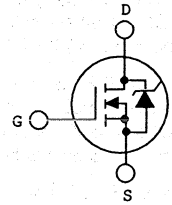
Radiation-Hardened N-Channel Power MOSFETs

FRL130D rated to 10K rads (Si) total dose and 2E12 n; typical photocurrent 1.5nA per rad (Si) sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

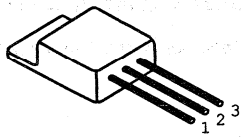
This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
Continuous Drain Current, Id @Tc = 25°C	8	A
@Tc = 100°C	5	A
Pulsed Drain Current, I_{DM}	24	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	24	A
Continuous Source Current (Body diode), Is	8	A
Pulsed Source Current (Body diode), Ism	24	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C



TO-257AA

Radiation-Hardened N-Channel Power MOSFETs

FRS130D rated to 10K rads (Si) total dose and 2E12 n; typical photocurrent 1.5nA per rad (Si)/sec transient dose

Features:

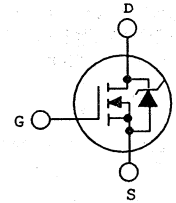
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}		100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)		100	V
Continuous Drain Current, Id	@Tc = 25°C	12	A
	@Tc = 100°C	7	A
Pulsed Drain Current, I_{DM}		36	A
Gate-Source Voltage, V_{GS}		±20	V
Power Dissipation, P_T:	At Tc = 25°C	50	W
	At Tc = 100°C	20	W
	Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)		36	A
Continuous Source Current (Body diode), Is		12	A
Pulsed Source Current (Body diode), Ism		36	A
Operating and Storage Temperature, Tjc, Tstg		−55 to +150	°C
Lead Temperature (During soldering): T_L			
	Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

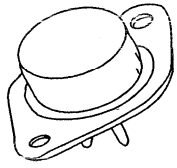
HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

FRM230D

8A, 200V

RDS (on) = 0.50Ω



TO–204AA

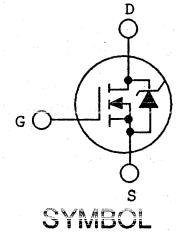
Radiation-Hardened N-Channel Power MOSFETs

FRM230D rated to 10K rads (Si) total dose and 2E12 n; typical photocurrent 3.0nA per rad (Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

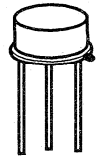
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
Continuous Drain Current, Id @Tc = 25°C	8	A
@Tc = 100°C	5	A
Pulsed Drain Current, I_{DM}	24	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	24	A
Continuous Source Current (Body diode), Is	8	A
Pulsed Source Current (Body diode), Ism	24	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRL230D

5A, 200V
RDS (on) = 0.50Ω



JEDEC TO–205AF

Radiation-Hardened N-Channel Power MOSFETs

FRL230D rated to 10K rads (Si) total dose and 2E12 n; typical photocurrent 3.0nA per rad (Si)/sec transient dose

Features:

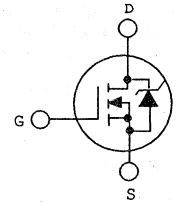
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
Continuous Drain Current, Id @Tc = 25°C	5	A
@Tc = 100°C	3	A
Pulsed Drain Current, I_{DM}	15	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	15	A
Continuous Source Current (Body diode), Is	5	A
Pulsed Source Current (Body diode), Ism	15	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

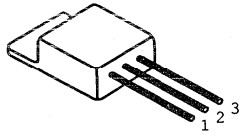
HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

PRELIMINARY

FRS230D

7A, 200V
RDS (on) = 0.515Ω

Radiation-Hardened N-Channel Power MOSFETs



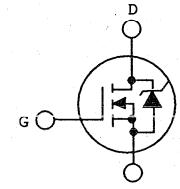
TO-257AA

FRS230D rated to 10K rads (Si) total dose and 2E12 n; typical photocurrent 3.0nA per rad (Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

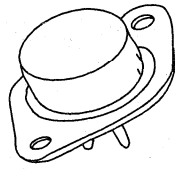
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
Continuous Drain Current, Id @Tc = 25°C	7	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	21	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	21	A
Continuous Source Current (Body diode), Is	7	A
Pulsed Source Current (Body diode), Ism	21	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRM234D

7A, 250V
RDS (on) = 0.70Ω



TO–204AA

Radiation-Hardened N-Channel Power MOSFETs

FRM234D rated to 10K rads (Si) total dose and 2E12 n; typical photocurrent 4.0nA per rad (Si)/sec transient dose

Features:

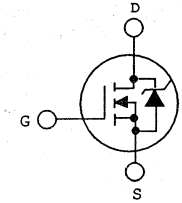
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



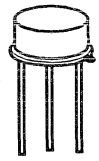
SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	7	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	21	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	21	A
Continuous Source Current (Body diode), Is	7	A
Pulsed Source Current (Body diode), Ism	21	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRL234D

4A, 250V
RDS (on) = 0.70Ω



JEDEC TO–205AF

Radiation–Hardened N–Channel Power MOSFETs

FRL234D rated to 10K rads (Si) total dose and 2E12 n; typical photocurrent 4.0nA per rad (Si)/sec transient dose

Features:

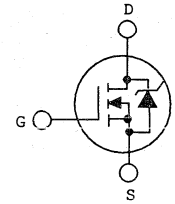
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

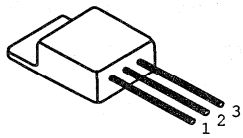
Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	4	A
@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}	12	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	12	A
Continuous Source Current (Body diode), Is	4	A
Pulsed Source Current (Body diode), Ism	12	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

FRS234D

5A, 250V
RDS (on) = 0.715Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-257AA

FRS234D rated to 10K rads (Si) total dose and 2E12 n; typical photocurrent 4.0nA per rad (Si)/sec transient dose

Features:

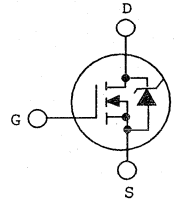
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

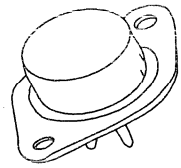
Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	5	A
@Tc = 100°C	3	A
Pulsed Drain Current, I_{DM}	15	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	15	A
Continuous Source Current (Body diode), Is	5	A
Pulsed Source Current (Body diode), Ism	15	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

PRELIMINARY

FRM430D

3A, 500V
RDS (on) = 2.50Ω



TO–204AA

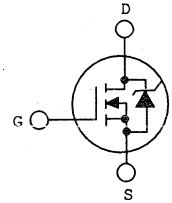
Radiation–Hardened N–Channel Power MOSFETs

FRM430D rated to 10K rads (Si) total dose and 2E12 n; typical photocurrent 8.0nA per rad (Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

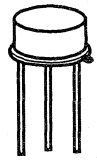
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	500	V
Continuous Drain Current, Id @Tc = 25°C	3	A
@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}	9	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	9	A
Continuous Source Current (Body diode), Is	3	A
Pulsed Source Current (Body diode), Ism	9	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

FRL430D

2A, 500V
RDS(on) = 2.50Ω



JEDEC TO–205AF

Radiation-Hardened N-Channel Power MOSFETs

FRL430D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 8.0nA per rad(Si)/sec transient dose

Features:

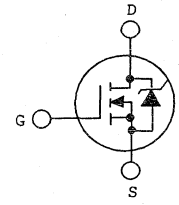
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	500	V
Continuous Drain Current, Id @Tc = 25°C	2	A
@Tc = 100°C	1	A
Pulsed Drain Current, I_{DM}	6	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	6	A
Continuous Source Current (Body diode), Is	2	A
Pulsed Source Current (Body diode), Ism	6	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

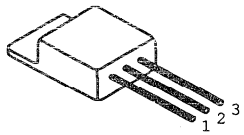
PRELIMINARY

FRS430D

3A, 500V

RDS(on) = 2.52Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-257AA

FRS430D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 8.0nA per rad(Si)/sec transient dose

Features:

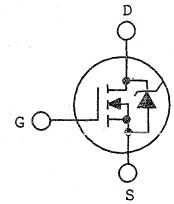
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



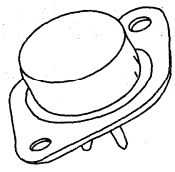
SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}		500	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)		500	V
Continuous Drain Current, Id	@Tc = 25°C	3	A
	@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}		9	A
Gate-Source Voltage, V_{GS}		±20	V
Power Dissipation, P_T:	At Tc = 25°C	50	W
	At Tc = 100°C	20	W
	Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)		9	A
Continuous Source Current (Body diode), Is		3	A
Pulsed Source Current (Body diode), Ism		9	A
Operating and Storage Temperature, Tjc, Tstg		−55 to +150	C°
Lead Temperature (During soldering): T_L			
	Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	C°

FRM140D

23A, 100V
RDS(on) = 0.13Ω



TO–204AA

Radiation-Hardened N-Channel Power MOSFETs

FRM140D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 3.0nA per rad(Si)/sec transient dose

Features:

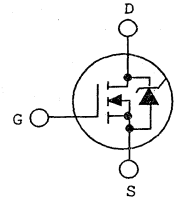
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
Continuous Drain Current, Id @Tc = 25°C	23	A
@Tc = 100°C	15	A
Pulsed Drain Current, I_{DM}	69	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	69	A
Continuous Source Current (Body diode), Is	23	A
Pulsed Source Current (Body diode), Ism	69	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

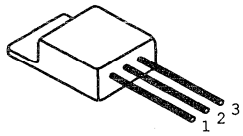
PRELIMINARY

FRS140D

17A, 100V

RDS(on) = 0.145Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-257AA

FRS140D rated to 10K rads(Si) and 2E12 n° typical photocurrent 3.0nA per rad(Si)/sec

Features:

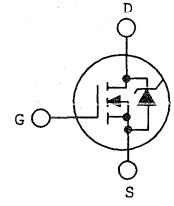
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



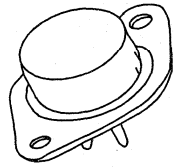
SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	100	V
Continuous Drain Current, Id @Tc = 25°C	17	A
@Tc = 100°C	11	A
Pulsed Drain Current, I_{DM}	51	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	51	A
Continuous Source Current (Body diode), Is	17	A
Pulsed Source Current (Body diode), Ism	51	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRM240D

16A, 200V
RDS(on) = 0.24Ω



TO–204AA

Radiation-Hardened N-Channel Power MOSFETs

FRM240D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 5.0nA per rad(Si)/sec transient dose

Features:

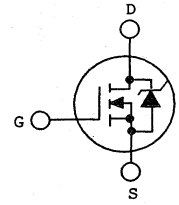
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
Continuous Drain Current, Id @Tc = 25°C	16	A
@Tc = 100°C	10	A
Pulsed Drain Current, I_{DM}	48	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	48	A
Continuous Source Current (Body diode), Is	16	A
Pulsed Source Current (Body diode), Ism	48	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

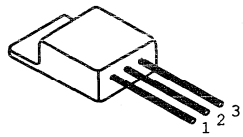
HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

PRELIMINARY

FRS240D

12A, 200V
RDS(on) = 0.255Ω



TO-257AA

Radiation-Hardened N-Channel Power MOSFETs

FRS240D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 5.0nA per rad(Si)/sec transient dose

Features:

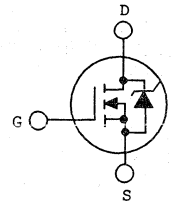
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



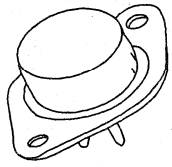
SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}		200	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)		200	V
Continuous Drain Current, Id	@Tc = 25°C	12	A
	@Tc = 100°C	7	A
Pulsed Drain Current, I_{DM}		36	A
Gate-Source Voltage, V_{GS}		±20	V
Power Dissipation, P_T:	At Tc = 25°C	75	W
	At Tc = 100°C	30	W
	Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)		36	A
Continuous Source Current (Body diode), Is		12	A
Pulsed Source Current (Body diode), Ism		36	A
Operating and Storage Temperature, Tjc, Tstg		−55 to +150	°C
Lead Temperature (During soldering): T_L			
	Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRM244D

12A, 250V
RDS(on) = 0.40Ω



TO–204AA

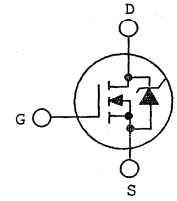
Radiation-Hardened N-Channel Power MOSFETs

FRM244D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 7.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	12	A
@Tc = 100°C	7	A
Pulsed Drain Current, I_{DM}	36	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	36	A
Continuous Source Current (Body diode), Is	12	A
Pulsed Source Current (Body diode), Ism	36	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

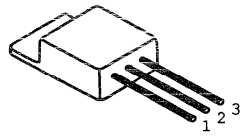
HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

PRELIMINARY

FRS244D

9A, 250V
RDS(on) = 0.415Ω

Radiation-Hardened N-Channel Power MOSFETs



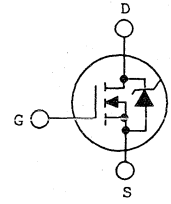
TO-257AA

FRS244D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 7.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

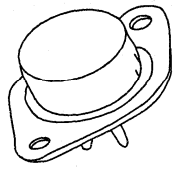
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	9	A
@Tc = 100°C	6	A
Pulsed Drain Current, I_{DM}	27	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	27	A
Continuous Source Current (Body diode), Is	9	A
Pulsed Source Current (Body diode), Ism	27	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

FRM440D

6A, 500V
RDS(on) = 1.40Ω



TO–204AA

Radiation-Hardened N-Channel Power MOSFETs

FRM440D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 12nA per rad(Si)/sec transient dose

Features:

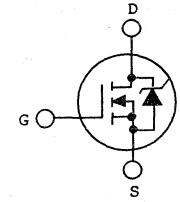
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

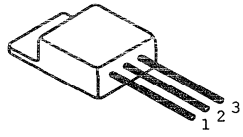
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	500	V
Continuous Drain Current, Id @Tc = 25°C	6	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	18	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	18	A
Continuous Source Current (Body diode), Is	6	A
Pulsed Source Current (Body diode), Ism	18	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

FRS440D

5A, 500V
RDS(on) = 1.42Ω



TO-257AA

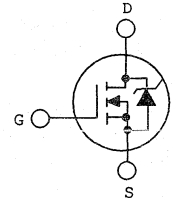
Radiation-Hardened N-Channel Power MOSFETs

FRS 440D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 7.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

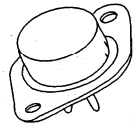
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	500	V
Continuous Drain Current, Id @Tc = 25°C	5	A
@Tc = 100°C	3	A
Pulsed Drain Current, I_{DM}	15	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	15	A
Continuous Source Current (Body diode), Is	5	A
Pulsed Source Current (Body diode), Ism	15	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	C°
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	C°

FRK150D

40A, 100V
RDS(on) = 0.055Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AE

FRK150D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 7.0nA per rad(Si)/sec transient dose

Features:

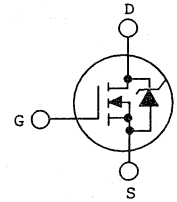
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

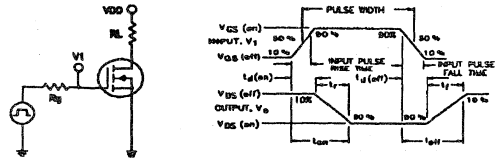
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
Continuous Drain Current, Id @Tc = 25°C	40	A
@Tc = 100°C	25	A
Pulsed Drain Current, I_{DM}	100	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	100	A
Continuous Source Current (Body diode), Is	40	A
Pulsed Source Current (Body diode), Ism	100	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

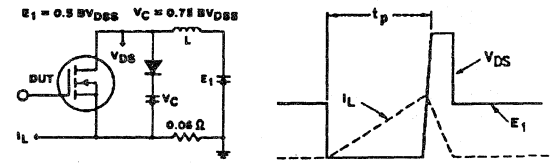
FRK150D
Pre and Post Radiation Electrical Characteristics

Gamma = 10KRAD (Si) Neutron = 2E12 n/cm2
Case Temperature (Tc) = 25°C unless otherwise specified

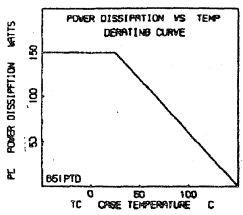
CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVdss	Vgs = 0, Id = 1mA	100	—	V
Gate-Threshold Volts	Vgs(th)	Vds = Vgs, Id = 1ma	2	4	V
Gate-Body Leakage Forward	Igssf	Vgs = +20V	—	100	nA
Gate-Body Leakage Reverse	Igssr	Vgs = −20V	—	100	nA
Zero-Gate Voltage Drain Current	Idss1 Idss2 Idss3	Vds = 100V, Vgs = 0 Vds = 80V, Vgs = 0 Vds = 80V, Vgs = 0, Tc = 125°C	— — —	1 .025 .25	mA
Rated Avalanche Current	Iar	Time = 20uS	—	100	A
Drain-Source On-State Volts	Vds(on)	Vgs = 10V, Id = 40A	—	2.32	V
Drain-Source On Resistance	Rds(on)	Vgs = 10V, Id = 25A	—	.055	Ω
Turn-On Delay Time	td(on)	Vdd = 50V, Id = 40A PULSE WIDTH = 3uS PERIOD = 300mS Rg = 25Ω 0 ≤ VGS ≤ 10 (SEE TEST CIRCUIT)	—	170	nS
Rise Time	tr		—	1120	
Turn-Off Delay Time	td(off)		—	420	
Fall Time	tf		—	380	
Gate-Charge Threshold	Qg(th)	Vdd = 50V, IGS1 = IGS2 Id = 40A 0 ≤ VGS ≤ 20 (SEE FIGURE)	3.5	15	nC
Gate-Charge Total	Qgm		140	560	
Gate-Charge On State	Qg(on)		58	230	
Diode Forward Voltage	Vsd	Id = 40A, Vgd = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 10A; di/dt = 100A/uS	—	1400	nS
Junction-To-Case	Rθjc	—	—	0.83	°C/W
Junction-to-Ambient	Rθja	Free Air Operation	—	30	

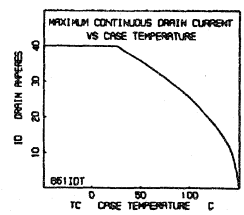


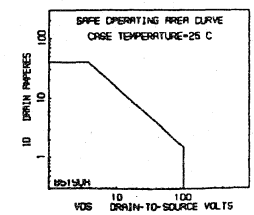
SWITCHING TIME TESTING



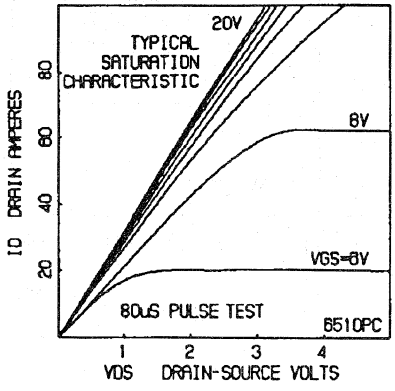
CLAMPED INDUCTIVE SWITCHING, ILM

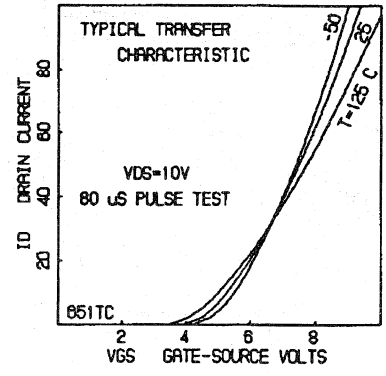


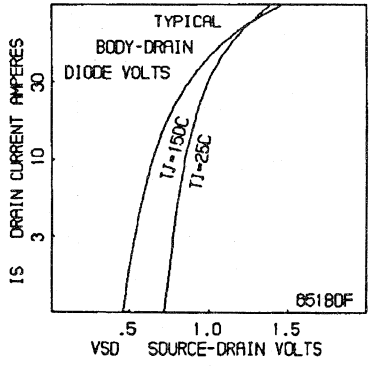


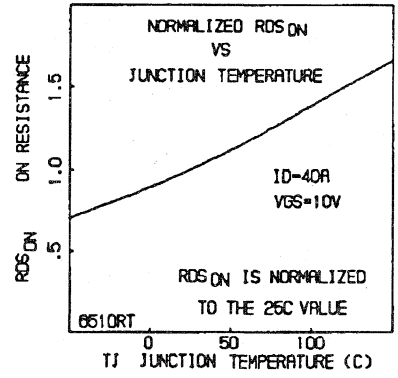


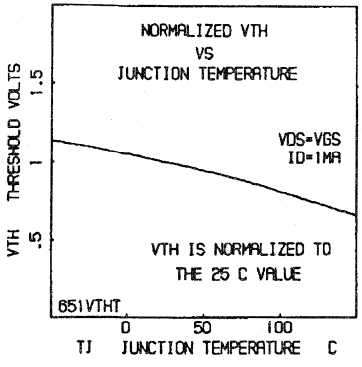
FRK150D
Typical Characteristics

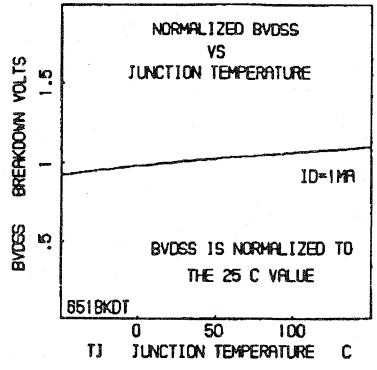




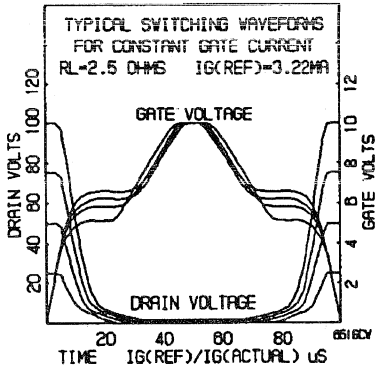


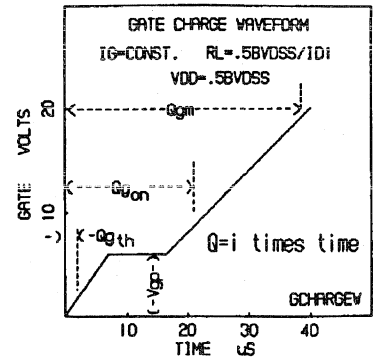


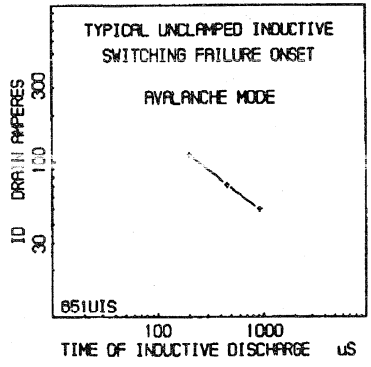


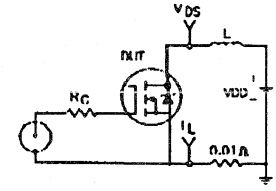


FRK150D
Typical Characteristics, Continued

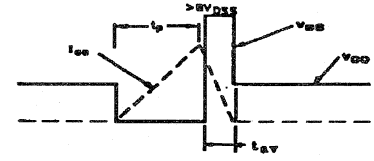


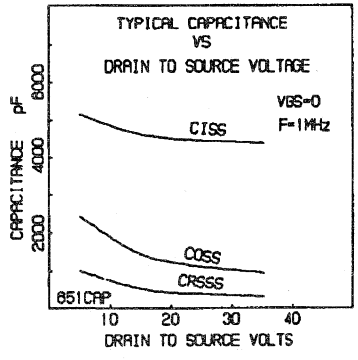


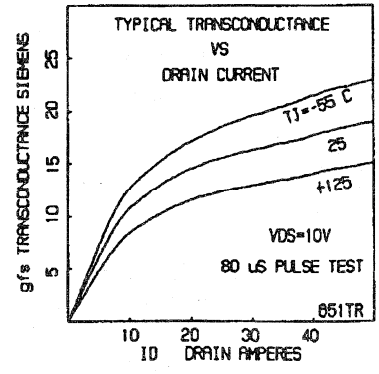




UNCLAMPED INDUCTIVE SWITCHING

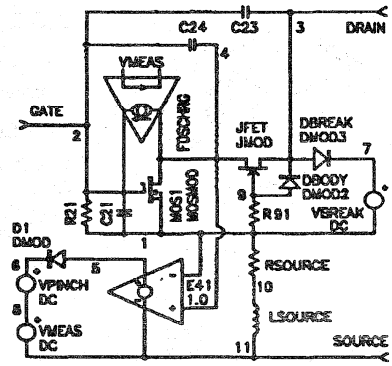






FRK150D
Spice Parameters and Sub Circuit

```
.SUBCKT FRK150D 3 2 11; REV 5/03/90
R21 2 1 1E9
R91 9 1 0.0001
C21 2 1 3900p
C23 2 3 350p
C24 2 4 8000p
FDSCHRG 4 2 VMEAS 1.0
MOS1 4 2 1 1 mosmod L = 1u   W = 1u
JFET 3 9 4 JMOD 1
DBODY 9 3 DMOD2
RSOURCE 1 10 .016
LSOURCE 10 11 7.5n
E41 5 11 4 1 1.0
D1 5 6 DMOD
VPINCH 6 8 DC 5.5
VMEAS 8 11 DC 0
DBREAK 3 7 DMOD3
VBREAK 7 1 DC 115
.MODEL MOSMOD NMOS VTO = 4   KP = 14   TOX = 1.OE+06U
.MODEL JMOD NJF VTO = 5.5   BETA = 1400   IS = 5.1E-18   RD = .0111
.MODEL DMOD D IS = 1.OE-13   N = 0.03   RS = .001
.MODEL DMOD2 D CJO = 8910P   TT = 700n   IS = 5.1E-12
.MODEL DMOD3 D IS = 1.OE-13   RS = .5   N = 1.0
.ENDS
```

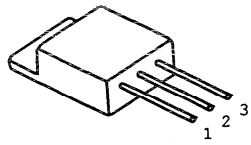


Verified on PSPICE

Reference: C.F. Wheatley, Jr. H.R. Ronan, Jr. G.M. Dolny, "Spicing-Up Spice II Software For Power MOSFET Modeling", Harris Application Note AN-8610, 4-87

FRF150D

25A, 100V
RDS(on)=0.07Ω



TO-254AA

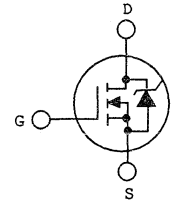
Radiation-Hardened N-Channel Power MOSFETs

FRF150D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 7.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

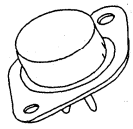
The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}		100	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)		100	V
Continuous Drain Current, Id	@Tc = 25°C	25	A
	@Tc = 100°C	20	A
Pulsed Drain Current, I_{DM}		75	A
Gate-Source Voltage, V_{GS}		±20	V
Power Dissipation, P_T:	At Tc = 25°C	125	W
	At Tc = 100°C	50	W
	Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)		75	A
Continuous Source Current (Body diode), Is		25	A
Pulsed Source Current (Body diode), Ism		75	A
Operating and Storage Temperature, Tjc, Tstg		−55 to +150	°C
Lead Temperature (During soldering): T_L			
	Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

Radiation-Hardened N-Channel Power MOSFETs



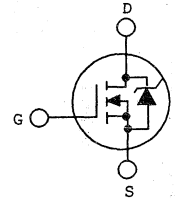
TO–204AE

FRK250D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 12nA per rad(Si)/sec transient

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

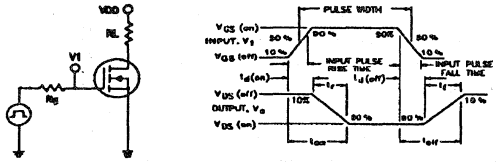
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
Continuous Drain Current, Id @Tc = 25°C	27	A
@Tc = 100°C	17	A
Pulsed Drain Current, I_{DM}	81	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	81	A
Continuous Source Current (Body diode), Is	27	A
Pulsed Source Current (Body diode), Ism	81	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

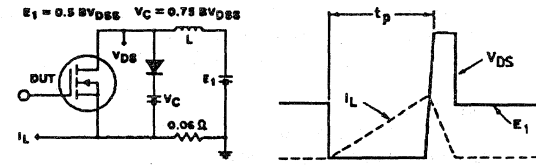
FRK250D
Pre and Post Radiation Electrical Characteristics

Gamma = 10KRAD (Si) Neutron = 2E12 n/cm2
Case Temperature (Tc) = 25°C unless otherwise specified

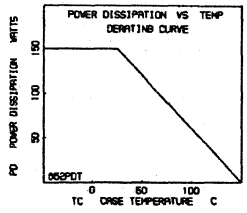
CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVdss	Vgs = 0, Id = 1mA	200	—	V
Gate-Threshold Volts	Vgs(th)	Vds = Vgs, Id = 1ma	2	4	V
Gate-Body Leakage Forward	Igssf	Vgs = +20V	—	100	nA
Gate-Body Leakage Reverse	Igssr	Vgs = −20V	—	100	nA
Zero-Gate Voltage Drain Current	Idss1 Idss2 Idss3	Vds = 200V, Vgs = 0 Vds = 160V, Vgs = 0 Vds = 160V, Vgs = 0, Tc = 125°C	— — —	1 .025 .25	mA
Rated Avalanche Current	Iar	Time = 20uS	—	81	A
Drain-Source On-State Volts	Vds(on)	Vgs = 10V, Id = 27A	—	2.7	V
Drain-Source On Resistance	Rds(on)	Vgs = 10V, Id = 17A	—	.100	Ω
Turn-On Delay Time	td(on)	Vdd = 100V, Id = 27A PULSE WIDTH = 3uS PERIOD = 300mS Rg = 25Ω 0 ≤ VGS ≤ 10 (SEE TEST CIRCUIT)	—	170	nS
Rise Time	tr		—	600	
Turn-Off Delay Time	td(off)		—	580	
Fall Time	tf		—	300	
Gate-Charge Threshold	Qg(th)	Vdd = 100V, IGS1 = IGS2 Id = 27A 0 ≤ VGS ≤ 20 (SEE FIGURE)	3.5	15	nC
Gate-Charge Total	Qgm		120	485	
Gate-Charge On State	Qg(on)		61	244	
Diode Forward Voltage	Vsd	Id = 27A, Vgd = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 10A; di/dt = 100A/uS	—	1700	nS
Junction-To-Case	Rθjc	—	—	0.83	°C/W
Junction-to-Ambient	Rθja	Free Air Operation	—	30	

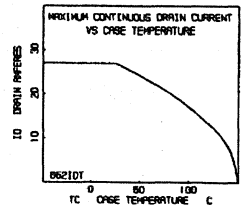


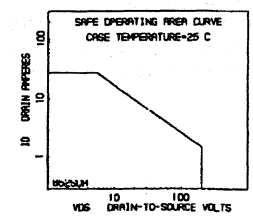
SWITCHING TIME TESTING



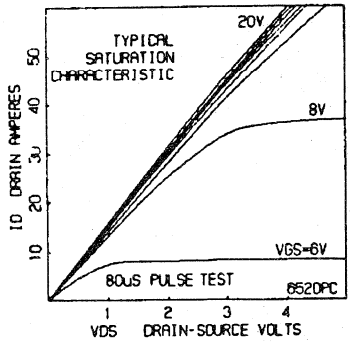
CLAMPED INDUCTIVE SWITCHING, ILM

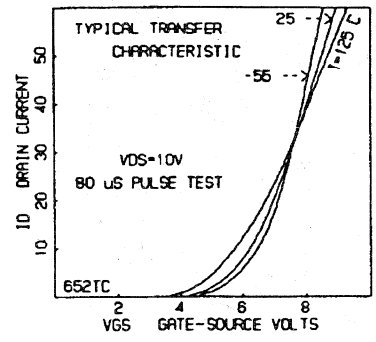


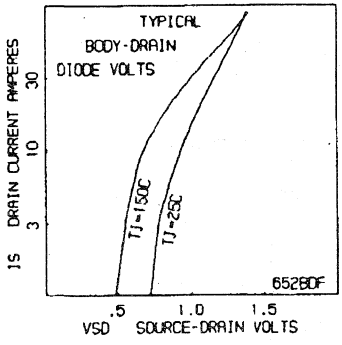


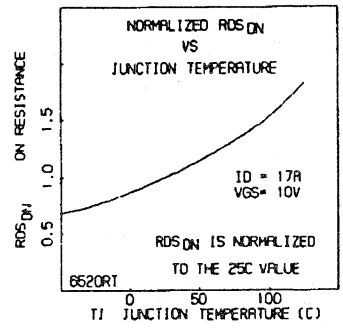


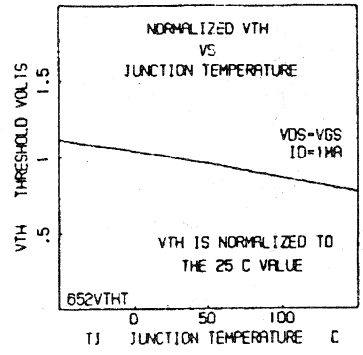
FRK250D
Typical Characteristics

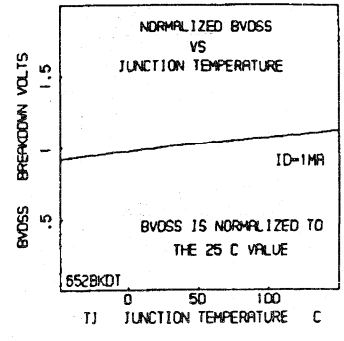




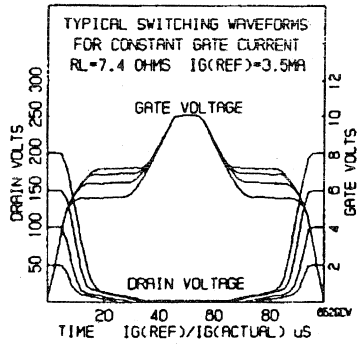


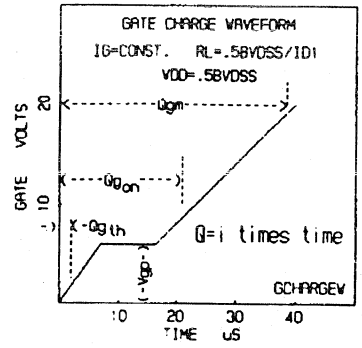


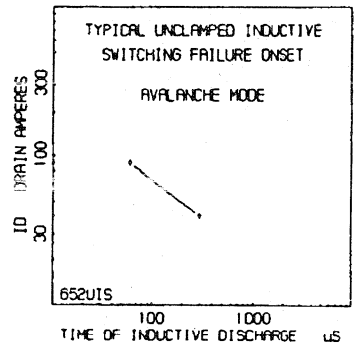


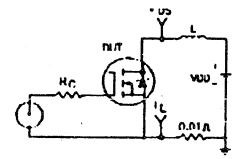


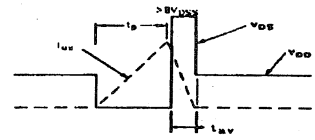
FRK250D
Typical Characteristics, Continued

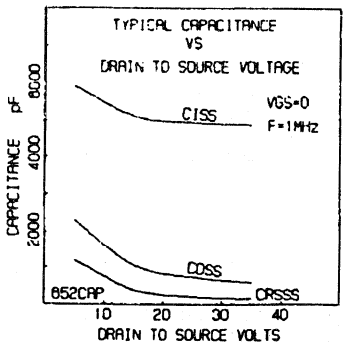


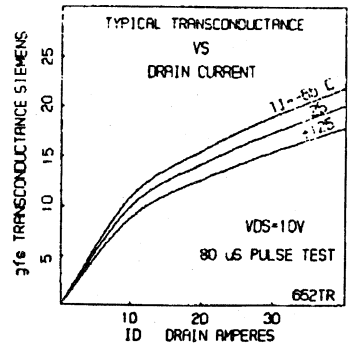






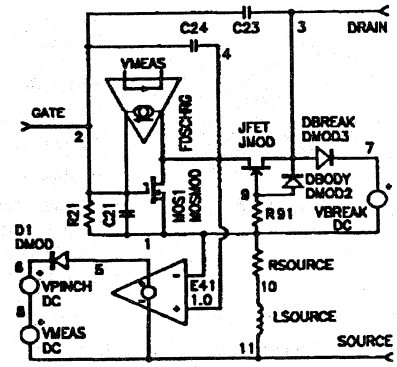






FRK250D
Spice Parameters and Sub Circuit

```
.SUBCKT FRK250 3 2 11; REV 6/15/90
R21 2 1 1E9
R91 9 1 0.00654
C21 2 1 4800p
C23 2 3 200p
C24 2 4 9400p
FDCHRG 4 2 VMEAS 1.0
MOS1 4 2 1 1 mosmod L = 1u   W = 1u
JFET 3 9 4 JMOD 1
DBODY 9 3 DMOD2
RSOURCE 1 10 0.01827
LSOURCE 10 11 7.500n
E41 5 11 4 1 1.0
D1 5 6 DMOD
VPINCH 6 8 DC 8.000
VMEAS 8 11 DC 0
DBREAK 3 7 DMOD3
VBREAK 7 1 DC 240.0
.MODEL MOSMOD NMOS VTO = 4.463   KP = 12.162   TOX = 1.OE+06U
.MODEL JMOD NJF VTO = 8.000   BETA = 1216.2   IS = 8.7E-019   RD = 0.05983
.MODEL DMOD D IS = 1.OE-13   N = 0.03   RS = .001
.MODEL DMOD2 D CJO = 4200p   TT = 1000n   IS = 8.7E-013
.MODEL DMOD3 D IS = 1.OE-13   RS = 1.111   N = 1.0
.ENDS
```



Verified on PSPICE

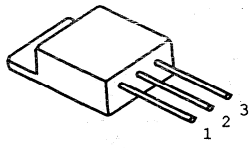
Reference: C.F. Wheatley, Jr., H.R. Ronan, Jr., G.M. Dolny, "Spicing-Up Spice II Software For Power MOSFET Modeling", Harris Application Note AN-8610, 4-87

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

PRELIMINARY

FRF250D

23A, 200V
RDS(on)=0.115Ω



TO-254AA

Radiation-Hardened N-Channel Power MOSFETs

FRF250D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 12nA per rad(Si)/sec transient dose

Features:

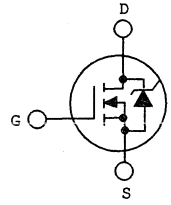
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
Continuous Drain Current, Id @Tc = 25°C	23	A
@Tc = 100°C	15	A
Pulsed Drain Current, I_{DM}	69	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	69	A
Continuous Source Current (Body diode), Is	23	A
Pulsed Source Current (Body diode), Ism	69	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRK254D

20A, 250V
RDS(on) = 0.17Ω

Radiation-Hardened N-Channel Power MOSFETs

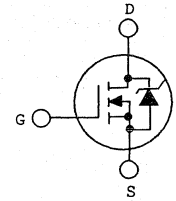
TO–204AE

FRK254D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 15nA per rad(Si)/sec transient dose.

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

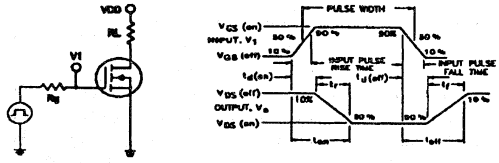
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	20	A
@Tc = 100°C	12	A
Pulsed Drain Current, I_{DM}	60	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	60	A
Continuous Source Current (Body diode), Is	20	A
Pulsed Source Current (Body diode), Ism	60	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

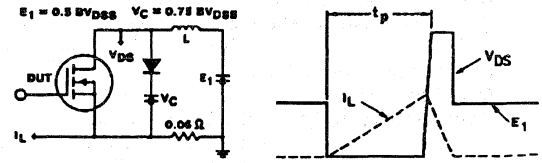
FRK254D
Pre and Post Radiation Electrical Characteristics

Gamma = 10KRAD (Si) Neutron = 2E12
Case Temperature (Tc) = 25°C unless otherwise specified

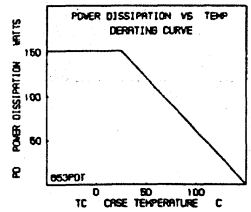
CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volt	BVdss	Vgs = 0, Id = 1mA	250	—	V
Gate-Threshold Volts	Vgs(th)	Vds = Vgs, Id = 1ma	2	4	V
Gate-Body Leakage Forward	Igssf	Vgs = +20V	—	100	nA
Gate-Body Leakage Reverse	Igssr	Vgs = −20V	—	100	nA
Zero-Gate Voltage Drain Current	Idss1 Idss2 Idss3	Vds = 250V, Vgs = 0 Vds = 200V, Vgs = 0 Vds = 200V, Vgs = 0, Tc = 125°C	— — —	1 .025 .25	mA
Rated Avalanche Current	Iar	Time = 20uS	—	60	A
Drain-Source On-State Volts	Vds(on)	Vgs = 10V, Id = 20A	—	3.58	V
Drain-Source On Resistance	Rds(on)	Vgs = 10V, Id = 12A	—	.17	Ω
Turn-On Delay Time	td(on)	Vdd = 125V, Id = 20A PULSE WIDTH = 3uS PERIOD = 300mS Rg = 25Ω 0 ≤ VGS ≤ 10 (SEE TEST CIRCUIT)	—	150	nS
Rise Time	tr		—	450	
Turn-Off Delay Time	td(off)		—	650	
Fall Time	tf		—	260	
Gate-Charge Threshold	Qg(th)	Vdd = 125V, IGS1 = IGS2 Id = 20A 0 ≤ VGS ≤ 20 (SEE FIGURE)	3.5	15	nC
Gate-Charge Total	Qgm		127	510	
Gate-Charge On State	Qg(on)		63	252	
Diode Forward Voltage	Vsd	Id = 20A, Vgd = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 10A; di/dt = 100A/uS	—	2000	nS
Junction-To-Case	Rθjc	—	—	0.83	°C/W
Junction-to-Ambient	Rθja	Free Air Operation	—	30	

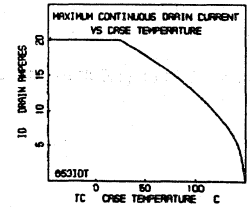


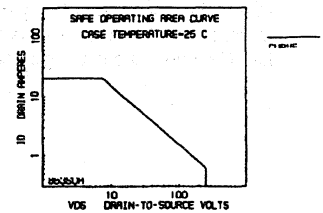
SWITCHING TIME TESTING



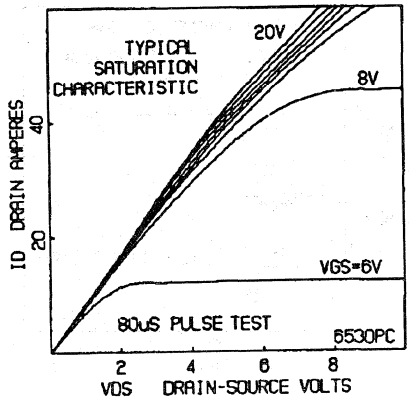
CLAMPED INDUCTIVE SWITCHING, ILM

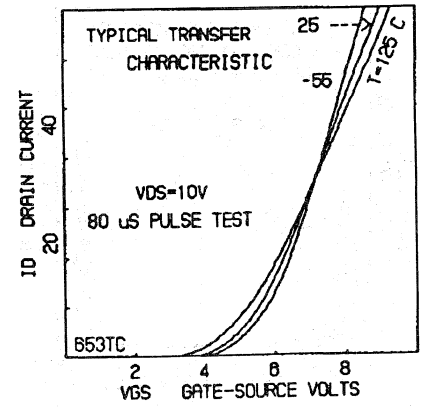


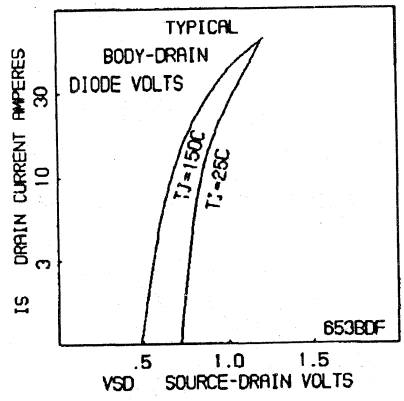


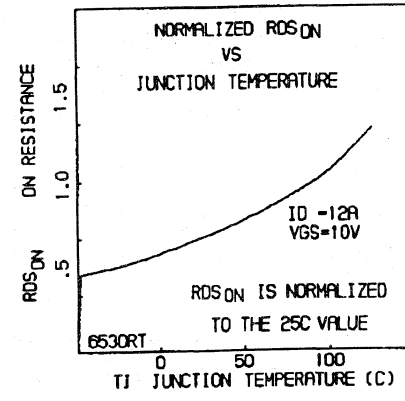


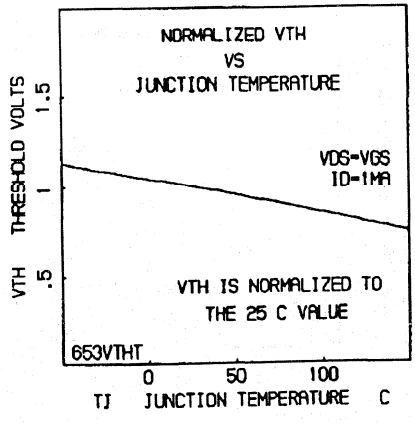
FRK254D
Typical Characteristics

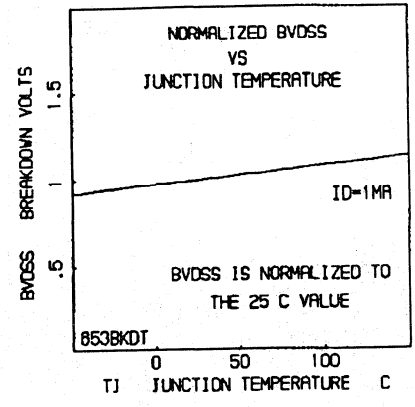




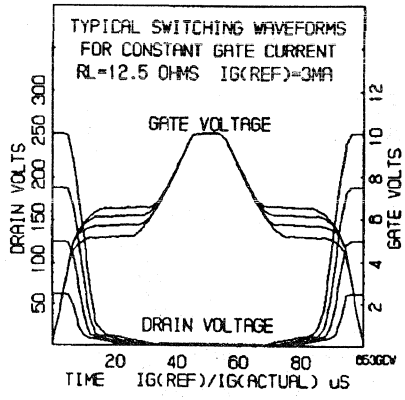


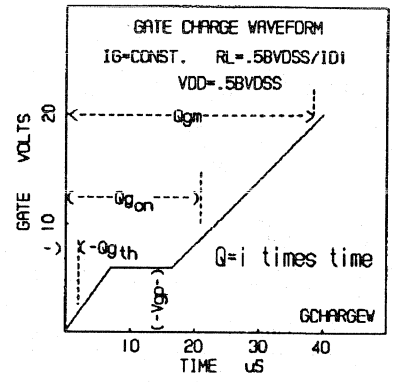


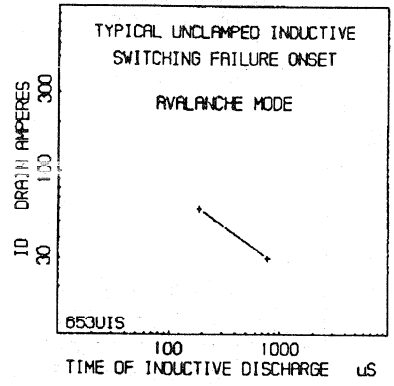


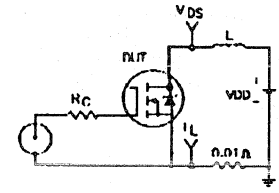


FRK254D
Typical Characteristics, Continued

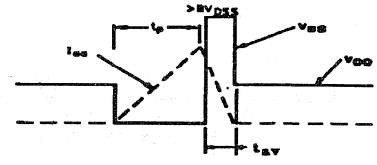


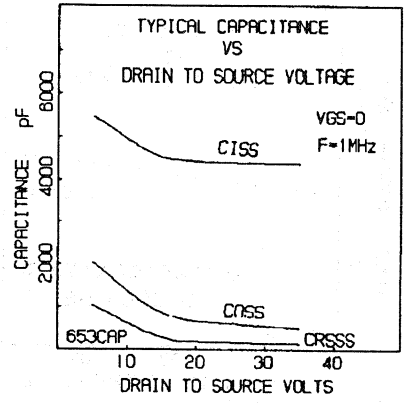


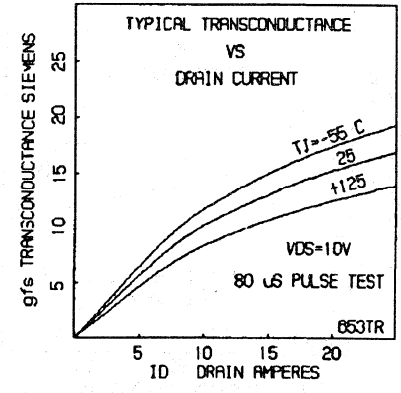




UNCLAMPED INDUCTIVE SWITCHING

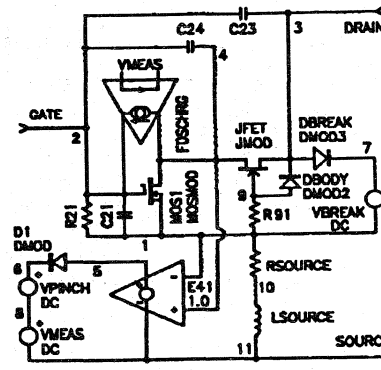






FRK254D
Spice Parameters and Sub Circuit

```
.SUBCKT FRK254D 3 2 11; REV 5/09/90
R21 2 1 1e9
R91 9 1 .00125
C21 2 1 4100p
C23 2 3 50p
C24 2 4 7000p
FDSCHRG 4 2 VMEAS 1.0
MOS1 4 2 1 1 mosmod L = 1u   W = 1u
JFET 3 9 4 JMOD 1
DBODY 9 3 DMOD2
RSOURCE 1 10 .01
LSOURCE 10 11 7.5n
E41 5 11 4 1 1.0
D1 5 6 DMOD
VPINCH 6 8 DC 7.5
VMEAS 8 11 DC 0
DBREAK 3 7 DMOD3
VBREAK 7 1 DC 280
.MODEL MOSMOD NMOS VTO = 3.75   KP = 7.346   TOX = 1.OE+06U
.MODEL JMOD NJF VTO = 7.5   BETA = 734.6   IS = 1.2E-18   RD = .1241
.MODEL DMOD D IS = 1.OE-13   N = 0.03   RS = .001
.MODEL DMOD2 D CJO = 3600p   TT = 1500n   IS = 1.2E-12
.MODEL DMOD3 D IS = 1.OE-13   RS = 1   N = 1.0
.ENDS
```



Verified on PSPICE

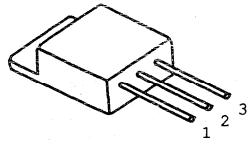
Reference: C.F. Wheatley, Jr., H.R. Ronan, Jr., G.M. Dolny, "Spicing-Up Spice II Software For Power MOSFET Modeling", Harris Application Note AN-8610, 4-87

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

FRF254D

17A, 250V
RDS(on)=0.185Ω



TO-254AA

Radiation-Hardened N-Channel Power MOSFETs

FRF254D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 15nA per rad(Si)/sec transient dose

Features:

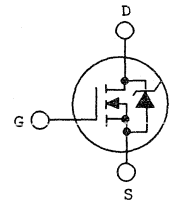
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

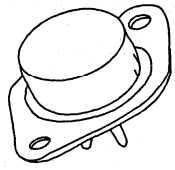
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	17	A
@Tc = 100°C	11	A
Pulsed Drain Current, I_{DM}	51	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	51	A
Continuous Source Current (Body diode), Is	17	A
Pulsed Source Current (Body diode), Ism	51	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

FRM450D

10A, 500V
RDS(on)=0.60Ω



TO–204AA

Radiation-Hardened N-Channel Power MOSFETs

FRM450D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 30nA per rad(Si)/sec transient dose

Features:

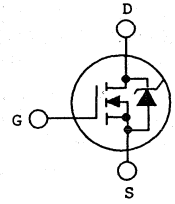
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

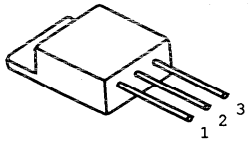
Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	500	V
Continuous Drain Current, Id @Tc = 25°C	10	A
@Tc = 100°C	6	A
Pulsed Drain Current, I_{DM}	30	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	30	A
Continuous Source Current (Body diode), Is	10	A
Pulsed Source Current (Body diode), Ism	30	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

PRELIMINARY

FRF450D

9A, 500V
RDS(on)=0.615Ω



TO-254AA

Radiation-Hardened N-Channel Power MOSFETs

FRF450D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 30nA per rad(Si)/sec transient dose

Features:

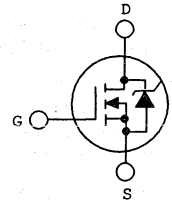
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

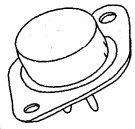
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	500	V
Continuous Drain Current, Id @Tc = 25°C	9	A
@Tc = 100°C	6	A
Pulsed Drain Current, I_{DM}	27	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	27	A
Continuous Source Current (Body diode), Is	9	A
Pulsed Source Current (Body diode), Ism	27	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRK160D

66A, 100V
RDS(on)=0.04Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AE

FRK160D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 10nA per rad(Si)/sec transient dose

Features:

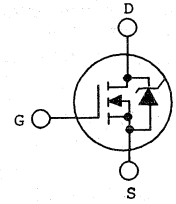
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
Continuous Drain Current, Id @Tc = 25°C	66	A
@Tc = 100°C	42	A
Pulsed Drain Current, I_{DM}	100	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	100	A
Continuous Source Current (Body diode), Is	66	A
Pulsed Source Current (Body diode), Ism	100	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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FRK260D

46A, 200V

RDS(on)=0.07Ω

Radiation-Hardened N-Channel Power MOSFETs

TO–204AE

FRK260D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 18nA per rad(Si)/sec transient dose

Features:

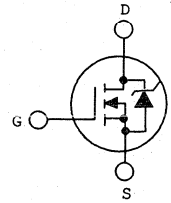
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

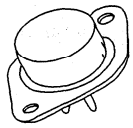
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
Continuous Drain Current, Id @Tc = 25°C	46	A
@Tc = 100°C	29	A
Pulsed Drain Current, I_{DM}	100	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	100	A
Continuous Source Current (Body diode), Is	46	A
Pulsed Source Current (Body diode), Ism	100	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRK264D

34A, 250V
RDS(on)=0.12Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AE

FRK264D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 22nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

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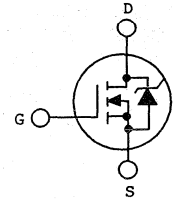


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

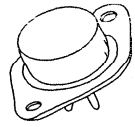
Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	34	A
@Tc = 100°C	21	A
Pulsed Drain Current, I_{DM}	100	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	100	A
Continuous Source Current (Body diode), Is	34	A
Pulsed Source Current (Body diode), Ism	100	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

FRK460D

17A, 500V
RDS(on)=0.40Ω

Radiation-Hardened N-Channel Power MOSFETs



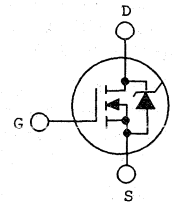
TO–204AE

FRK460D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 45nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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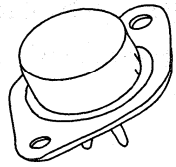
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	500	V
Continuous Drain Current, Id @Tc = 25°C	17	A
@Tc = 100°C	11	A
Pulsed Drain Current, I_{DM}	51	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	51	A
Continuous Source Current (Body diode), Is	17	A
Pulsed Source Current (Body diode), Ism	51	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRM9130D

6A, –100V
RDS(on)=0.55Ω



TO–204AA

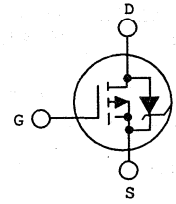
Radiation-Hardened P-Channel Power MOSFETs

FRM9130D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 1.5nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

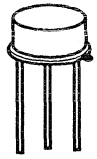
Drain-Source Voltage, V_{DS}	–100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–100	V
Continuous Drain Current, Id @Tc = 25°C	6	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	18	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	18	A
Continuous Source Current (Body diode), Is	6	A
Pulsed Source Current (Body diode), Ism	18	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

FRL9130D

5A, −100V
RDS(on)=0.55Ω



JEDEC TO–205AF

Radiation-Hardened P-Channel Power MOSFETs

FRL9130D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 1.5nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

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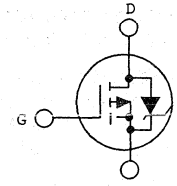

SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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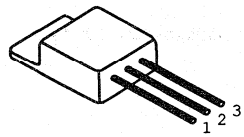
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	−100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	−100	V
Continuous Drain Current, Id @Tc = 25°C	5	A
@Tc = 100°C	3	A
Pulsed Drain Current, I_{DM}	15	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	15	A
Continuous Source Current (Body diode), Is	5	A
Pulsed Source Current (Body diode), Ism	15	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

FRS9130D

6A, −100V
RDS(on)=0.565Ω



TO-257AA

Radiation-Hardened P-Channel Power MOSFETs

FRS9130D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 1.5nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

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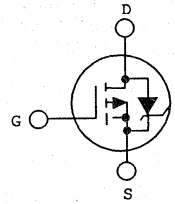


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	−100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	−100	V
Continuous Drain Current, Id @Tc = 25°C	6	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	18	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	18	A
Continuous Source Current (Body diode), Is	6	A
Pulsed Source Current (Body diode), Ism	18	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

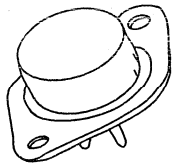
HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

FRM9230D

4A, –200V

RDS(on)=1.30Ω



TO–204AA

Radiation-Hardened P-Channel Power MOSFETs

FRM9230D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 3.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

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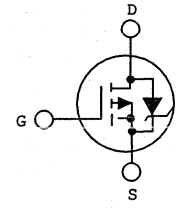


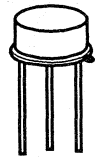
SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
Continuous Drain Current, Id @Tc = 25°C	4	A
@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}	12	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	12	A
Continuous Source Current (Body diode), Is	4	A
Pulsed Source Current (Body diode), Ism	12	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRL9230D

3A, –200V
RDS(on)=1.30Ω



JEDEC TO–205AF

Radiation-Hardened P-Channel Power MOSFETs

FRL9230D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 3.0nA per rad(Si)/sec transient dose

Features:

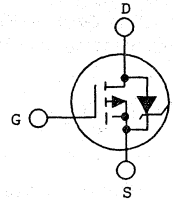
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

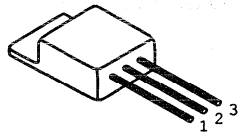
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
Continuous Drain Current, Id @Tc = 25°C	3	A
@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}	9	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	9	A
Continuous Source Current (Body diode), Is	3	A
Pulsed Source Current (Body diode), Ism	9	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

FRS9230D

4A, –200V
RDS(on)=1.32Ω



TO-257AA

Radiation-Hardened P-Channel Power MOSFETs

FRS9230D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 3.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

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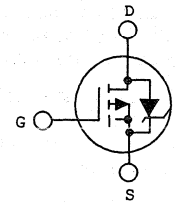


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

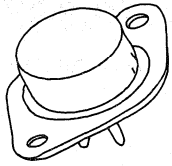
Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
Continuous Drain Current, Id @Tc = 25°C	4	A
@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}	12	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	12	A
Continuous Source Current (Body diode), Is	4	A
Pulsed Source Current (Body diode), Ism	12	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

OBJECTIVE

FRM9430D

1.5A, –500V
RDS(on)=7.60Ω

This Objective Data Sheet Represents the Proposed Device Performance.



TO–204AA

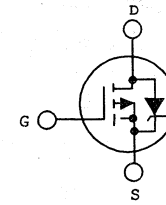
Radiation-Hardened P-Channel Power MOSFETs

FRM9430D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 8.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	–500	V
Continuous Drain Current, Id @Tc = 25°C	1.5	A
@Tc = 100°C	1	A
Pulsed Drain Current, I_{DM}	4.5	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	4.5	A
Continuous Source Current (Body diode), Is	1.5	A
Pulsed Source Current (Body diode), Ism	4.5	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
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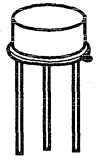
OBJECTIVE

FRL9430D

1A, –500V
RDS(on)=7.60Ω

This Objective Data Sheet Represents the Proposed Device Performance.



JEDEC TO–205AF

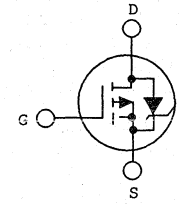
Radiation-Hardened P-Channel Power MOSFETs

FRL9430D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 8.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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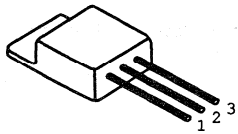
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	–500	V
Continuous Drain Current, Id @Tc = 25°C	1	A
@Tc = 100°C	0.5	A
Pulsed Drain Current, I_{DM}	3	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	3	A
Continuous Source Current (Body diode), Is	1	A
Pulsed Source Current (Body diode), Ism	3	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C



TO-257AA

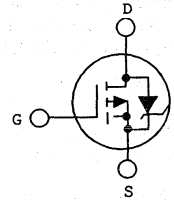
Radiation-Hardened P-Channel Power MOSFETs

FRS9430D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 8.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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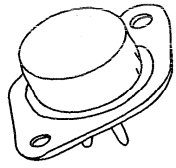
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	−500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	−500	V
Continuous Drain Current, Id @Tc = 25°C	1.5	A
@Tc = 100°C	1	A
Pulsed Drain Current, I_{DM}	4.5	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	4.5	A
Continuous Source Current (Body diode), Is	1.5	A
Pulsed Source Current (Body diode), Ism	4.5	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRM9140D

11A, −100V
RDS(on)=0.30Ω



TO–204AA

Radiation-Hardened P-Channel Power MOSFETs

FRM9140D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 3.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

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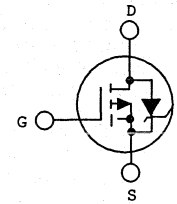

SYMBOL

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

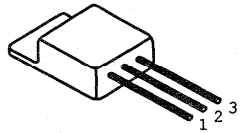
Drain-Source Voltage, V_{DS}	−100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	−100	V
Continuous Drain Current, Id @Tc = 25°C	11	A
@Tc = 100°C	7	A
Pulsed Drain Current, I_{DM}	33	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	33	A
Continuous Source Current (Body diode), Is	11	A
Pulsed Source Current (Body diode), Ism	33	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

FRS9140D

11A, –100V
RDS(on)=0.315Ω

Radiation-Hardened P-Channel Power MOSFETs



TO-257AA

FRS9140D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 3.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
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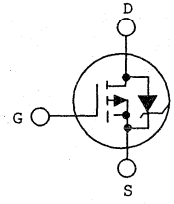


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–100	V
Continuous Drain Current, Id @Tc = 25°C	11	A
@Tc = 100°C	7	A
Pulsed Drain Current, I_{DM}	33	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	33	A
Continuous Source Current (Body diode), Is	11	A
Pulsed Source Current (Body diode), Ism	33	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

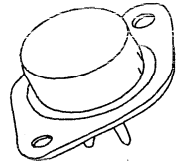
HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

FRM9240D

7A, –200V

RDS(on)=0.72Ω



TO–204AA

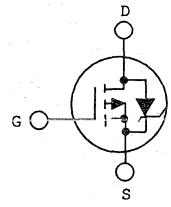
Radiation-Hardened P-Channel Power MOSFETs

FRM9240D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 5.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

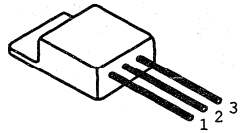
Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
Continuous Drain Current, Id @Tc = 25°C	7	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	21	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	21	A
Continuous Source Current (Body diode), Is	7	A
Pulsed Source Current (Body diode), Ism	21	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

FRS9240D

7A, –200V
RDS(on)=7.35Ω

Radiation-Hardened P-Channel Power MOSFETs



TO-257AA

FRS9240D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 5.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

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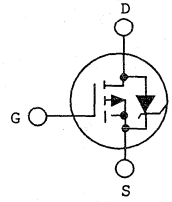


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
Continuous Drain Current, Id @Tc = 25°C	7	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	21	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	21	A
Continuous Source Current (Body diode), Is	7	A
Pulsed Source Current (Body diode), Ism	21	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

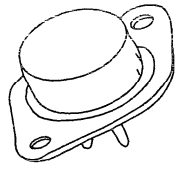
OBJECTIVE

FRM9440D

2.5A, –500V

RDS(on)=4.20Ω

This Objective Data Sheet Represents the Proposed Device Performance.



TO–204AA

Radiation-Hardened P-Channel Power MOSFETs

FRM9440D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 12nA per rad(Si)/sec transient dose

Features:

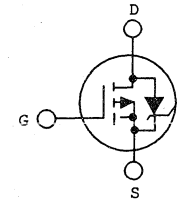
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

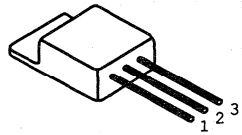
Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
Continuous Drain Current, Id @Tc = 25°C	2.5	A
@Tc = 100°C	1.5	A
Pulsed Drain Current, I_{DM}	7.5	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	7.5	A
Continuous Source Current (Body diode), Is	2.5	A
Pulsed Source Current (Body diode), Ism	7.5	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

OBJECTIVE

FRS9440D

2.5A, −500V
RDS(on)=4.22Ω

This Objective Data Sheet Represents the Proposed Device Performance.



TO-257AA

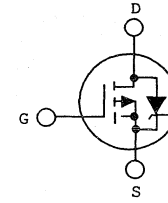
Radiation-Hardened P-Channel Power MOSFETs

FRS9440D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 12nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

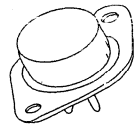
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	−500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	−500	V
Continuous Drain Current, Id @Tc = 25°C	2.5	A
@Tc = 100°C	1.5	A
Pulsed Drain Current, I_{DM}	7.5	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	7.5	A
Continuous Source Current (Body diode), Is	2.5	A
Pulsed Source Current (Body diode), Ism	7.5	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRK9150D

26A, −100V
RDS(on)=0.125Ω

Radiation-Hardened P-Channel Power MOSFETs



TO–204AE

FRK9150D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 7.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

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This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

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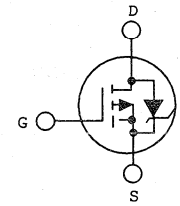


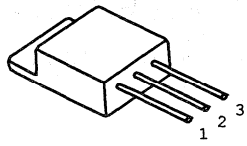
SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	−100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	−100	V
Continuous Drain Current, Id @Tc = 25°C	26	A
@Tc = 100°C	17	A
Pulsed Drain Current, I_{DM}	78	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	78	A
Continuous Source Current (Body diode), Is	26	A
Pulsed Source Current (Body diode), Ism	78	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRF9150D

23A, –100V
RDS(on)=0.14Ω



TO-254AA

Radiation-Hardened P-Channel Power MOSFETs

FRF9150D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 7.0nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

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This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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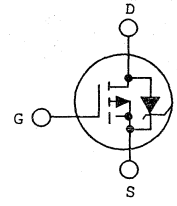


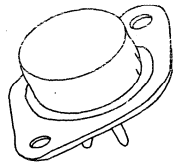
SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–100	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	–100	V
Continuous Drain Current, Id @Tc = 25°C	23	A
@Tc = 100°C	15	A
Pulsed Drain Current, I_{DM}	69	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	69	A
Continuous Source Current (Body diode), Is	23	A
Pulsed Source Current (Body diode), Ism	69	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRM9250D

16A, –200V
RDS(on)=0.30Ω



TO–204AA

Radiation-Hardened P-Channel Power MOSFETs

FRM9250D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 12nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

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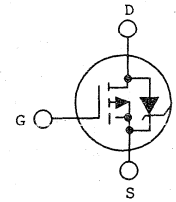


SYMBOL

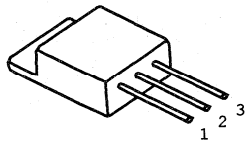
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	–200	V
Continuous Drain Current, Id @Tc = 25°C	16	A
@Tc = 100°C	10	A
Pulsed Drain Current, I_{DM}	48	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	48	A
Continuous Source Current (Body diode), Is	16	A
Pulsed Source Current (Body diode), Ism	48	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRF9250D

14A, –200V
RDS(on)=0.315Ω

Radiation-Hardened P-Channel Power MOSFETs



TO-254AA

FRF9250D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 12nA per rad(Si)/sec transient dose

Features:

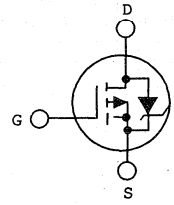
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
Continuous Drain Current, Id @Tc = 25°C	14	A
@Tc = 100°C	9	A
Pulsed Drain Current, I_{DM}	42	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	42	A
Continuous Source Current (Body diode), Is	14	A
Pulsed Source Current (Body diode), Ism	42	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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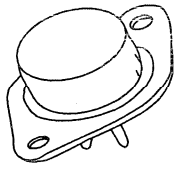
OBJECTIVE

FRM9450D

6A, –500V

RDS(on)=1.80Ω

This Objective Data Sheet Represents the Proposed Device Performance.



TO–204AA

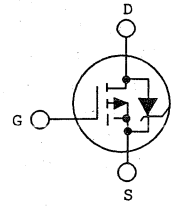
Radiation-Hardened P-Channel Power MOSFETs

FRM9450D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 30nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

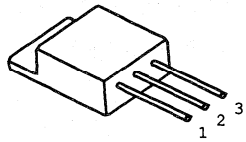
Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
Continuous Drain Current, Id @Tc = 25°C	6	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	18	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	18	A
Continuous Source Current (Body diode), Is	6	A
Pulsed Source Current (Body diode), Ism	18	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

OBJECTIVE

FRF9450D

5A, –500V
RDS(on)=1.82Ω

This Objective Data Sheet Represents the Proposed Device Performance.



TO-254AA

Radiation-Hardened P-Channel Power MOSFETs

FRF9450D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 30nA per rad(Si)/sec transient dose

Features:

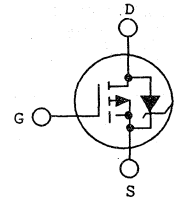
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
Continuous Drain Current, Id @Tc = 25°C	5	A
@Tc = 100°C	3	A
Pulsed Drain Current, I_{DM}	15	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	15	A
Continuous Source Current (Body diode), Is	5	A
Pulsed Source Current (Body diode), Ism	15	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

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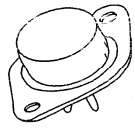
FRK9160D

40A, −100V
RDS(on)=0.085Ω

Radiation-Hardened P-Channel Power MOSFETs



TO–204AE

FRK9160D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 10nA per rad(Si)/sec transient dose

Features:

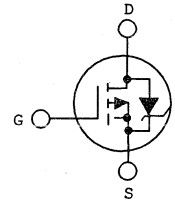
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	−100	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	−100	V
Continuous Drain Current, Id @Tc = 25°C	40	A
@Tc = 100°C	26	A
Pulsed Drain Current, I_{DM}	100	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	100	A
Continuous Source Current (Body diode), Is	40	A
Pulsed Source Current (Body diode), Ism	100	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

FRK9260D

26A, –200V
RDS(on)=0.20Ω

Radiation-Hardened P-Channel Power MOSFETs

TO–204AE

FRK9260D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 18nA per rad(Si)/sec transient dose

Features:

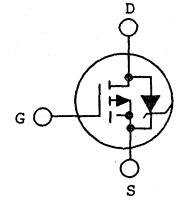
- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	–200	V
Continuous Drain Current, Id @Tc = 25°C	26	A
@Tc = 100°C	17	A
Pulsed Drain Current, I_{DM}	78	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	78	A
Continuous Source Current (Body diode), Is	26	A
Pulsed Source Current (Body diode), Ism	78	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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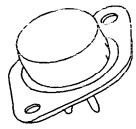
OBJECTIVE

FRK9460D

10A, –500V

RDS(on)=1.20Ω

This Objective Data Sheet Represents the Proposed Device Performance.



TO–204AE

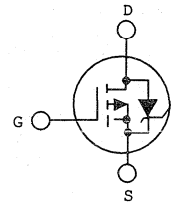
Radiation-Hardened P-Channel Power MOSFET

FRK9460D rated to 10K rads(Si) total dose and 2E12 n; typical photocurrent 45nA per rad(Si)/sec transient dose

Features:

- Designed, processed and tested for Tactical rad hard uses
- Special processing results in identical pre and post rad specs
- Ruggedized and 100% tested to enhance dose rate survival
- Ruggedized and 100% tested to enhance SEU survival
- Majority carrier device

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users with the vendor assuring a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and tested for SECOND GENERATION hardened power MOSFET's. Pre radiation specifications are met after exposure to 10 KRAD(Si) total dose and/or a neutron fluence of 2E12 n/cm2.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
Continuous Drain Current, Id @Tc = 25°C	10	A
@Tc = 100°C	6	A
Pulsed Drain Current, I_{DM}	30	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	30	A
Continuous Source Current (Body diode), Is	10	A
Pulsed Source Current (Body diode), Ism	30	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
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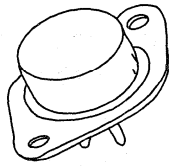
2N7271R, 2N7271H

REGISTRATION PENDING
Available As FRM130R, FRM130H
14A, 100V
RDS(on)=0.18Ω



TO–204AA

Radiation-Hardened N-Channel Power MOSFETs

Features:

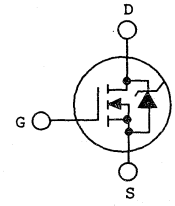
- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35 MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	100	V
Continuous Drain Current, Id @Tc = 25°C	14	A
@Tc = 100°C	9	A
Pulsed Drain Current, I_{DM}	42	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	42	A
Continuous Source Current (Body diode), Is	14	A
Pulsed Source Current (Body diode), Ism	42	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

2N7272R, 2N7272H

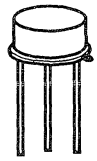
REGISTRATION PENDING

Available As FRL130R, FRL130H

8A, 100V

RDS(on)=0.18Ω

Radiation-Hardened N-Channel Power MOSFETs



JEDEC TO–205AF

Features:

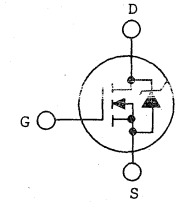
- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35 MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

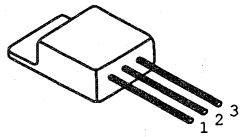
Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
Continuous Drain Current, Id @Tc = 25°C	8	A
@Tc = 100°C	5	A
Pulsed Drain Current, I_{DM}	24	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	24	A
Continuous Source Current (Body diode), Is	8	A
Pulsed Source Current (Body diode), Ism	24	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

2N7273R, 2N7273H

REGISTRATION PENDING
Available As FRS130R, FRS130H
12A, 100V
RDS(on)=0.195Ω

Radiation-Hardened N-Channel Power MOSFETs

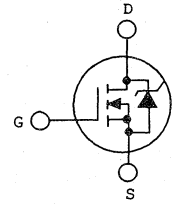


TO-257AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35 MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
Continuous Drain Current, Id @Tc = 25°C	12	A
@Tc = 100°C	7	A
Pulsed Drain Current, I_{DM}	36	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	36	A
Continuous Source Current (Body diode), Is	12	A
Pulsed Source Current (Body diode), Ism	36	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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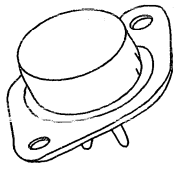
2N7274R, 2N7274H

REGISTRATION PENDING

Available As FRM230R, FRM230H

8A, 200V

RDS(on)=0.50Ω



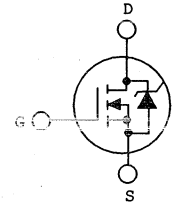
TO–204AA

Radiation-Hardened N-Channel Power MOSFETs

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35 MeV/mg/cm2 and a range ≥ 30 µm at 80% BVDSS

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
Continuous Drain Current, Id @Tc = 25°C	8	A
@Tc = 100°C	5	A
Pulsed Drain Current, I_{DM}	24	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	24	A
Continuous Source Current (Body diode), Is	8	A
Pulsed Source Current (Body diode), Ism	24	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

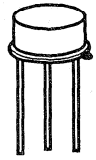
2N7275R, 2N7275H

REGISTRATION PENDING

Available As FRL230R, FRL230H

5A, 200V

RDS(on)=0.50Ω



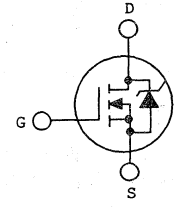
JEDEC TO–205AF

Radiation-Hardened N-Channel Power MOSFETs

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35 MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
Continuous Drain Current, Id @Tc = 25°C	5	A
@Tc = 100°C	3	A
Pulsed Drain Current, I_{DM}	15	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	15	A
Continuous Source Current (Body diode), Is	5	A
Pulsed Source Current (Body diode), Ism	15	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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PRELIMINARY

2N7276R, 2N7276H

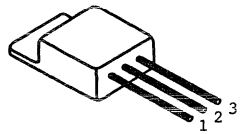
REGISTRATION PENDING

Available As FRS230R, FRS230H

7A, 200V

RDS(on)=0.515Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-257AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35 MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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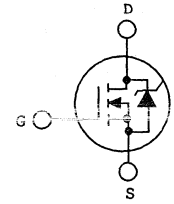


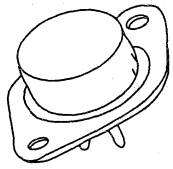
SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	200	V
Continuous Drain Current, Id @Tc = 25°C	7	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	21	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	21	A
Continuous Source Current (Body diode), Is	7	A
Pulsed Source Current (Body diode), Ism	21	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7277R, 2N7277H

REGISTRATION PENDING
Available As FRM234R, FRM234H
7A, 250V
RDS(on)=0.70Ω



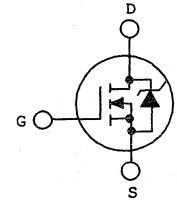
TO–204AA

Radiation-Hardened N-Channel Power MOSFETs

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35 MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	7	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	21	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	21	A
Continuous Source Current (Body diode), Is	7	A
Pulsed Source Current (Body diode), Ism	21	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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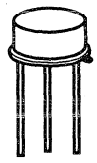
2N7278R, 2N7278H

REGISTRATION PENDING

Available As FRL234R, FRL234H

4A, 250V

RDS(on)=0.70Ω



JEDEC TO–205AF

Radiation-Hardened N-Channel Power MOSFETs

Features:

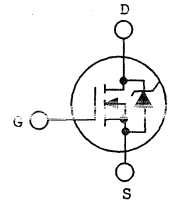
- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35 MeV/mg/cm2 and a range ≥ 30 µm at 80% BVDSS

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

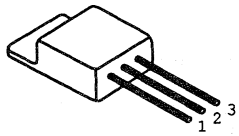
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	4	A
@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}	12	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	12	A
Continuous Source Current (Body diode), Is	4	A
Pulsed Source Current (Body diode), Ism	12	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

2N7279R, 2N7279H

REGISTRATION PENDING
Available As FRS234R, FRS234H
5A, 250V
RDS(on)=0.715Ω



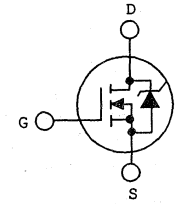
TO-257AA

Radiation-Hardened N-Channel Power MOSFETs

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35 MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
Continuous Drain Current, Id @Tc = 25°C	5	A
@Tc = 100°C	3	A
Pulsed Drain Current, I_{DM}	15	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	15	A
Continuous Source Current (Body diode), Is	5	A
Pulsed Source Current (Body diode), Ism	15	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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PRELIMINARY 2N7280R, 2N7280H

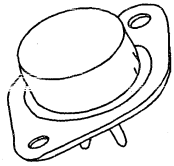
REGISTRATION PENDING

Available As FRM430R, FRM430H

3A, 500V

RDS(on)=2.50Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

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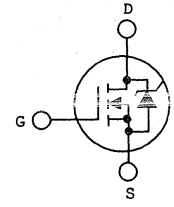


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

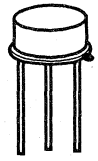
Drain-Source Voltage, VDS	500	V
Drain-Gate Voltage, VDGR (Rgs = 20 kΩ)	500	V
3Continuous Drain Current, Id @Tc = 25°C	3	A
@Tc = 100°C	2	A
Pulsed Drain Current, IDM	9	A
Gate-Source Voltage, VGS	±20	V
Power Dissipation, PT: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, ILM (See Test Figure)	9	A
Continuous Source Current (Body diode), Is	3	A
Pulsed Source Current (Body diode), Ism	9	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): TL		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

2N7281R, 2N7281H

REGISTRATION PENDING
Available As FRL430R, FRL430H
2A, 500V
RDS(on)=2.50Ω

Radiation-Hardened N-Channel Power MOSFETs



JEDEC TO–205AF

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 µm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

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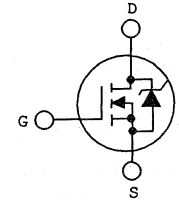

SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	500	V
3Continuous Drain Current, Id @Tc = 25°C	2	A
@Tc = 100°C	1	A
Pulsed Drain Current, I_{DM}	6	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	6	A
Continuous Source Current (Body diode), Is	2	A
Pulsed Source Current (Body diode), Ism	6	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
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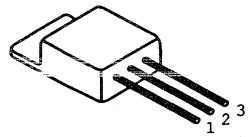
PRELIMINARY 2N7282R, 2N7282H

REGISTRATION PENDING
Available As FRS430R, FRS430H
3A, 500V
RDS(on)=2.52Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-257AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

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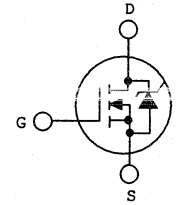


SYMBOL

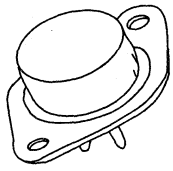
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	500	V
3Continuous Drain Current, Id @Tc = 25°C	3	A
@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}	9	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	9	A
Continuous Source Current (Body diode), Is	3	A
Pulsed Source Current (Body diode), Ism	9	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7283R, 2N7283H

REGISTRATION PENDING
Available As FRM140R, FRM140H
23A, 100V
RDS(on)=0.13Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
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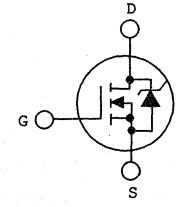

SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
3Continuous Drain Current, Id @Tc = 25°C	23	A
@Tc = 100°C	15	A
Pulsed Drain Current, I_{DM}	69	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	69	A
Continuous Source Current (Body diode), Is	23	A
Pulsed Source Current (Body diode), Ism	69	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
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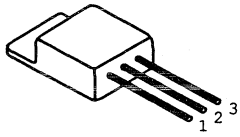
PRELIMINARY

2N7284R, 2N7284H

REGISTRATION PENDING
Available As FRS140R, FRS140H
17A, 100V
RDS(on)=0.145Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-257AA

Features:

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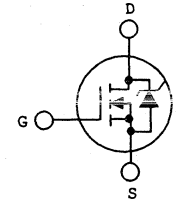


SYMBOL

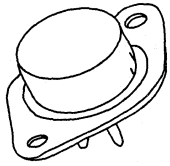
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
3Continuous Drain Current, Id @Tc = 25°C	17	A
@Tc = 100°C	11	A
Pulsed Drain Current, I_{DM}	51	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	51	A
Continuous Source Current (Body diode), Is	17	A
Pulsed Source Current (Body diode), Ism	51	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7285R, 2N7285H

REGISTRATION PENDING
Available As FRM240R, FRM240H
16A, 200V
RDS(on)=0.24Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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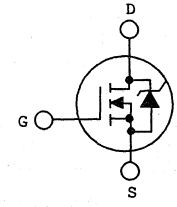


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
3Continuous Drain Current, Id @Tc = 25°C	16	A
@Tc = 100°C	10	A
Pulsed Drain Current, I_{DM}	48	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	48	A
Continuous Source Current (Body diode), Is	16	A
Pulsed Source Current (Body diode), Ism	48	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

PRELIMINARY 2N7286R, 2N7286H

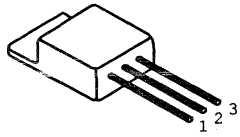
REGISTRATION PENDING

Available As FRS240R, FRS240H

12A, 200V

RDS(on)=0.255Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-257AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
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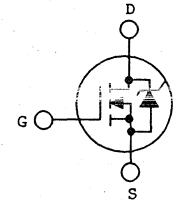


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

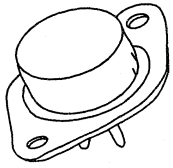
Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
3Continuous Drain Current, Id @Tc = 25°C	12	A
@Tc = 100°C	7	A
Pulsed Drain Current, I_{DM}	36	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	36	A
Continuous Source Current (Body diode), Is	12	A
Pulsed Source Current (Body diode), Ism	36	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

2N7287R, 2N7287H

REGISTRATION PENDING
Available As FRM244R, FRM244H
12A, 250V
RDS(on)=0.40Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
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- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
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  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

3 DISCRETE DEVICES (POWER MOSFETs)

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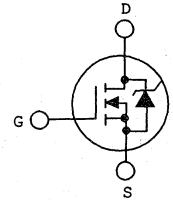

SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
3Continuous Drain Current, Id @Tc = 25°C	12	A
@Tc = 100°C	7	A
Pulsed Drain Current, I_{DM}	36	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
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Pulsed Source Current (Body diode), Ism	36	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

PRELIMINARY 2N7288R, 2N7288H

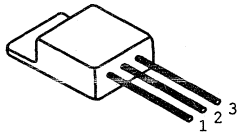
REGISTRATION PENDING

Available As FRS244R, FRS244H

9A, 250V

RDS(on)=0.415Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-257AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
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- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
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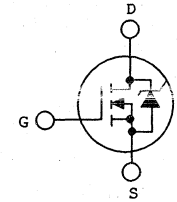


SYMBOL

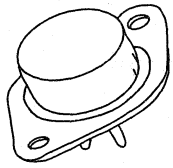
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
3Continuous Drain Current, Id @Tc = 25°C	9	A
@Tc = 100°C	6	A
Pulsed Drain Current, I_{DM}	27	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	27	A
Continuous Source Current (Body diode), Is	9	A
Pulsed Source Current (Body diode), Ism	27	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY 2N7289R, 2N7289H

REGISTRATION PENDING
Available As FRM440R, FRM440H
6A, 500V
RDS(on)=1.40Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AA

Features:

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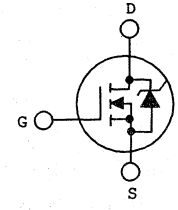

SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	500	V
3Continuous Drain Current, Id @Tc = 25°C	6	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	18	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
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Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	18	A
Continuous Source Current (Body diode), Is	6	A
Pulsed Source Current (Body diode), Ism	18	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

PRELIMINARY 2N7290R, 2N7290H

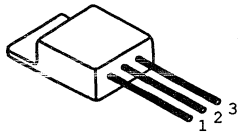
REGISTRATION PENDING

Available As FRS440R, FRS440H

5A, 500V

RDS(on)=1.42Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-257AA

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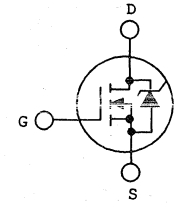


SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	500	V
3Continuous Drain Current, Id @Tc = 25°C	5	A
@Tc = 100°C	3	A
Pulsed Drain Current, I_{DM}	15	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	15	A
Continuous Source Current (Body diode), Is	5	A
Pulsed Source Current (Body diode), Ism	15	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7291R, 2N7291R

REGISTRATION PENDING
AVAILABLE AS FRK150R, FRK150H
40A, 100V
RDS(on) = 0.055Ω

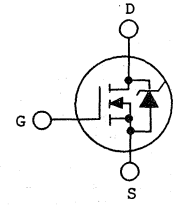
Radiation-Hardened N-Channel Power MOSFETs

TO–204AE

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)sec typically if current-limited to IDM.
- Photo Current—7nA per Rad(Si)/sec typically.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35 MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
Continuous Drain Current, Id @Tc = 25°C	40	A
@Tc = 100°C	25	A
Pulsed Drain Current, I_{DM}	100	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	100	A
Continuous Source Current (Body diode), Is	40	A
Pulsed Source Current (Body diode), Ism	100	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): TL		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

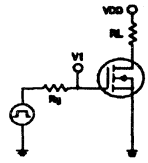
2N7291R, 2N7291H

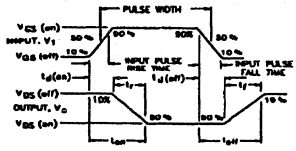
REGISTRATION PENDING

Pre Radiation Electrical Characteristics

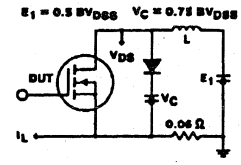
Case Temperature (Tc) = 25°C unless otherwise specified

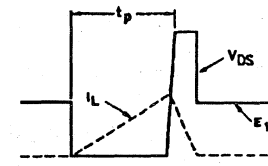
CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volt	BVdss	Vgs = 0, Id = 1mA	100	—	V
Gate-Threshold Volts	Vgs(th)	Vds = Vgs, Id = 1ma	2	4	V
Gate-Body Leakage Forward	Igssf	Vgs = +20V	—	100	nA
Gate-Body Leakage Reverse	Igssr	Vgs = −20V	—	100	nA
Zero-Gate Voltage Drain Current	Idss1 Idss2 Idss3	Vds = 100V, Vgs = 0 Vds = 80V, Vgs = 0 Vds = 80V, Vgs = 0, Tc = 125°C	— — —	1 .025 .25	mA
Rated Avalanche Current	Iar	Time = 20uS	—	100	A
Drain-Source On-State Volts	Vds(on)	Vgs = 10V, Id = 40A	—	2.32	V
Drain-Source On Resistance	Rds(on)	Vgs = 10V, Id = 25A	—	.055	Ω
Turn-On Delay Time	td(on)	Vdd = 50V, Id = 40A PULSE WIDTH = 3uS PERIOD = 300mS Rg = 25Ω 0 ≤ VGS ≤ 20 (SEE TEST CIRCUIT)	—	170	nS
Rise Time	tr		—	1120	
Turn-Off Delay Time	td(off)		—	420	
Fall Time	tf		—	380	
Gate-Charge Threshold	Qg(th)	Vdd = 50V, IGS1 = IGS2 Id = 40A 0 ≤ VGS ≤ 20 (SEE FIGURE)	3.5	15	nC
Gate-Charge Total	Qgm		140	560	
Gate-Charge On State	Qg(on)		58	230	
Diode Forward Voltage	Vsd	Id = 40A, Vgd = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 10A; di/dt = 100A/uS	—	1400	nS
Junction-To-Case	RΘjc	—	—	0.83	°C/W
Junction-to-Ambient	RΘja	Free Air Operation	—	30	



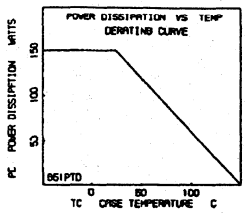


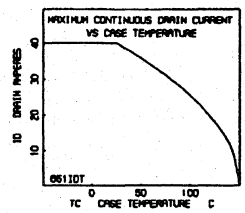
SWITCHING TIME TESTING

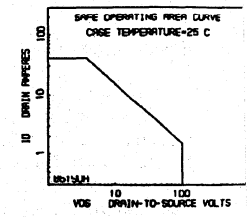




CLAMPED INDUCTIVE SWITCHING, ILM



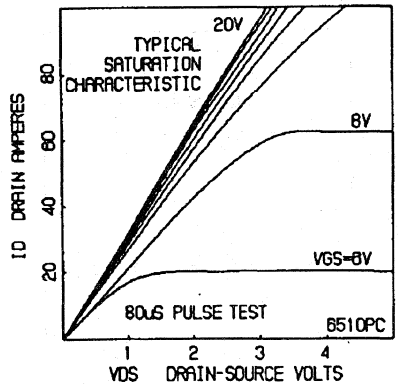


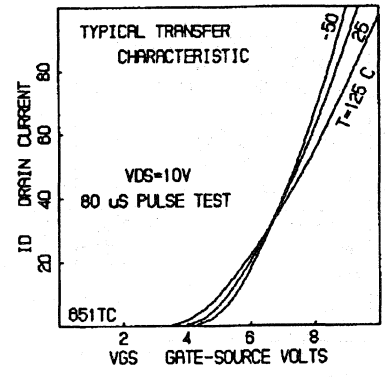


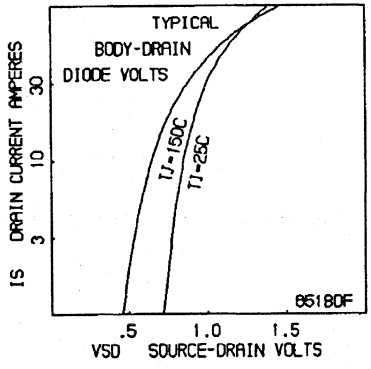
2N7291R, 2N7291H

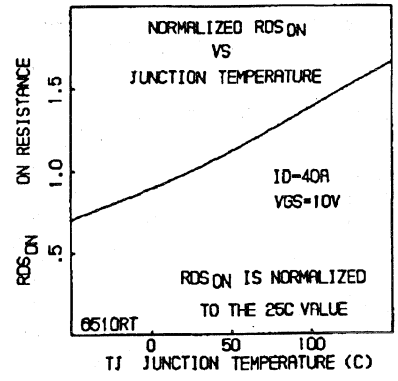
REGISTRATION PENDING

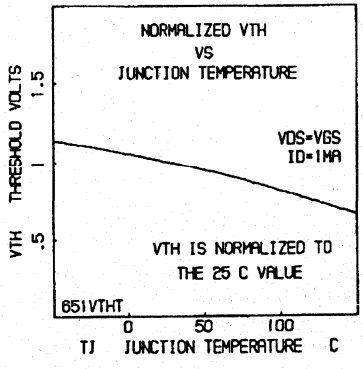
Typical Characteristics

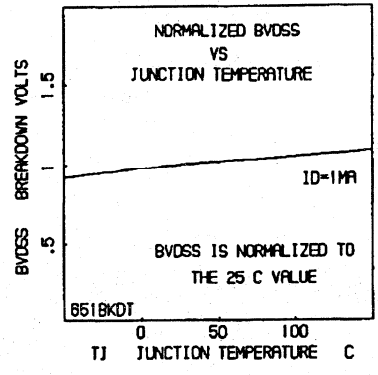








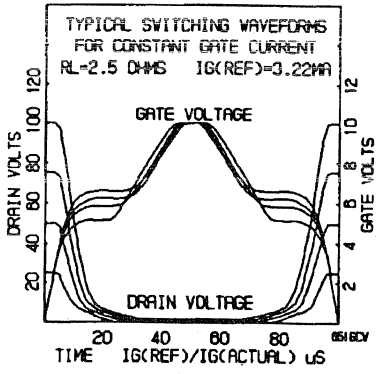


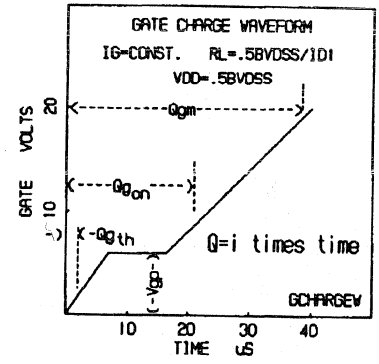


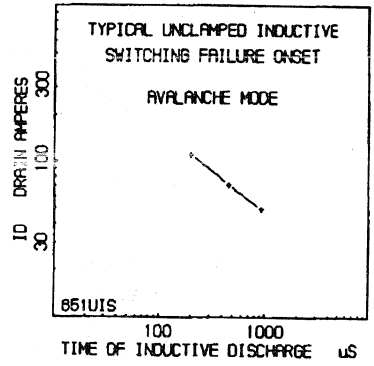
2N7291R, 2N7291H

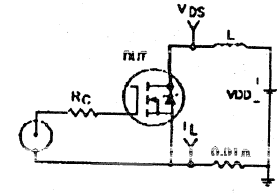
REGISTRATION PENDING

Typical Characteristics, Continued

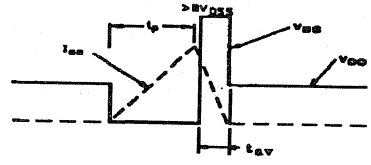


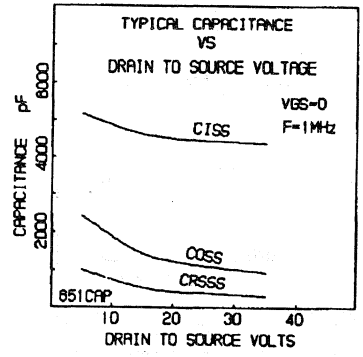


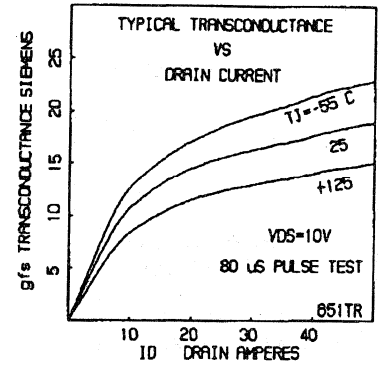




UNCLAMPED INDUCTIVE SWITCHING







2N7291R, 2N7291H

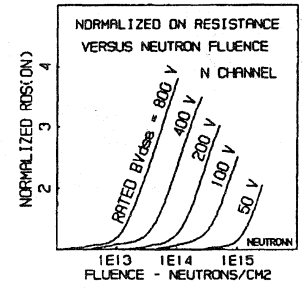
REGISTRATION PENDING

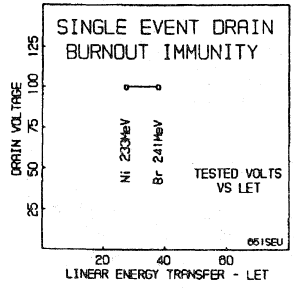
Post Radiation Electrical Characteristics

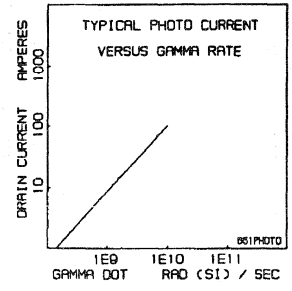
Case Temperature (Tc) = 25°C unless otherwise specified

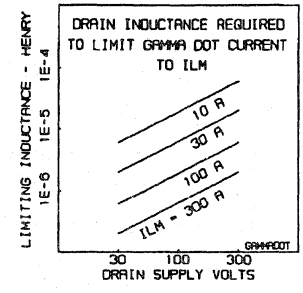
CHARACTERISTIC		TYPE	NOTES	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVdss	2N7291R	4, 6	Vgs = 0V, Id = 1mA	100	—	V
		2N7291H	5, 6		95	—	
Gate Source Threshold Volts	Vgs(th)	2N7291R	4, 6	Vgs = Vds, Id = 1mA	2	4	V
		2N7291H	3, 5, 6		1.5	4.5	
Gate-Body Leakage Forward	Igssf	2N7291R	4, 6	Vgs = 20V, Vds = 0V	—	100	nA
		2N7291H	5, 6		—	200	
Gate-Body Leakage Reverse	Igssr	2N7291R	2, 4, 6	Vgs = −20V, Vds = 0V	—	100	nA
		2N7291H	2, 5, 6		—	200	
Zero-Gate Voltage Drain Current	Idss	2N7291R	4, 6	Vgs = 0, Vds = 80V	—	25	µA
		2N7291H	5, 6		—	100	
Drain-Source On-State Volts	Vds(on)	2N7291R	1, 4, 6	Vgs = 10V, Id = 40A	—	2.32	V
		2N7291H	1, 5, 6	Vgs = 16V, Id = 40A	—	3.20	
Drain-Source On Resistance	Rds(on)	2N7291R	1, 4, 6	Vgs = 10V, Id = 25A	—	.055	Ω
		2N7291H	1, 5, 6	Vgs = 14V, ID = 25A	—	.080	

NOTES: (1) Pulse test, 300us max
(2) Absolute value
(3) Gamma = 300KRad(Si)
(4) Gamma = 100KRad(Si) and/or Neutron = 3E13
(5) Gamma = 1000KRad(Si) and/or Neutron = 3E13
(6) Insitu Gamma bias must be sampled for both
Vgs = +10V, Vds = 0V and
Vgs = 0V, Vds = 80% BVdss
(7) Gamma data taken 11/6/89 on TA17651 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
(8) Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
(9) Neutron derivation, HARRIS Application note AN-8831, Oct, 1988







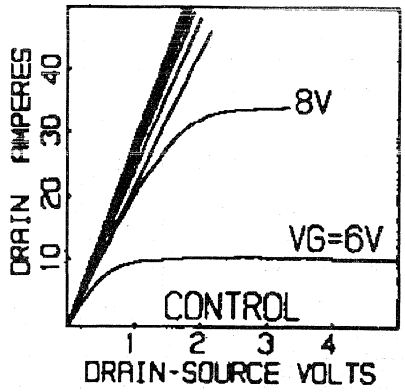


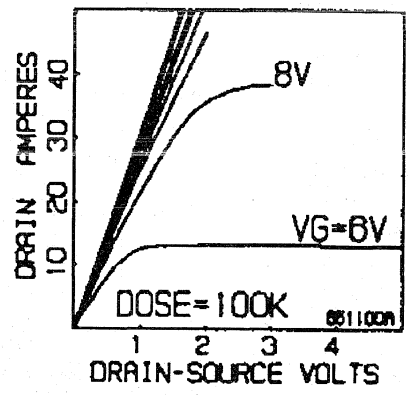
2N7291R, 2N7291H

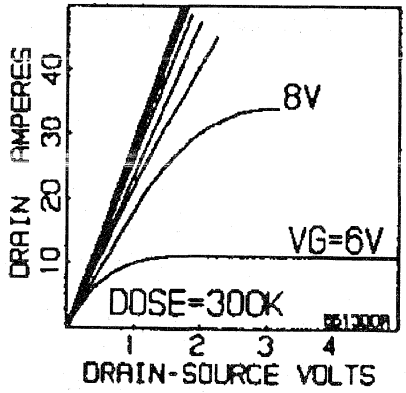
REGISTRATION PENDING

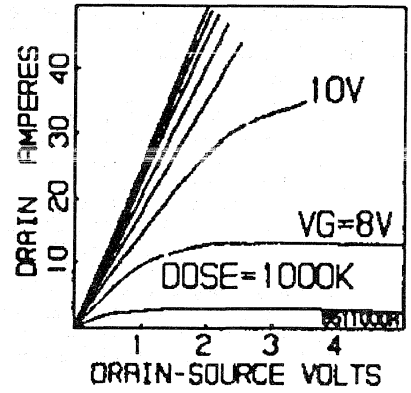
Typical Post Response Curves to Gamma (Total Dose)

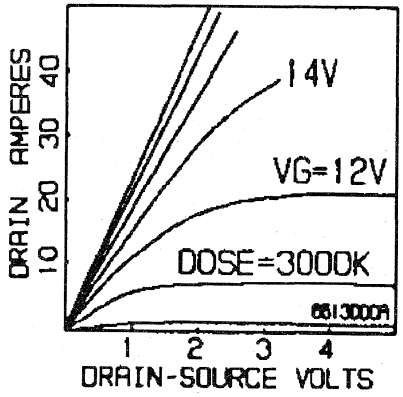
Device Bias During Irradiation (Insitu Bias) is = VG = +10, VD = 0

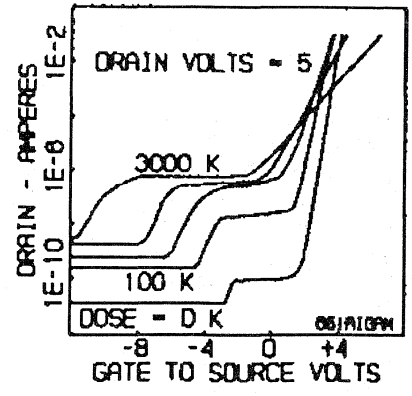






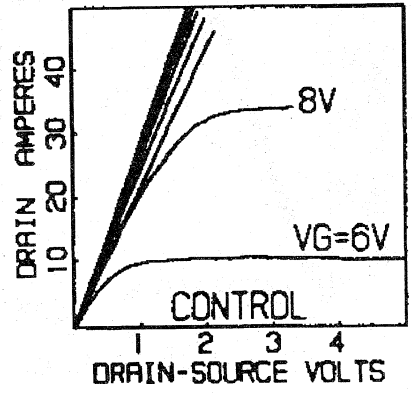


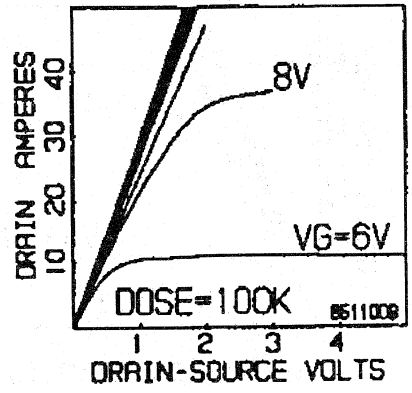


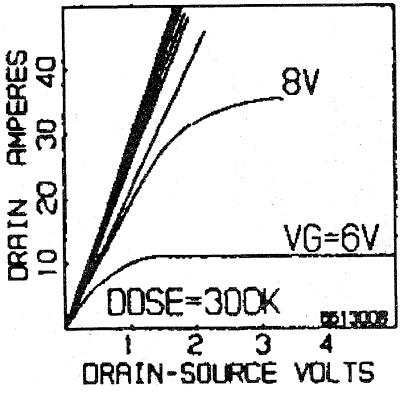


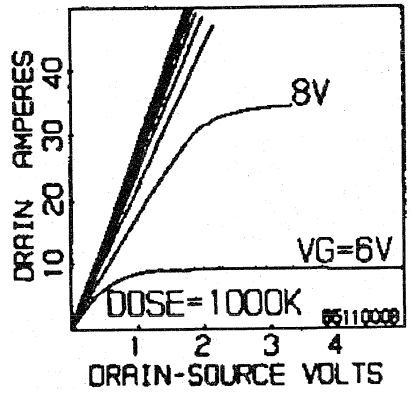
Typical Post Response Curves to Gamma (Total Dose), Cont'd.

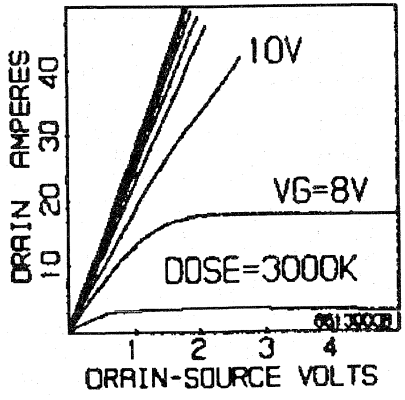
Device Bias During Irradiation (Insitu Bias) is = VG = -10, VD = 0

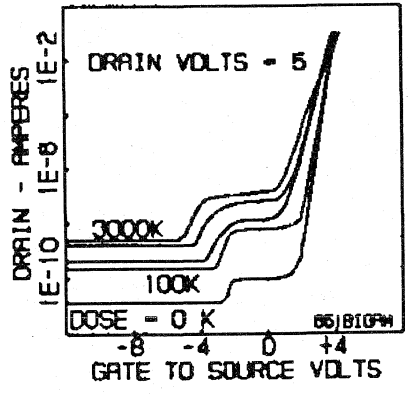






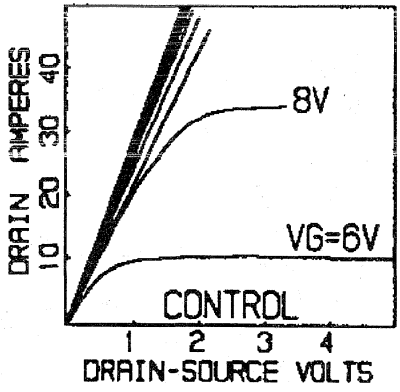


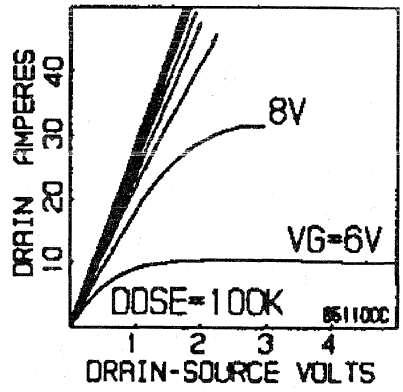


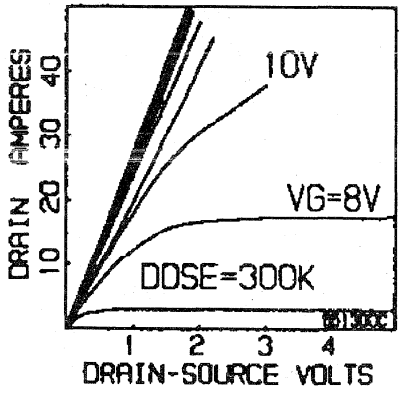


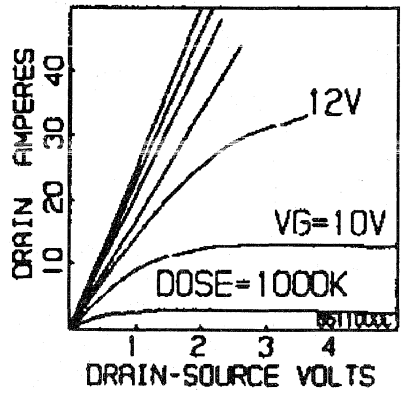
Typical Post Response Curves to Gamma (Total Dose), Cont'd.

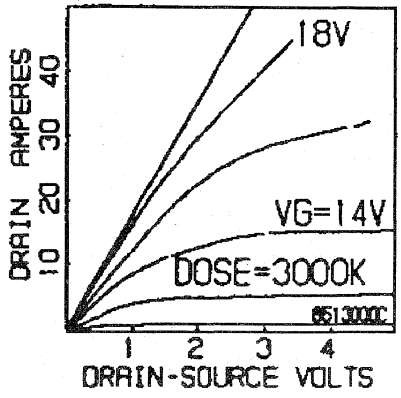
Device Bias During Irradiation (Insitu Bias) is = VG = 0, VD = 0

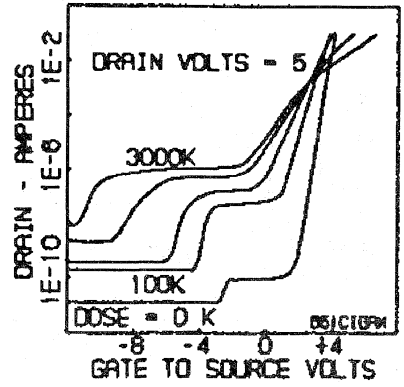






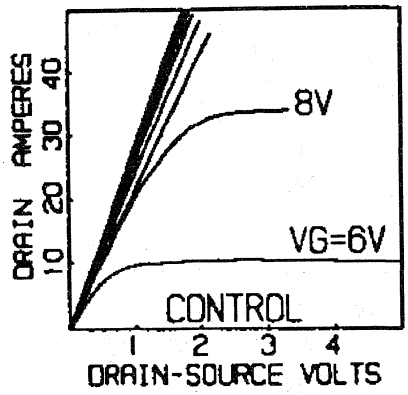


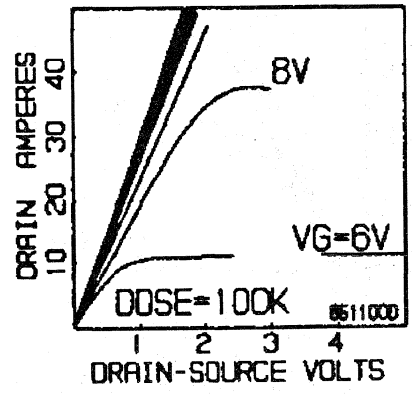


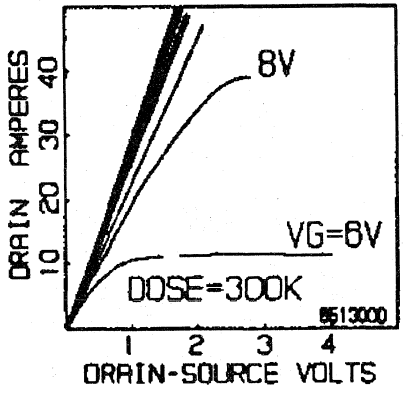


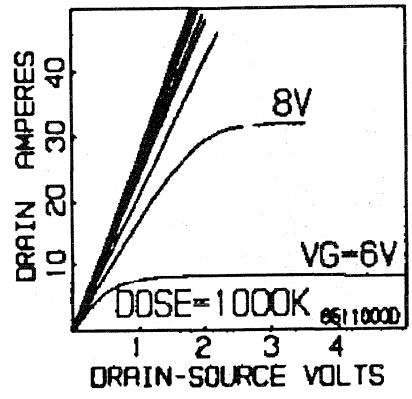
Typical Post Response Curves to Gamma (Total Dose), Cont'd.

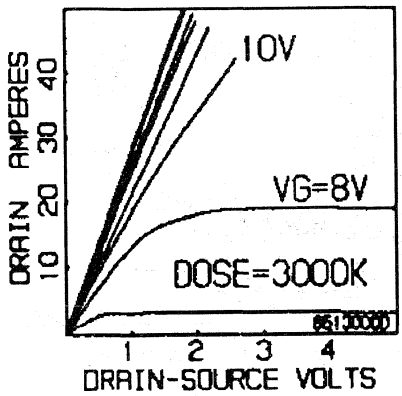
Device Bias During Irradiation (Insitu Bias) is = VG = -10, VD = 80

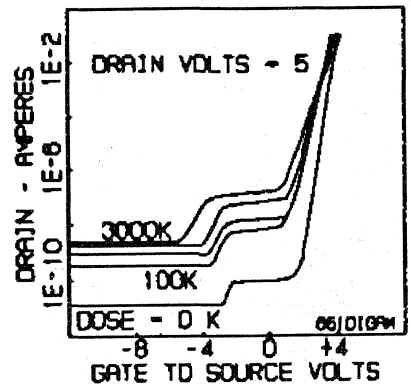










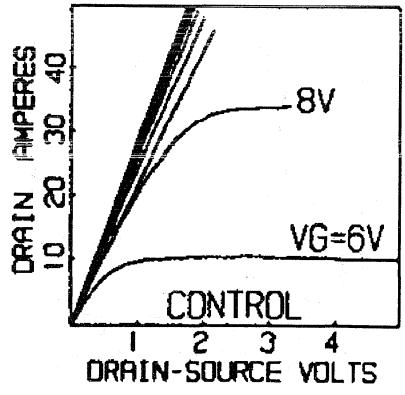


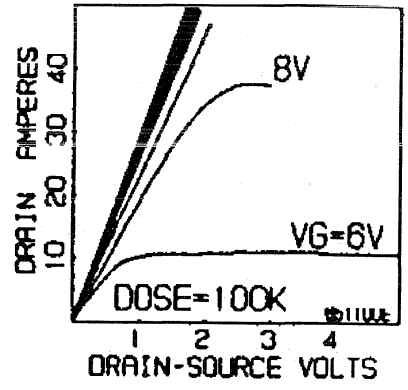
2N7291R, 2N7291H

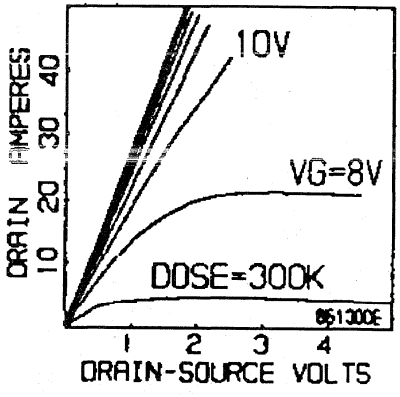
REGISTRATION PENDING

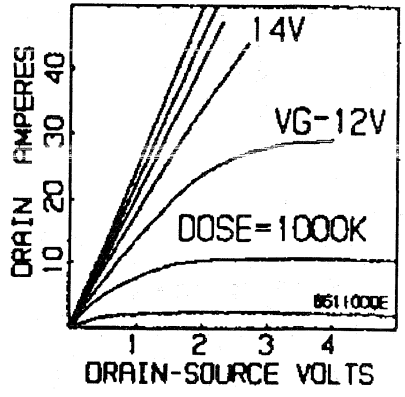
Typical Post Response Curves to Gamma (Total Dose), Cont'd.

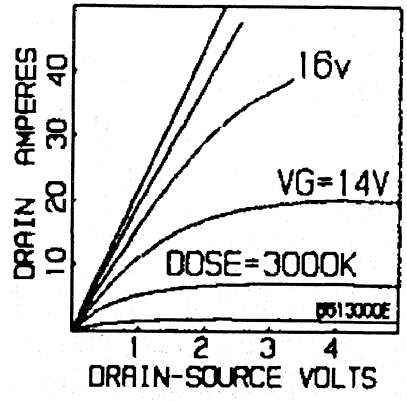
Device Bias During Irradiation (Insitu Bias) is = VG = 0, VD = 80

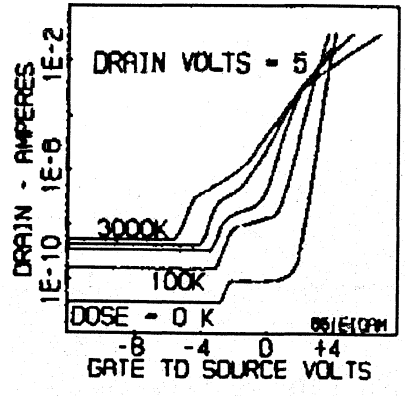










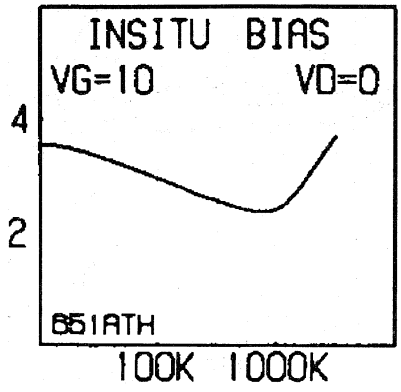


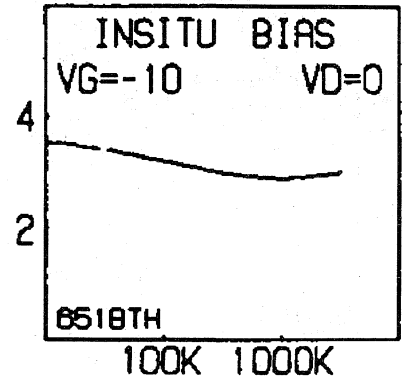
2N7291R, 2N7291H

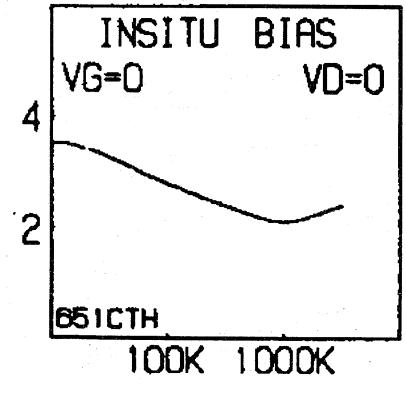
REGISTRATION PENDING

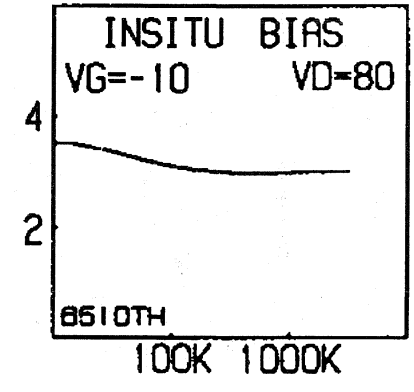
Typical Response Curves to Gamma (Total Dose)

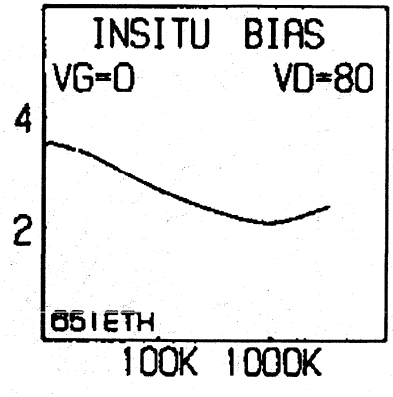
Threshold Volts VS Total Dose RAD(Si) VGS = VDS; ID = 1ma









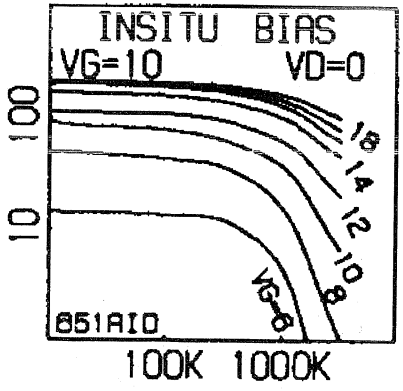


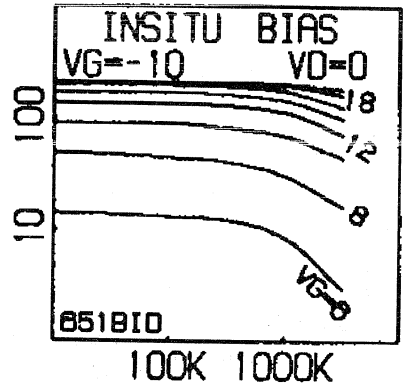
2N7291R, 2N7291H

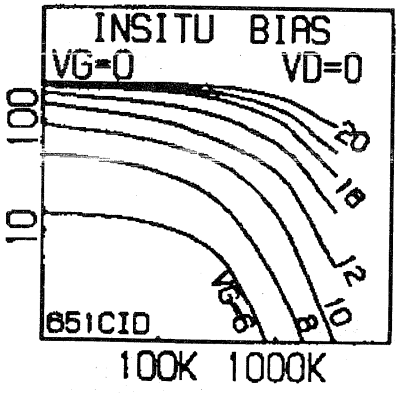
REGISTRATION PENDING

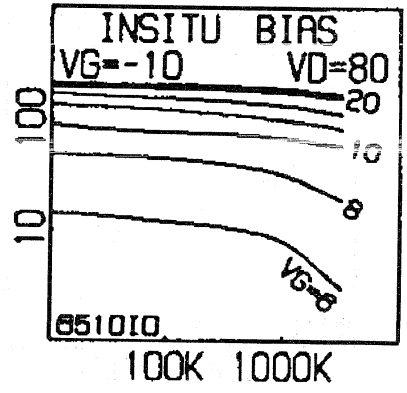
Typical Response Curves to Gamma (Total Dose), Cont'd.

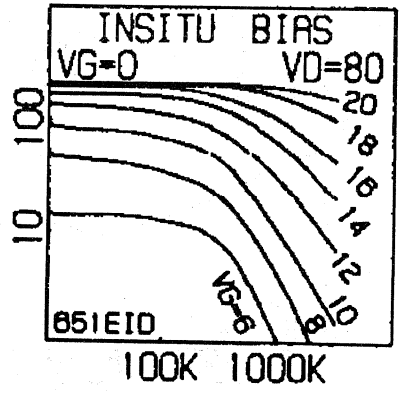
Drain Amperes IDS(on) VS Total Dose RAD(Si) VDS = 10; VGS = 6, 8, 10, 12, 14, 16, 18, 20 Volts





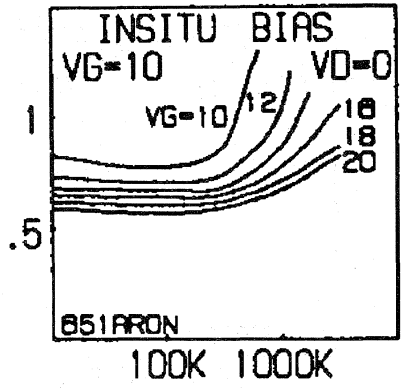


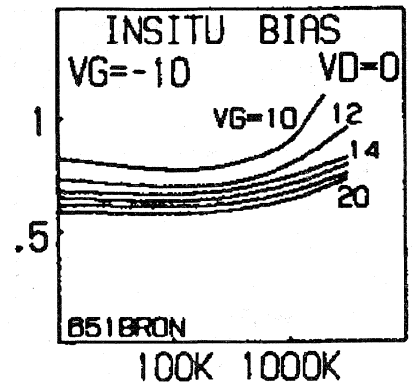


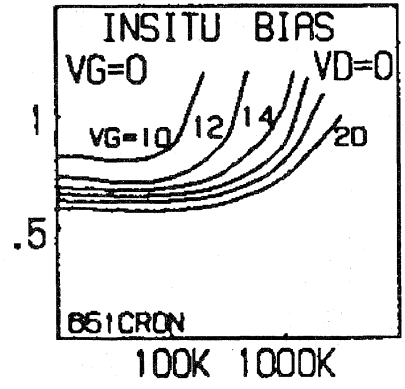


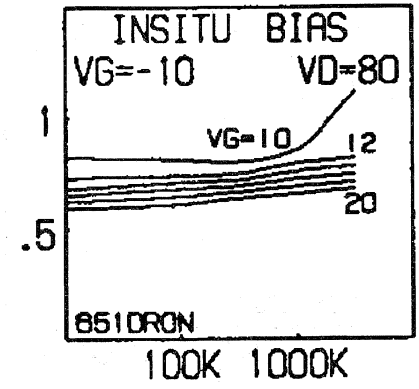
Typical Response Curves to Gamma (Total Dose), Cont'd.

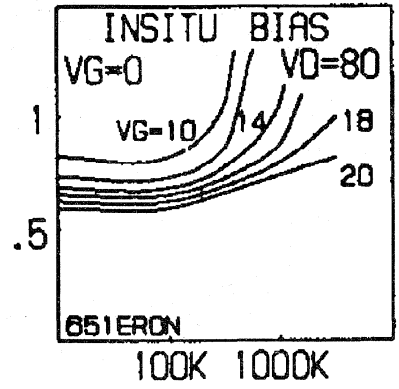
RDS(on) [Normalized to Rated RDS(on)] VS Total Dose RAD(Si) Id = 40A; Vgs = 10, 12, 14, 16, 18, 20 Volts





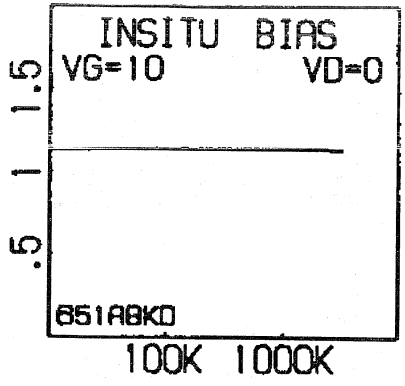


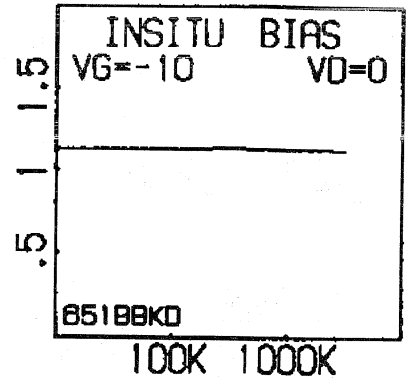


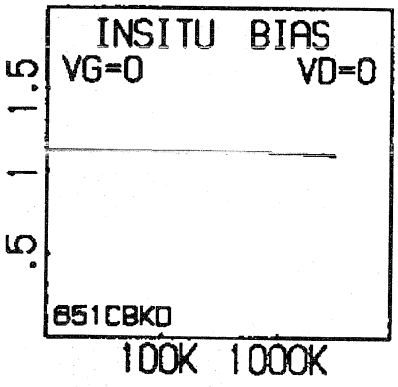


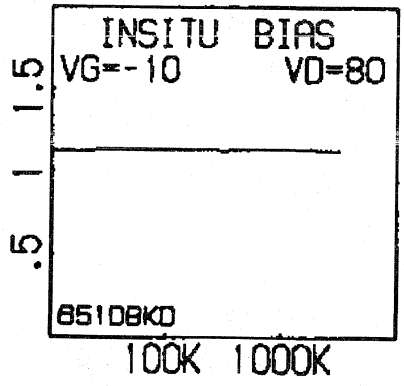
Typical Response Curves to Gamma (Total Dose), Cont'd.

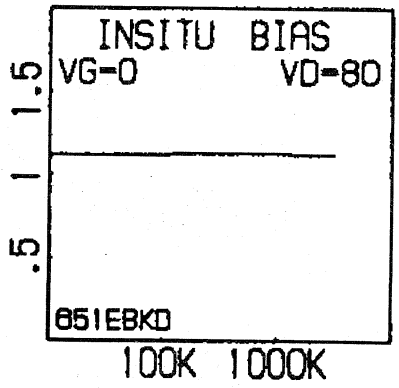
BVdss (Normalized to Rated BVdss) VS Total Dose RAD(Si) Id = 1mA









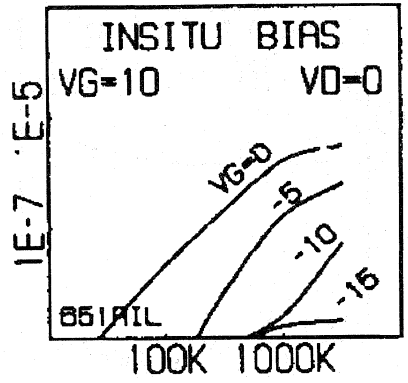


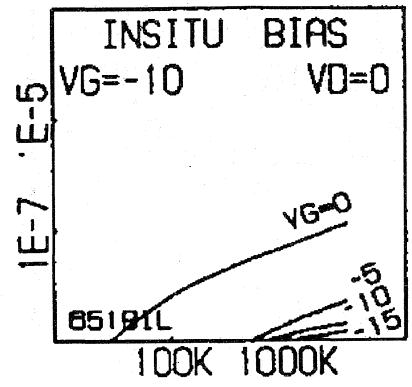
2N7291R, 2N7291H

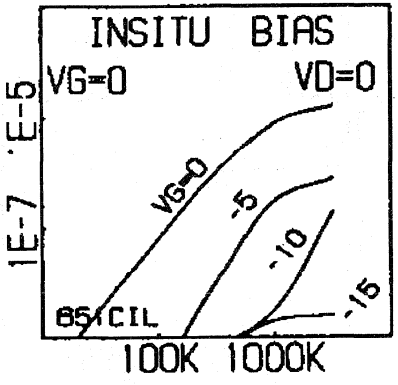
REGISTRATION PENDING

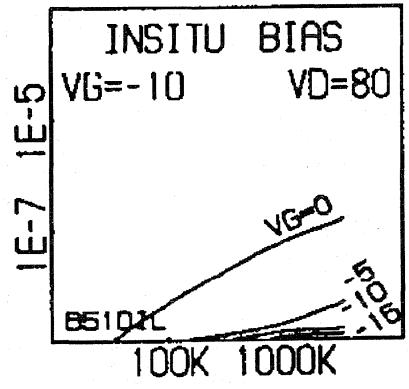
Typical Response Curves to Gamma (Total Dose), Cont'd.

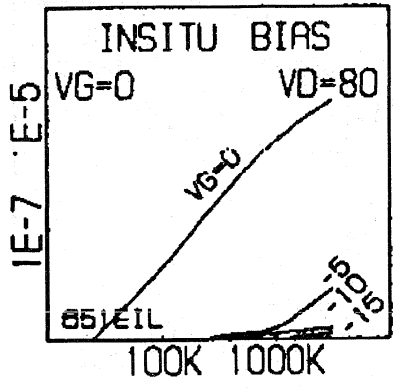
Drain Leakage Amperes VS Total Dose RAD(Si) Vgs = 0, -5, -10, -15; Vds = 5 Volts









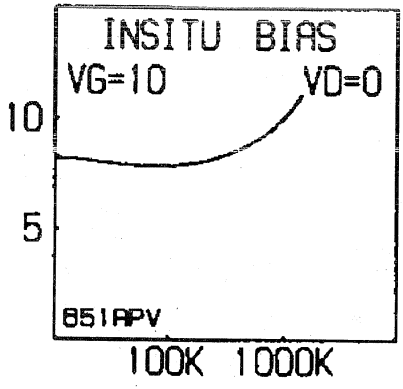


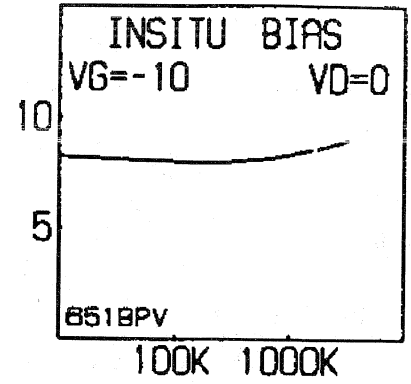
2N7291R, 2N7291H

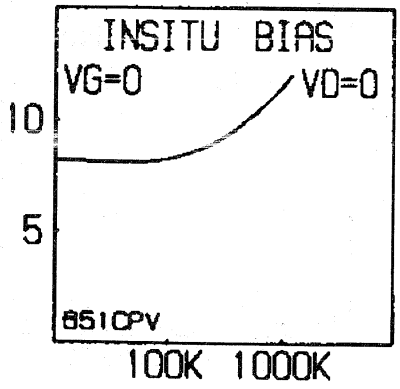
REGISTRATION PENDING

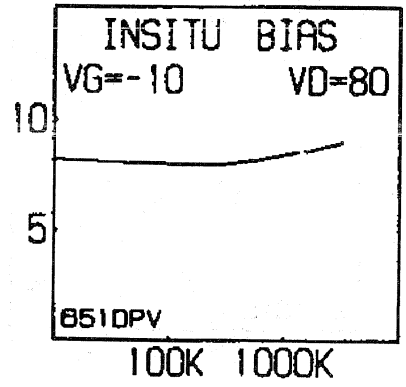
Typical Response Curves to Gamma (Total Dose), Cont'd.

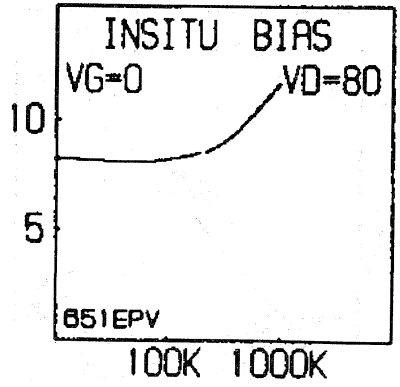
VGP Gate Plateau Volts VS Total Dose RAD(Si) Id = 40A; Vd = 10 Volts









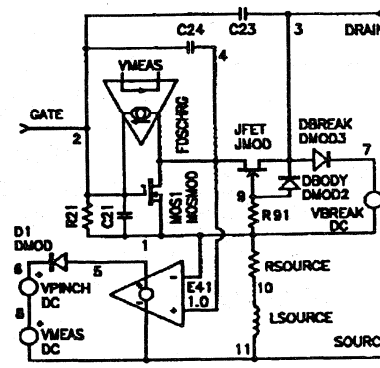


2N7291R, 2N7291H

REGISTRATION PENDING

Spice Parameters and Sub Circuit

```
.SUBCKT 2N7291 3 2 11; REV 5/03/90
R21 2 1 1E9
R91 9 1 0.0001
C21 2 1 3900p
C23 2 3 350p
C24 2 4 8000p
FDSCHRG 4 2 VMEAS 1.0
MOS1 4 2 1 1 mosmod L = 1u   W = 1u
JFET 3 9 4 JMOD 1
DBODY 9 3 DMOD2
RSOURCE 1 10 .016
LSOURCE 10 11 7.5n
E41 5 11 4 1 1.0
D1 5 6 DMOD
VPINCH 6 8 DC 5.5
VMEAS 8 11 DC 0
DBREAK 3 7 DMOD3
VBREAK 7 1 DC 115
.MODEL MOSMOD NMOS VTO = 4   KP = 14   TOX = 1.OE+06U
.MODEL JMOD NJF VTO = –5.5   BETA = 1400   IS = 5.1E–18   RD = .0111
.MODEL DMOD D IS = 1.OE–13   N = 0.03   RS = .001
.MODEL DMOD2 D CJO = 8910P   TT = 700n   IS = 5.1E–12
.MODEL DMOD3 D IS = 1.OE–13   RS = .5   N = 1.0
.ENDS
```



Verified on PSPICE

Reference: C.F. Wheatley, Jr. H.R. Ronan, Jr. G.M. Dolny, "Spicing-Up Spice II Software For Power MOSFET Modeling", Harris Application Note AN-8610, 4-87

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

2N7292R, 2N7292H

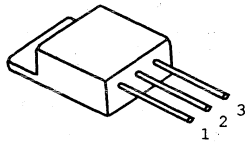
REGISTRATION PENDING

Available As FRF150R, FRF150H

25A, 100V

RDS(on)=0.07Ω

Radiation-Hardened N-Channel Power MOSFETs

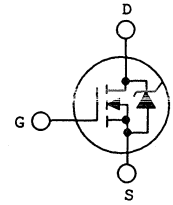


TO-254AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 µm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
3Continuous Drain Current, Id @Tc = 25°C	25	A
@Tc = 100°C	20	A
Pulsed Drain Current, I_{DM}	75	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	75	A
Continuous Source Current (Body diode), Is	25	A
Pulsed Source Current (Body diode), Ism	75	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7293R, 2N7293H

REGISTRATION PENDING
Available As FRK250R, FRK250H
27A, 200V
RDS(on)=0.10Ω

Radiation-Hardened N-Channel Power MOSFETs

TO–204AE

Features:

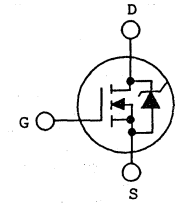
- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	200	V
3Continuous Drain Current, Id @Tc = 25°C	27	A
@Tc = 100°C	17	A
Pulsed Drain Current, I_{DM}	81	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	81	A
Continuous Source Current (Body diode), Is	27	A
Pulsed Source Current (Body diode), Ism	81	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7293R, 2N7293H

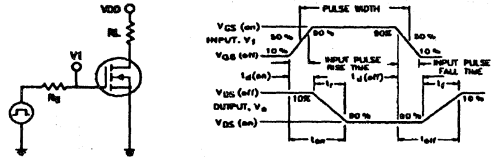
REGISTRATION PENDING

Available As FRK250 (R/H)

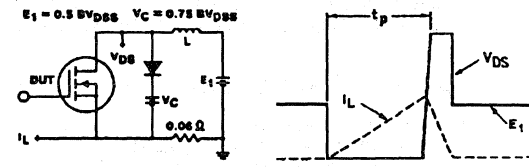
Pre Radiation Electrical Characteristics

Case Temperature (Tc) = 25°C unless otherwise specified

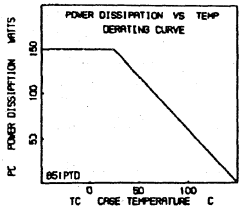
CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volt	BVdss	Vgs = 0, Id = 1mA	200	—	V
Gate-Threshold Volts	Vgs(th)	Vds = Vgs, Id = 1ma	2	4	V
Gate-Body Leakage Forward	Igssf	Vgs = +20V	—	100	nA
Gate-Body Leakage Reverse	Igssr	Vgs = −20V	—	100	nA
Zero-Gate Voltage Drain Current	Idss1 Idss2 Idss3	Vds = 200V, Vgs = 0 Vds = 160V, Vgs = 0 Vds = 160V, Vgs = 0, Tc = 125°C	— — —	1 .025 .25	mA
Rated Avalanche Current	Iar	Time = 20uS	—	81	A
Drain-Source On-State Volts	Vds(on)	Vgs = 10V, Id = 27A	—	2.7	V
Drain-Source On Resistance	Rds(on)	Vgs = 10V, Id = 17A	—	.100	Ω
Turn-On Delay Time	td(on)	Vdd = 100V, Id = 27A PULSE WIDTH = 3uS PERIOD = 300mS Rg = 25Ω 0 ≤ VGS ≤ 20 (SEE TEST CIRCUIT)	—	170	nS
Rise Time	tr		—	600	
Turn-Off Delay Time	td(off)		—	580	
Fall Time	tf		—	300	
Gate-Charge Threshold	Qg(th)	Vdd = 100V, IGS1 = IGS2 Id = 27A 0 ≤ VGS ≤ 20 (SEE FIGURE)	3.5	15	nC
Gate-Charge Total	Qgm		120	485	
Gate-Charge On State	Qg(on)		61	244	
Diode Forward Voltage	Vsd	Id = 40A, Vgd = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 10A; di/dt = 100A/uS	—	1700	nS
Junction-To-Case	Rθjc	—	—	0.83	°C/W
Junction-to-Ambient	Rθja	Free Air Operation	—	30	

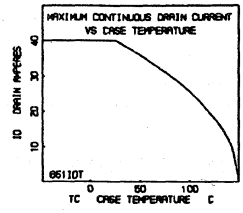


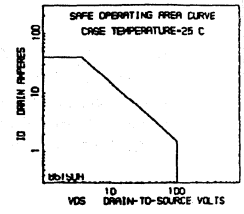
SWITCHING TIME TESTING



CLAMPED INDUCTIVE SWITCHING, ILM





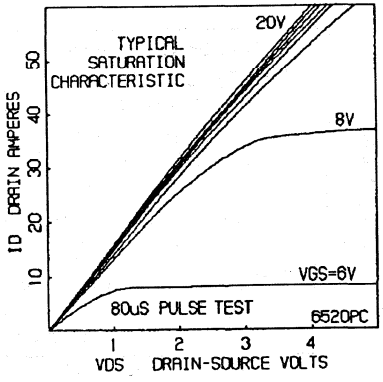


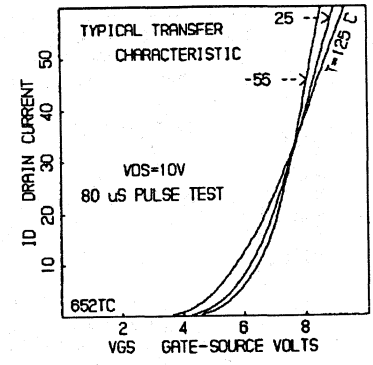
2N7293R, 2N7293H

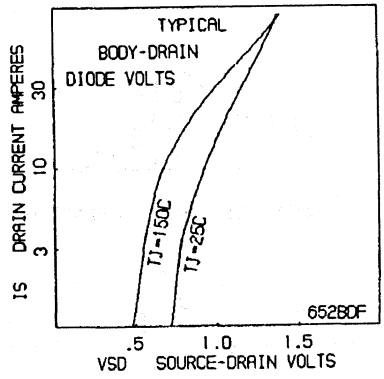
REGISTRATION PENDING

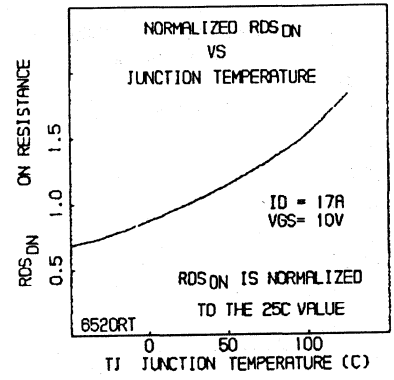
Available As FRK250 (R/H)

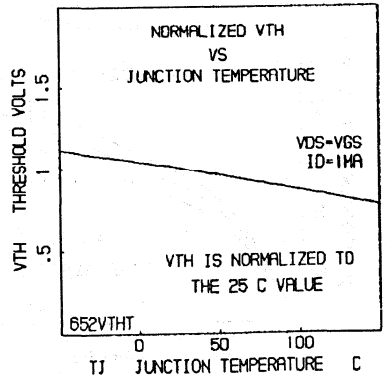
Typical Characteristics

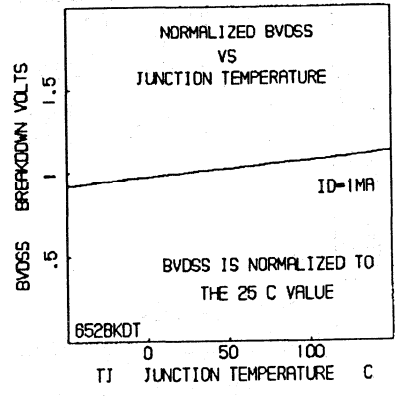










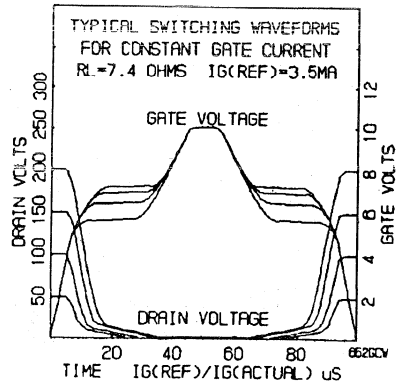


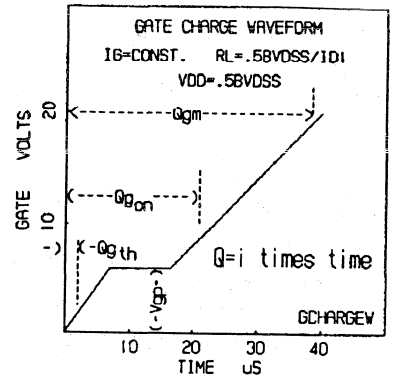
2N7293R, 2N7293H

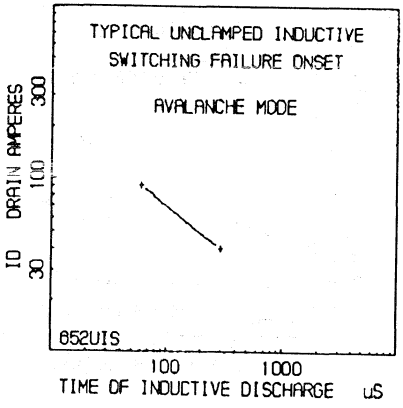
REGISTRATION PENDING

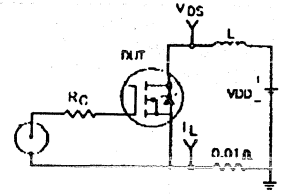
Available As FRK250 (R/H)

Typical Characteristics, Continued

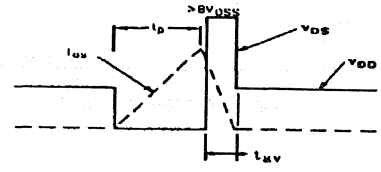


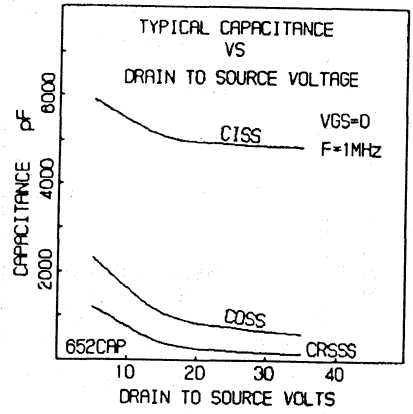


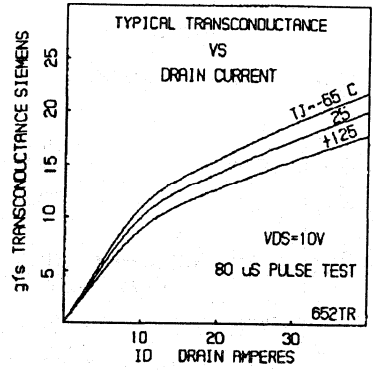




UNCLAMPED INDUCTIVE SWITCHING







2N7293R, 2N7293H

REGISTRATION PENDING

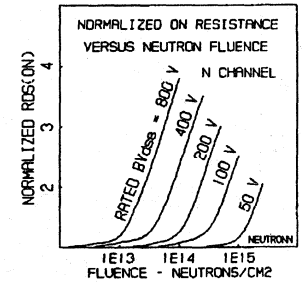
Available As FRK250 (R/H)

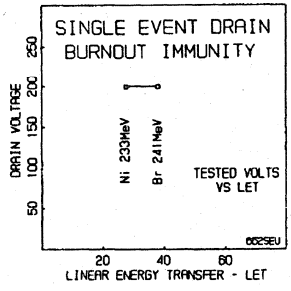
Post Radiation Electrical Characteristics

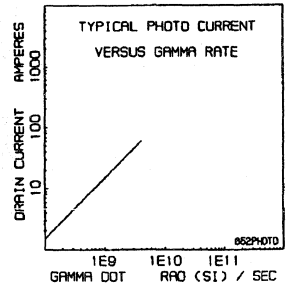
Case Temperature (Tc) = 25°C unless otherwise specified

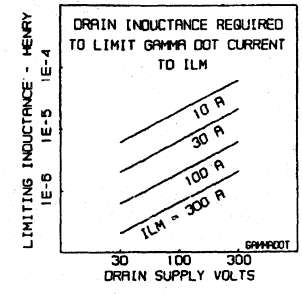
CHARACTERISTIC		TYPE	NOTES	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVdss	2N7293R	4, 6	Vgs = 0, Id = 1mA	200	—	V
		2N7293H	5, 6		190	—	
Gate Source Threshold Volts	Vgs(th)	2N7293R	4, 6	Vgs = Vds, Id = 1mA	2	4	V
		2N7293H	3, 5, 6		1.5	4.5	
Gate-Body Leakage Forward	Igssf	2N7293R	4, 6	Vgs = 20, Vds = 0	—	100	nA
		2N7293H	5, 6		—	200	
Gate-Body Leakage Reverse	Igssr	2N7293R	2, 4, 6	Vgs = −20, Vds = 0	—	100	nA
		2N7293H	2, 5, 6		—	200	
Zero-Gate Voltage Drain Current	Idss	2N7293R	4, 6	Vgs = 0, Vds = 160	—	25	µA
		2N7293H	5, 6		—	100	
Drain-Source On-State Volts	Vds(on)	2N7293R	1, 4, 6	Vgs = 10, Id = 27	—	2.7	V
		2N7293H	1, 5, 6	Vgs = 16, Id = 27	—	2.7	
Drain-Source On Resistance	Rds(on)	2N7293R	1, 4, 6	Vgs = 10, Id =17	—	.100	Ω
		2N7293H	1, 5, 6	Vgs = 14, ID = 17	—	.140	

NOTES: (1) Pulse test, 300us max
(2) Absolute value
(3) Gamma = 300KRad(Si)
(4) Gamma = 100KRad(Si) and/or Neutron = 3E13
(5) Gamma = 1000KRad(Si) and/or Neutron = 3E13
(6) Insitu Gamma bias must be sampled for both
Vgs = +12V, Vds = 0V and
Vgs = 0V, Vds = 80% BVdss
(7) Gamma data taken 11/1/89 on TA17652 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
(8) Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
(9) Neutron derivation, HARRIS Application note AN-8831, Oct, 1988









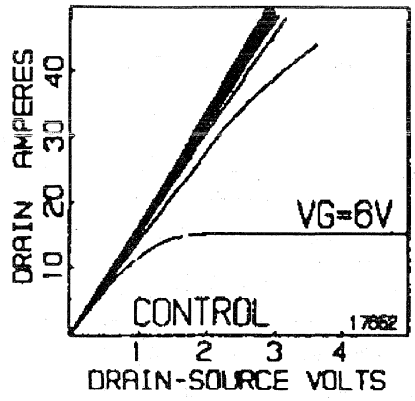
2N7293R, 2N7293H

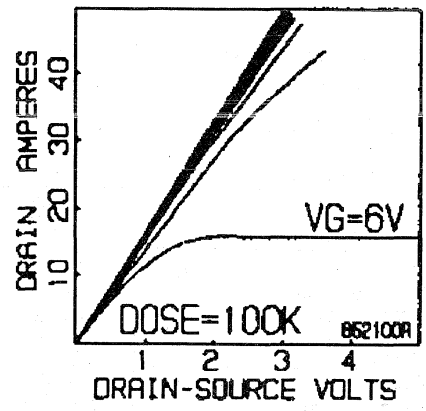
REGISTRATION PENDING

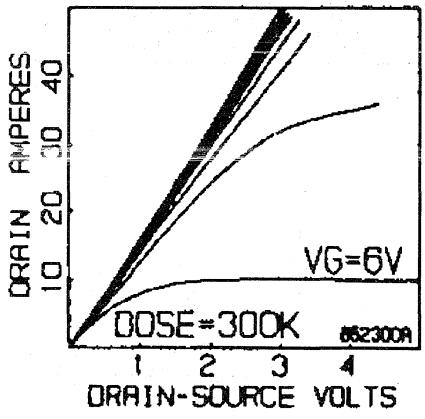
Available As FRK250 (R/H)

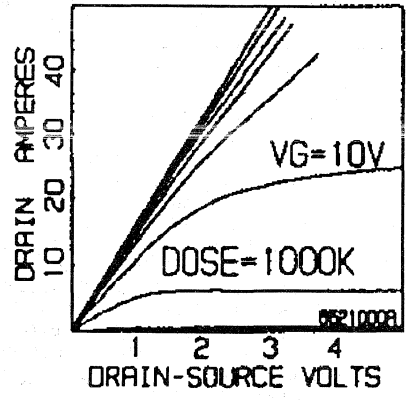
Typical Post Response Curves To Gamma (Total Dose)

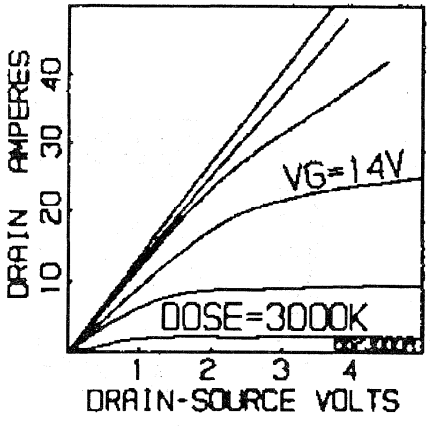
Device Bias During Irradiation (Insitu Bias) is = VG=+10, VD=0

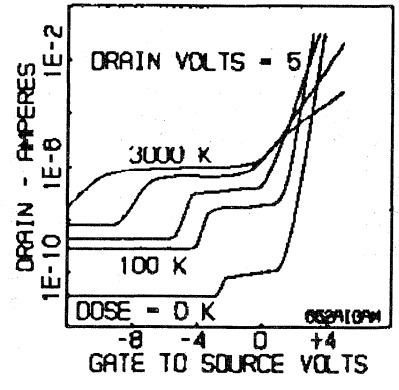












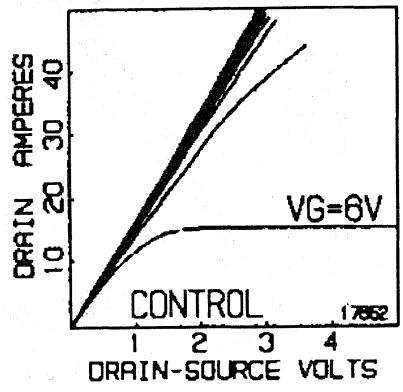
2N7293R, 2N7293H

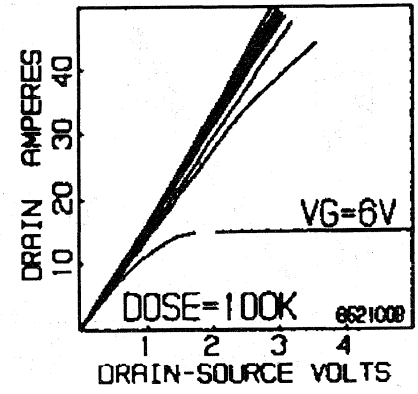
REGISTRATION PENDING

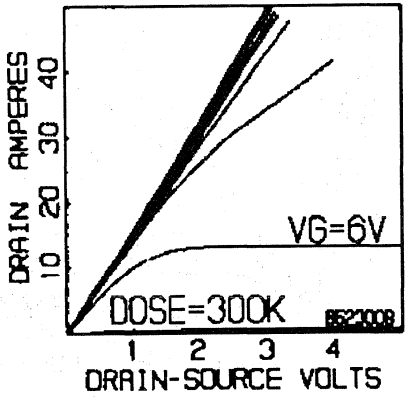
Available As FRK250 (R/H)

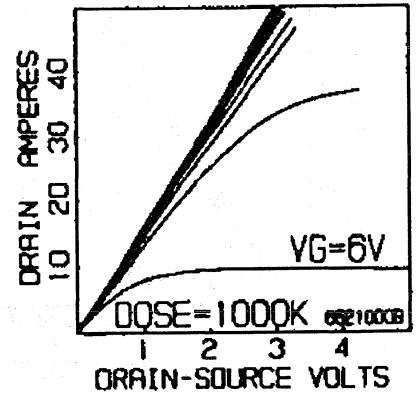
Typical Post Response Curves To Gamma (Total Dose), Cont'd.

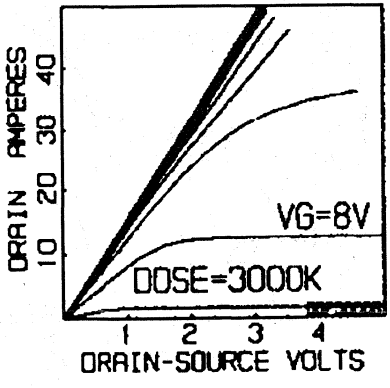
Device Bias During Irradiation (Insitu Bias) is = VG=-10, VD=0

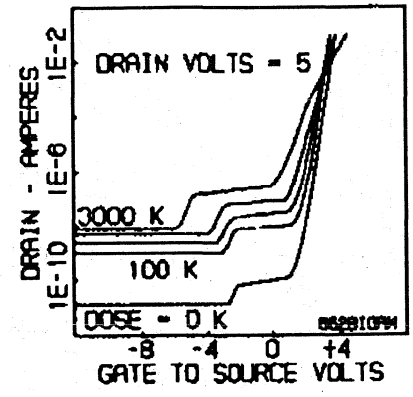












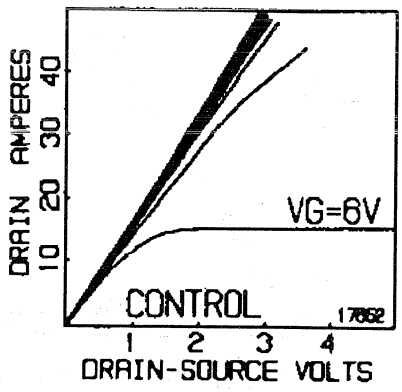
2N7293R, 2N7293H

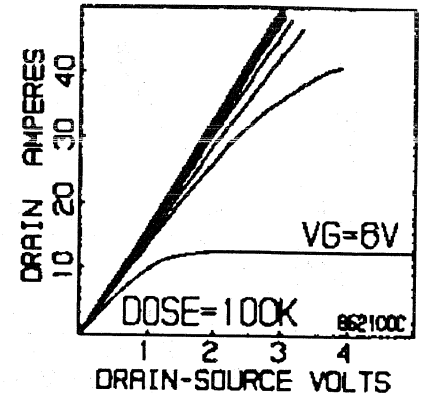
REGISTRATION PENDING

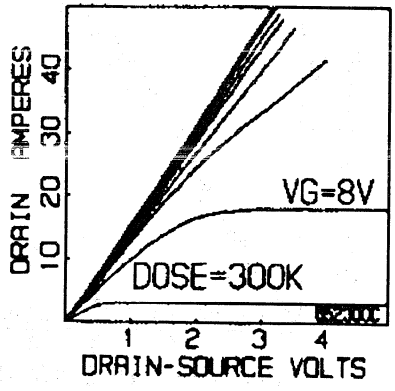
Available As FRK250 (R/H)

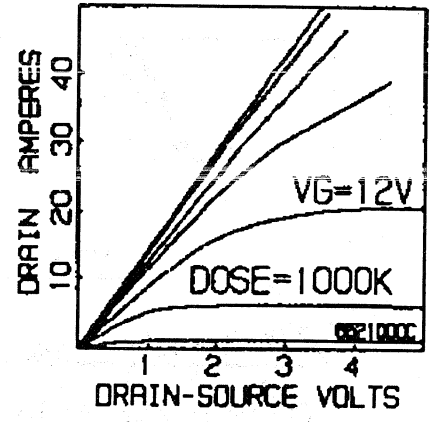
Typical Post Response Curves To Gamma (Total Dose), Cont'd.

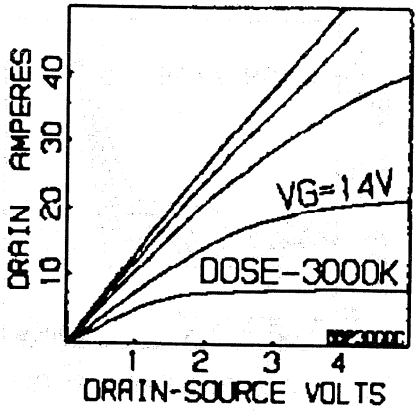
Device Bias During Irradiation (Insitu Bias) is = VG= 0, VD=0

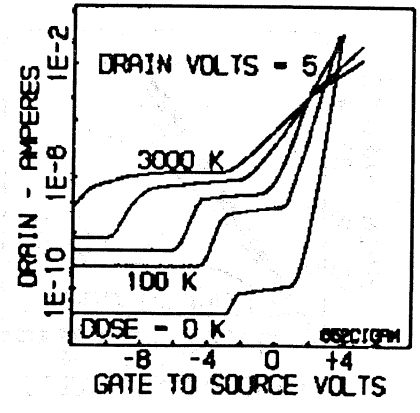






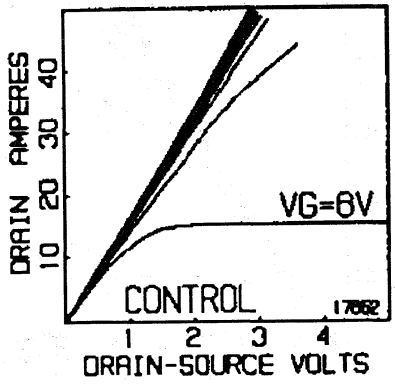


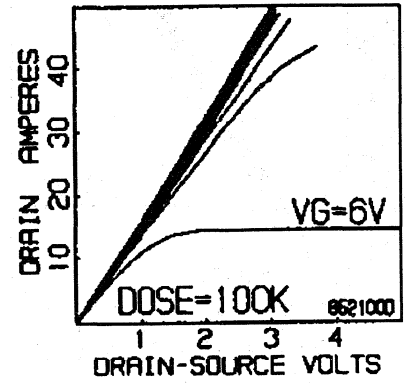


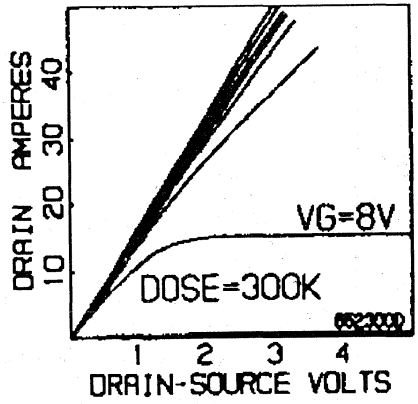


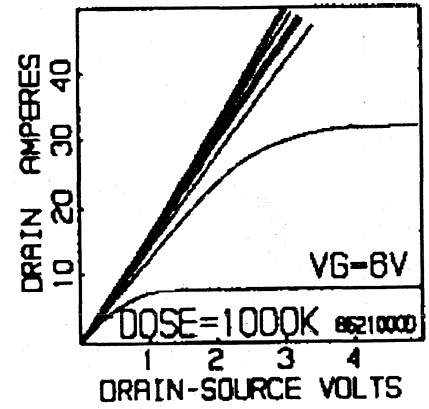
Typical Post Response Curves To Gamma (Total Dose), Cont'd.

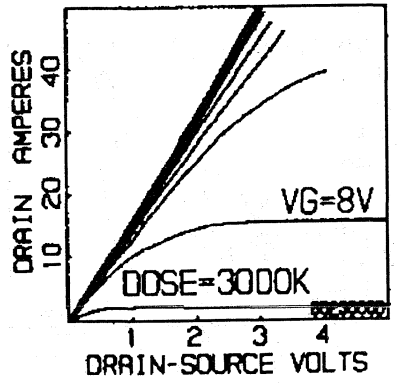
Device Bias During Irradiation (Insitu Bias) is = VG=-10, VD=160

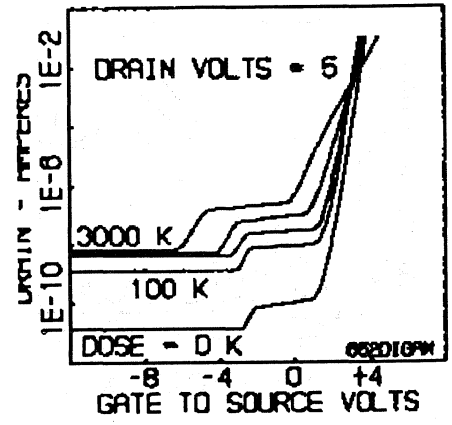












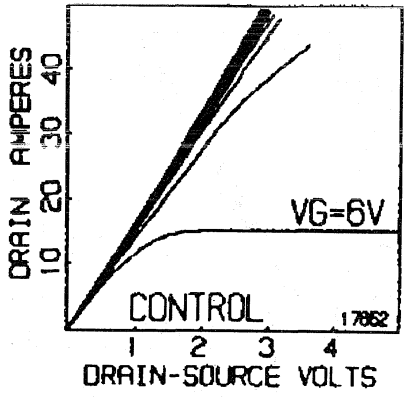
2N7293R, 2N7293H

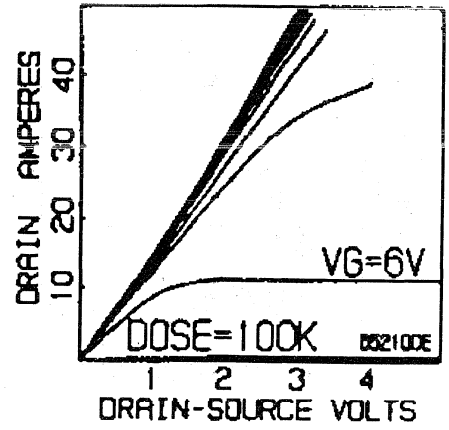
REGISTRATION PENDING

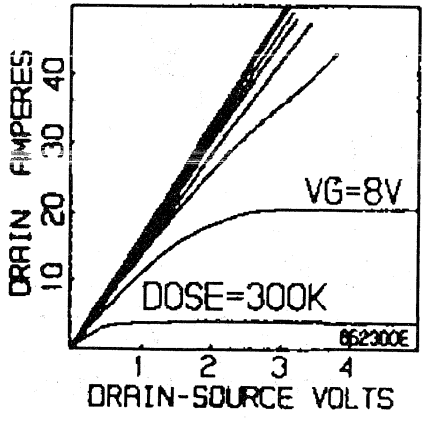
Available As FRK250 (R/H)

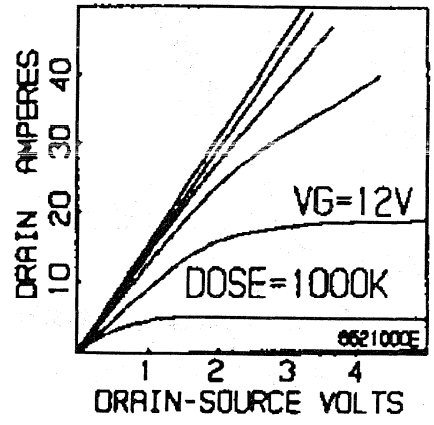
Typical Post Response Curves To Gamma (Total Dose), Cont'd.

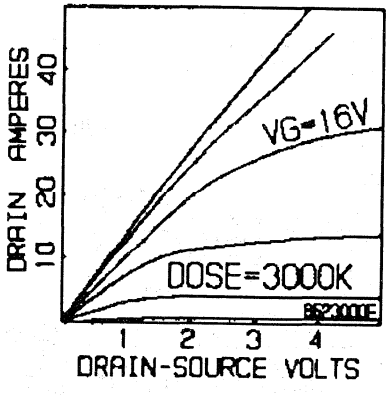
Device Bias During Irradiation (Insitu Bias) is = VG=0, VD=160

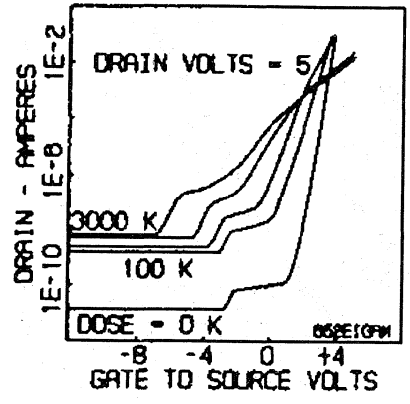












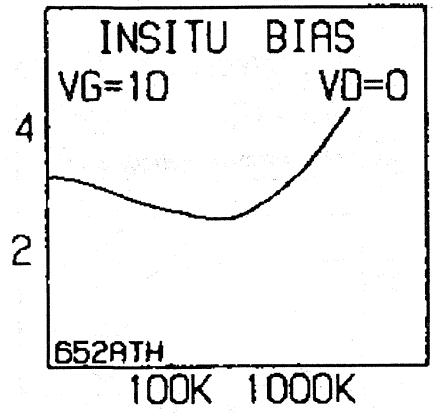
2N7293R, 2N7293H

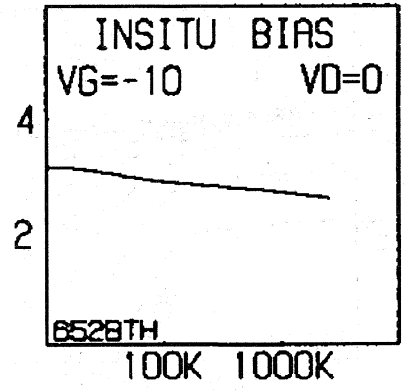
REGISTRATION PENDING

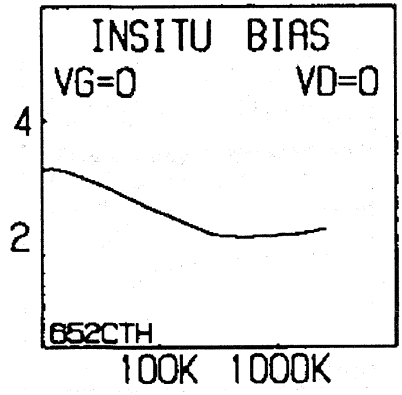
Available As FRK250 (R/H)

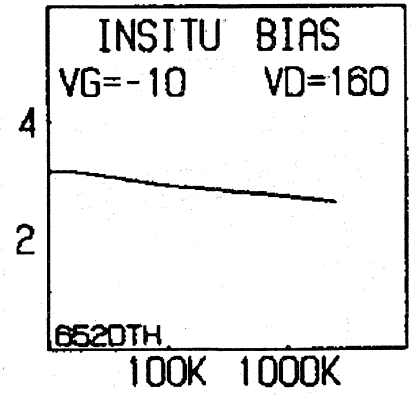
Typical Response Curves To Gamma (Total Dose)

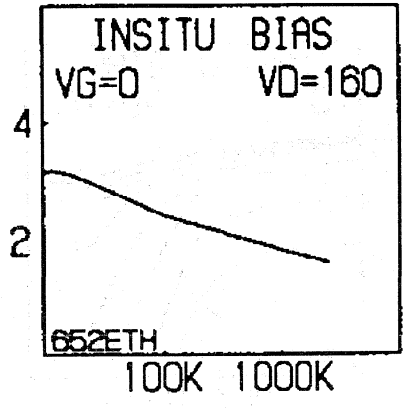
Threshold Volts VS Total Dose Rad (Si) VGS=VDS; ID=1ma





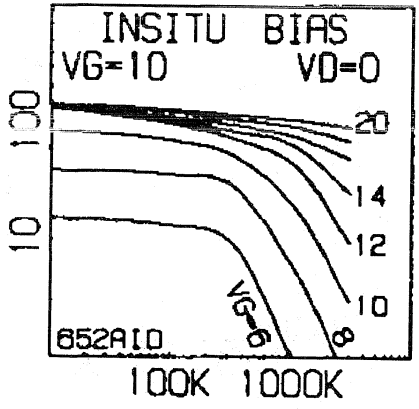


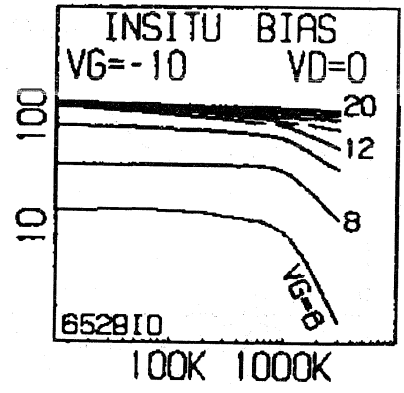


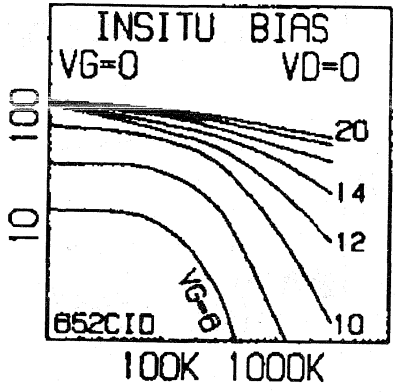


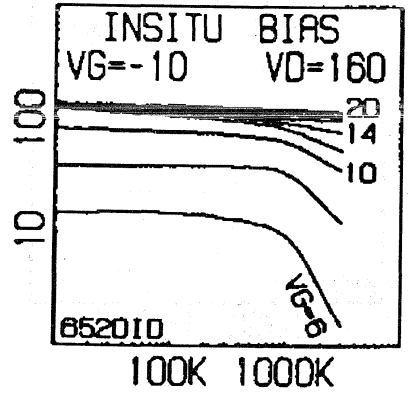
Typical Response Curves To Gamma (Total Dose), Cont'd.

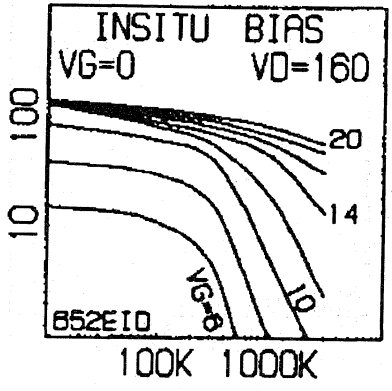
Drain Amperes IDS (on) VS Total Dose Rad (Si) VDS=VGS=6, 8, 10, 12, 14, 16, 18, 20 Volts





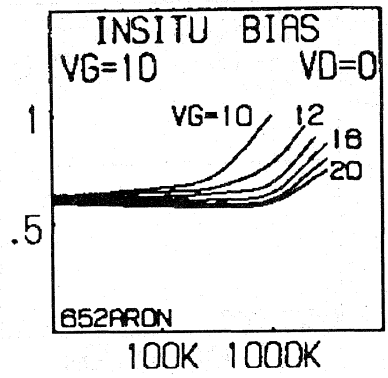


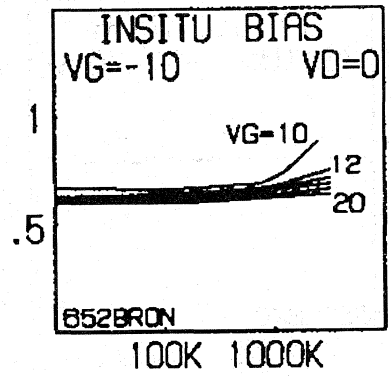


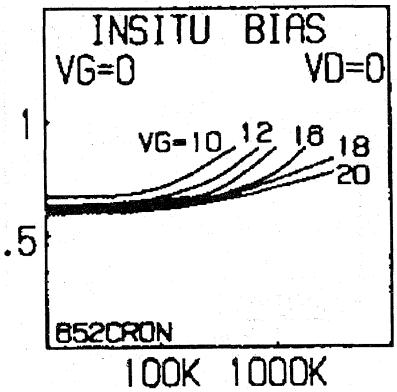


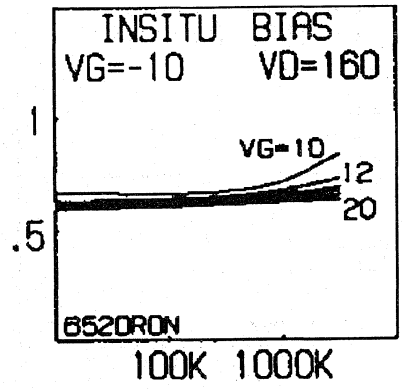
Typical Response Curves To Gamma (Total Dose), Cont'd.

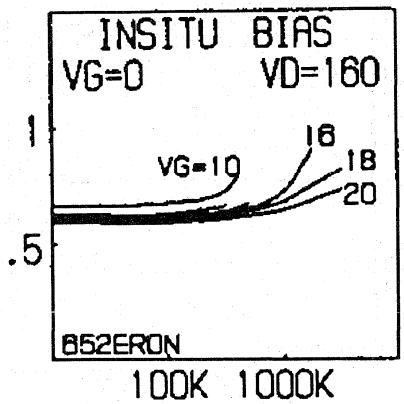
RDS (on) [Normalized to Rated RDS (on)] VS Total Dose Rad (Si) Id=27A; Vgs=10, 12, 14, 16, 18, 20 Volts











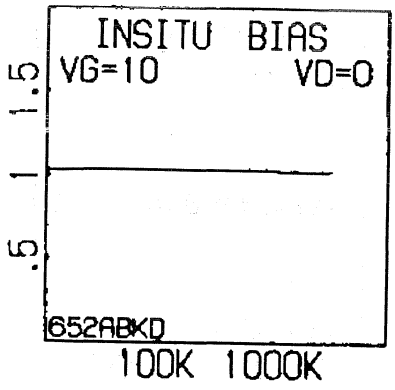
2N7293R, 2N7293H

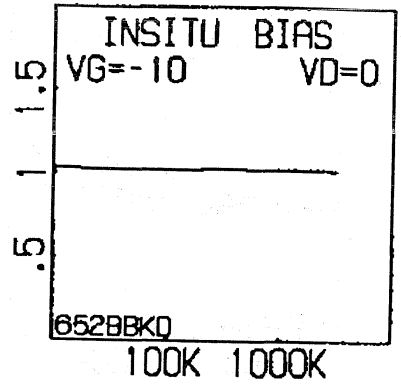
REGISTRATION PENDING

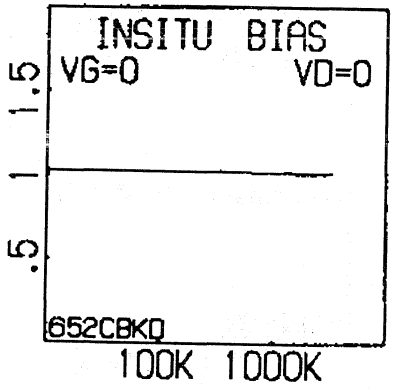
Available As FRK250 (R/H)

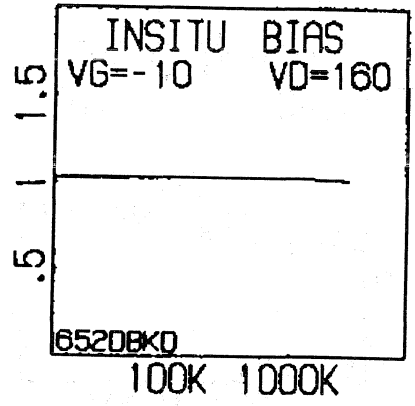
Typical Response Curves To Gamma (Total Dose), Cont'd.

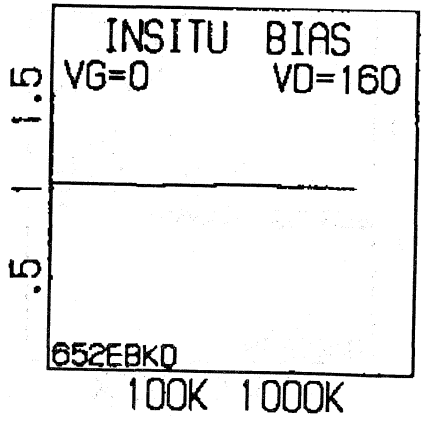
BVdss (Normalized to Rated BVdss) VS Total Dose Rad (Si) Id=1ma











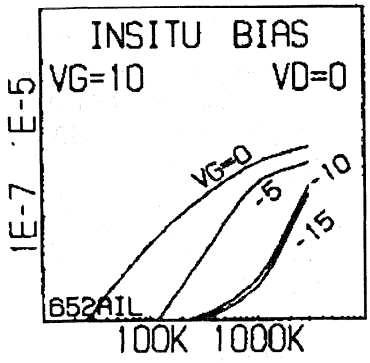
2N7293R, 2N7293H

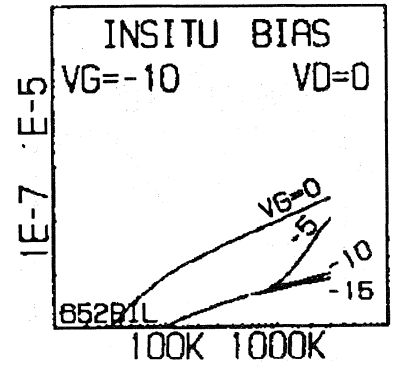
REGISTRATION PENDING

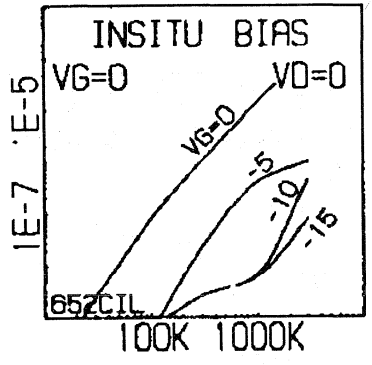
Available As FRK250 (R/H)

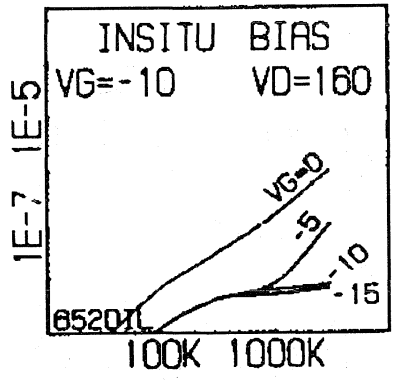
Typical Response Curves To Gamma (Total Dose), Cont'd.

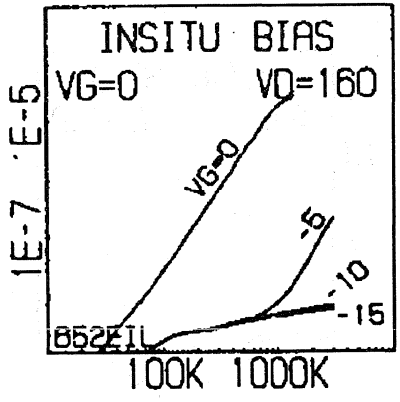
Drain Leakage Amperes VS Total Dose Rad (Si) = VGs=0, -5, -10, -15; Vds=5 Volts











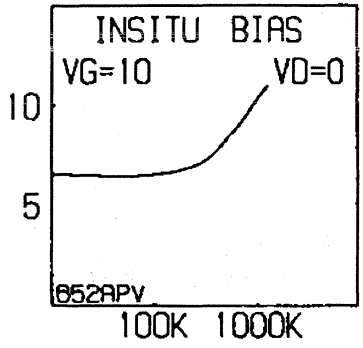
2N7293R, 2N7293H

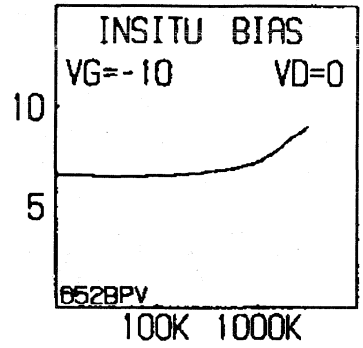
REGISTRATION PENDING

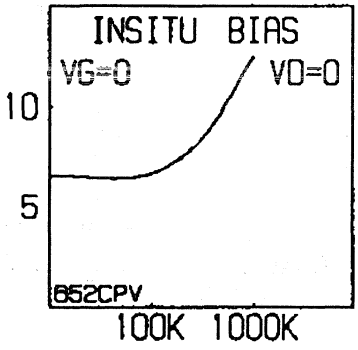
Available As FRK250 (R/H)

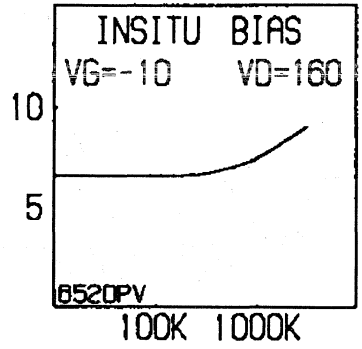
Typical Response Curves To Gamma (Total Dose), Cont'd.

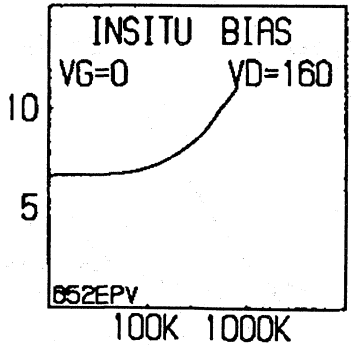
VGP Gate Plateau Volts VS Total Dose Rad (Si) Id=27A; Vd=10 Volts









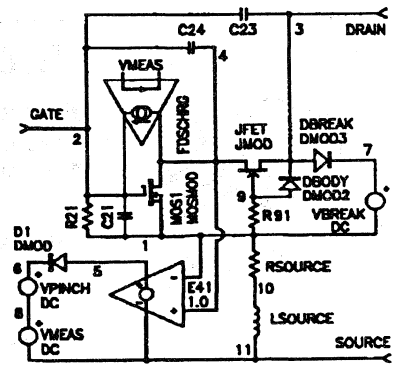


2N7293R, 2N7293H

REGISTRATION PENDING

Spice Parameters and Sub Circuit

```
.SUBCKT 2N7293 3 2 11; REV 6/14/90
R21 2 1 1E9
R91 9 1 0.00654
C21 2 1 4800p
C23 2 3 200p
C24 2 4 9400p
FDCCHRG 4 2 VMEAS 1.0
MOS1 4 2 1 1 MOSMOD L = 1u  W = 1u
JFET 3 9 4 JMOD 1
DBODY 9 3 DMOD2
RSOURCE 1 10 0.01827
LSOURCE 10 11 7.500n
E41 5 11 4 1 1.0
D1 5 6 DMOD
VPINCH 6 8 DC 8.000
VMEAS 8 11 DC 0
DBREAK 3 7 DMOD3
VBREAK 7 1 DC 240.0
.MODEL MOSMOD NMOS VTO = 4.463  KP = 12.162  TOX = 1.OE+06U
.MODEL JMOD NJF VTO = –8.000  BETA = 1216.2  IS = 8.7E-019  RD = 0.05983
.MODEL DMOD D IS = 1.OE–13  N = 0.03  RS = .001
.MODEL DMOD2 D CJO = 4200P  TT = 1000n  IS = 8.7E-013
.MODEL DMOD3 D IS = 1.OE–13  RS = .1.111  N = 1.0
.ENDS
```



Verified on PSPICE

Reference: C.F. Wheatley, Jr. H.R. Ronan, Jr. G.M. Dolny, "Spicing-Up Spice II Software For Power MOSFET Modeling", Harris Application Note AN-8610, 4-87

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

2N7294R, 2N7294H

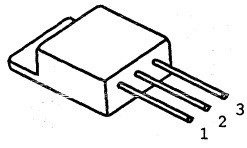
REGISTRATION PENDING

Available As FRF250R, FRF250H

23A, 200V

RDS(on)=0.115Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-254AA

Features:

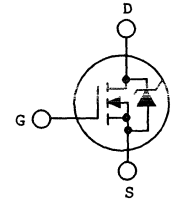
- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 µm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

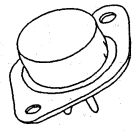
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
3Continuous Drain Current, Id @Tc = 25°C	23	A
@Tc = 100°C	15	A
Pulsed Drain Current, I_{DM}	69	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	69	A
Continuous Source Current (Body diode), Is	23	A
Pulsed Source Current (Body diode), Ism	69	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7295R, 2N7295H

REGISTRATION PENDING
Available As FRK254R, FRK254H
20A, 250V
RDS(on)=0.17Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AE

Features:

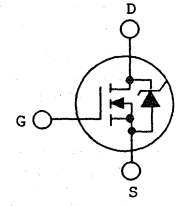
- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
3Continuous Drain Current, Id @Tc = 25°C	20	A
@Tc = 100°C	12	A
Pulsed Drain Current, I_{DM}	60	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	60	A
Continuous Source Current (Body diode), Is	20	A
Pulsed Source Current (Body diode), Ism	60	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7295R, 2N7295H

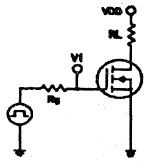
REGISTRATION PENDING

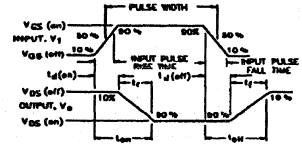
Available As FRK254 (R/H)

Pre Radiation Electrical Characteristics

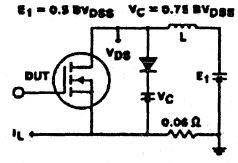
Case Temperature (Tc) = 25°C unless otherwise specified

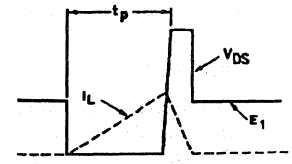
CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVdss	Vgs = 0, Id = 1mA	250	—	V
Gate-Threshold Volts	Vgs(th)	Vds = Vgs, Id = 1ma	2	4	V
Gate-Body Leakage Forward	Igssf	Vgs = +20V	—	100	nA
Gate-Body Leakage Reverse	Igssr	Vgs = −20V	—	100	nA
Zero-Gate Voltage Drain Current	Idss1 Idss2 Idss3	Vds = 250V, Vgs = 0 Vds = 200V, Vgs = 0 Vds = 0, Vgs = 0, Tc = 125°C	— — —	1 .025 .25	mA
Rated Avalanche Current	Iar	Time = 20uS	—	60	A
Drain-Source On-State Volts	Vds(on)	Vgs = 10V, Id = 20A	—	3.58	V
Drain-Source On Resistance	Rds(on)	Vgs = 10V, Id = 12A	—	.170	Ω
Turn-On Delay Time	td(on)	Vdd = 125V, Id = 20A PULSE WIDTH = 3uS PERIOD = 300mS Rg = 25Ω 0 ≤ VGS ≤ 10 (SEE TEST CIRCUIT)	—	150	nS
Rise Time	tr		—	450	
Turn-Off Delay Time	td(off)		—	650	
Fall Time	tf		—	260	
Gate-Charge Threshold	Qg(th)	Vdd = 125V, IGS1 = IGS2 Id = 20A 0 ≤ VGS ≤ 20 (SEE FIGURE)	3.5	15	nC
Gate-Charge Total	Qgm		127	510	
Gate-Charge On State	Qg(on)		63	252	
Diode Forward Voltage	Vsd	Id = 20A, Vgd = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 10A; di/dt = 100A/uS	—	2000	nS
Junction-To-Case	Rθjc	—	—	0.83	°C/W
Junction-to-Ambient	Rθja	Free Air Operation	—	30	



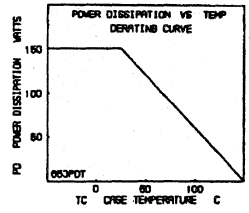


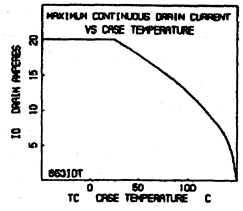
SWITCHING TIME TESTING

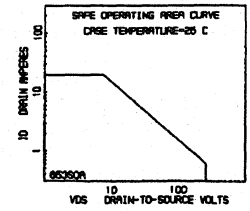




CLAMPED INDUCTIVE SWITCHING, ILM





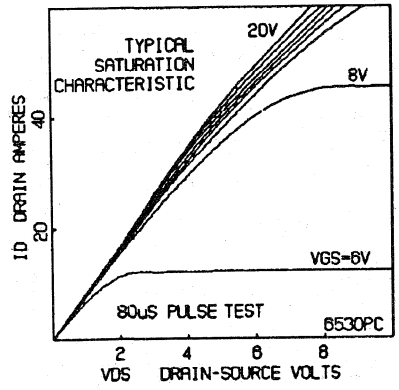


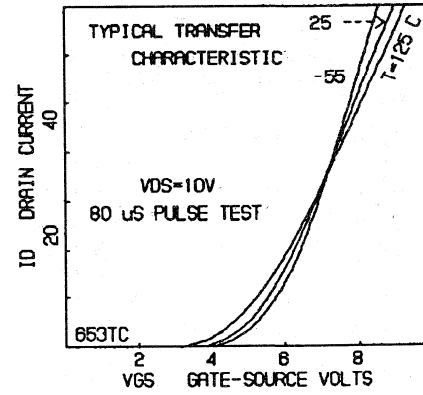
2N7295R, 2N7295H

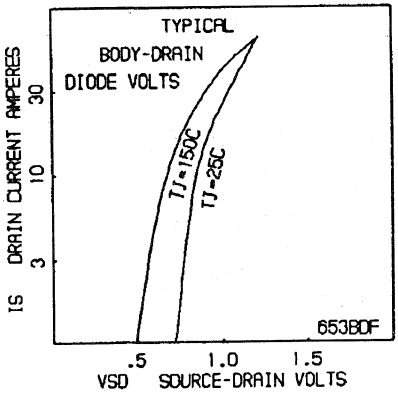
REGISTRATION PENDING

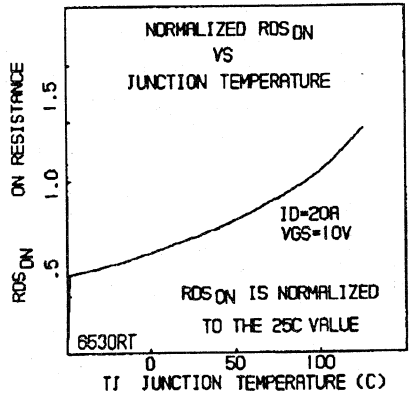
Available As FRK254 (R/H)

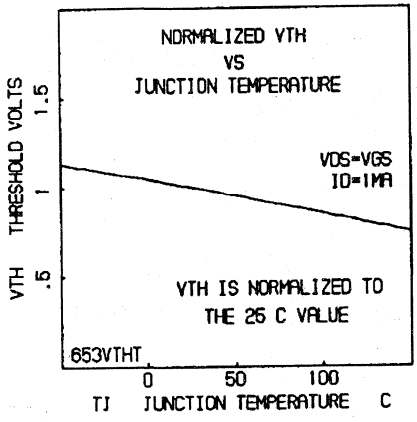
Typical Characteristics

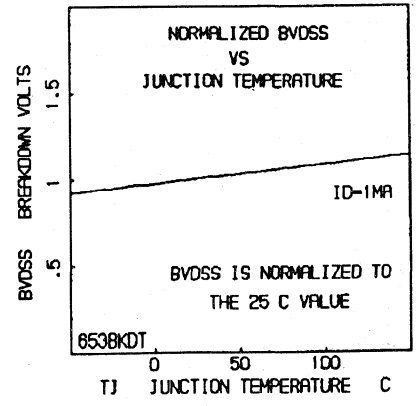










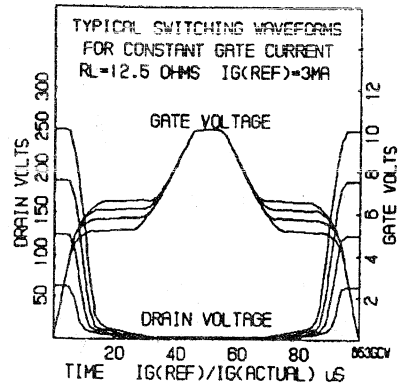


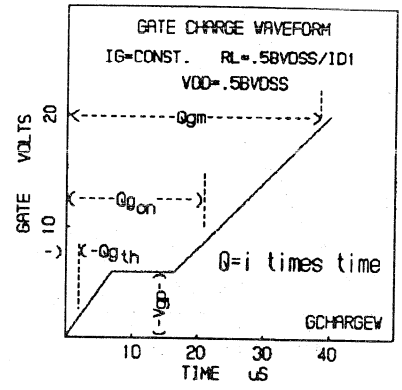
2N7295R, 2N7295H

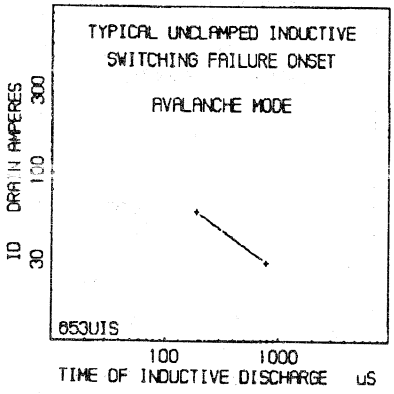
REGISTRATION PENDING

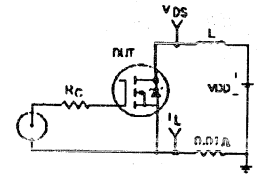
Available As FRK254 (R/H)

Typical Characteristics, Cont'd.

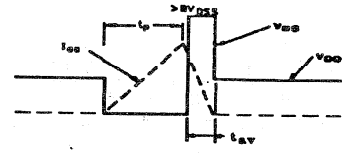


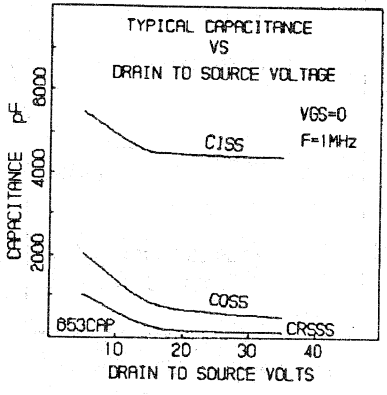


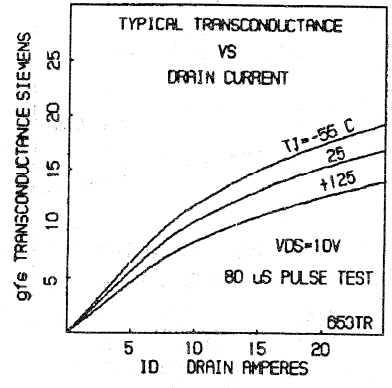




UNCLAMPED INDUCTIVE SWITCHING







2N7295R, 2N7295H

REGISTRATION PENDING

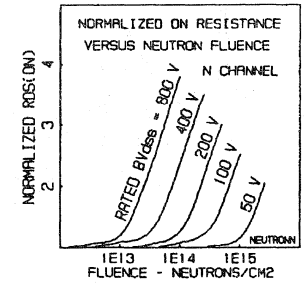
Available As FRK254 (R/H)

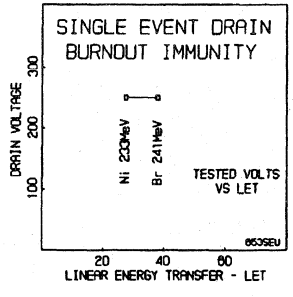
Post Radiation Electrical Characteristics

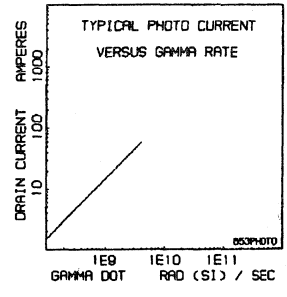
Case Temperature (Tc) = 25°C unless otherwise specified

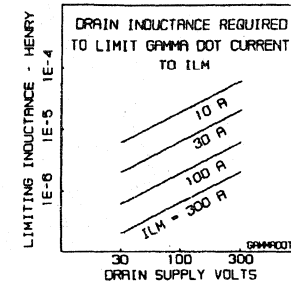
CHARACTERISTIC		TYPE	NOTES	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVdss	2N7295R	4, 6	Vgs = 0, Id = 1mA	100	—	V
		2N7295H	5, 6		95	—	
Gate Source Threshold Volts	Vgs(th)	2N7295R	4, 6	Vgs = Vds, Id = 1mA	2	4	V
		2N7295H	3, 5, 6		1.5	4.5	
Gate-Body Leakage Forward	Igssf	2N7295R	4, 6	Vgs = 20, Vds = 0	—	100	nA
		2N7295H	5, 6		—	200	
Gate-Body Leakage Reverse	Igssr	2N7295R	2, 4, 6	Vgs = −20V, Vds = 0	—	100	nA
		2N7295H	2, 5, 6		—	200	
Zero-Gate Voltage Drain Current	Idss	2N7295R	4, 6	Vgs = 0, Vds = 200V	—	25	µA
		2N7295H	5, 6		—	100	
Drain-Source On-State Volts	Vds(on)	2N7295R	1, 4, 6	Vgs = 10, Id = 20A	—	3.58	V
		2N7295H	1, 5, 6	Vgs = 16, Id = 20A	—	3.58	
Drain-Source On Resistance	Rds(on)	2N7295R	1, 4, 6	Vgs = 10, Id = 12A	—	.170	Ω
		2N7295H	1, 5, 6	Vgs = 14, ID = 12A	—	.215	

NOTES: (1) Pulse test, 300us max
(2) Absolute value
(3) Gamma = 300KRad(Si)
(4) Gamma = 100KRad(Si) and/or Neutron = 3E13
(5) Gamma = 1000KRad(Si) and/or Neutron = 3E13
(6) Insitu Gamma bias must be sampled for both
Vgs = +12V, Vds = 0V and
Vgs = 0V, Vds = 80% BVdss
(7) Gamma data taken 11/1/89 on TA17653 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
(8) Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
(9) Neutron derivation, HARRIS Application note AN-8831, Oct, 1988









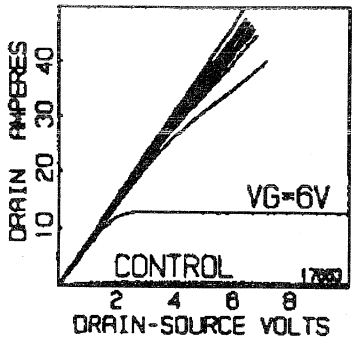
2N7295R, 2N7295H

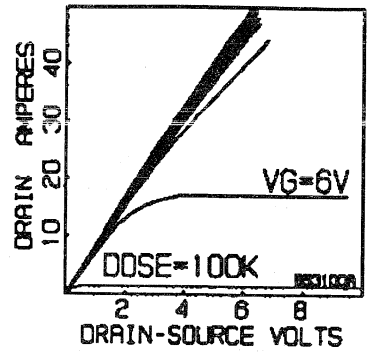
REGISTRATION PENDING

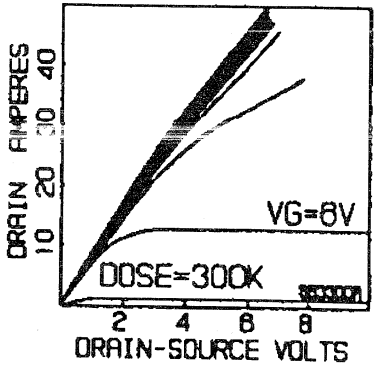
Available As FRK254 (R/H)

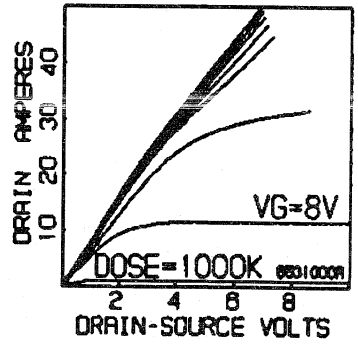
Typical Post Response Curves to Gamma (Total Dose), Cont'd.

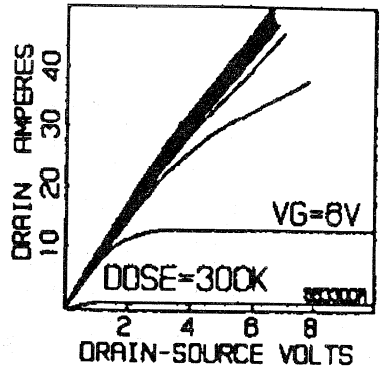
Device Bias During Irradiation (Insitu Bias) is = VG = +10, VD = 0

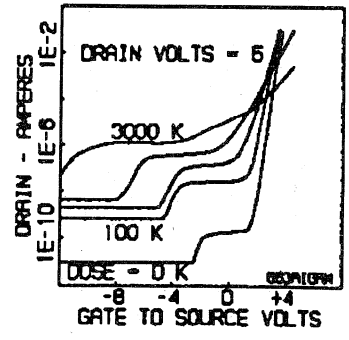






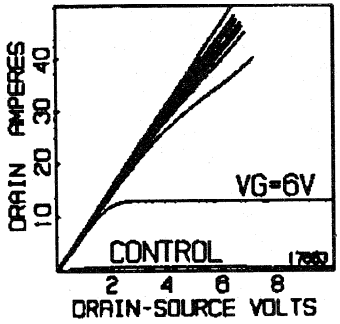


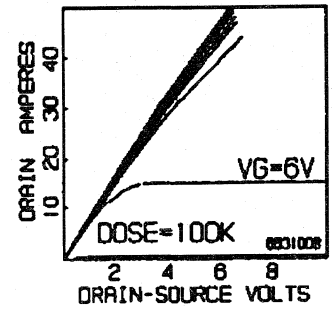


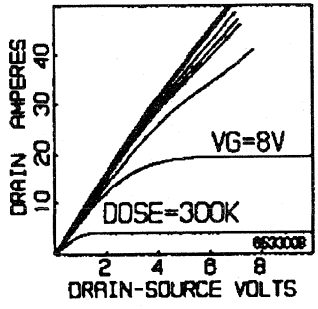


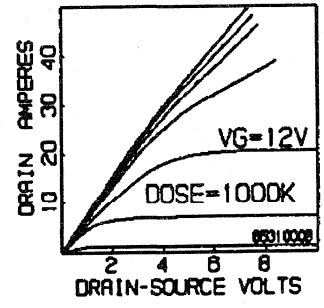
Typical Post Response Curves to Gamma (Total Dose), Cont'd.

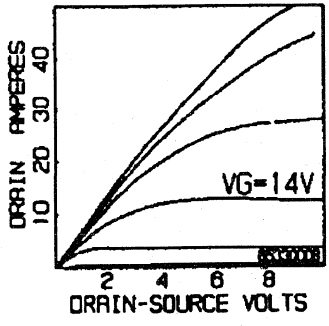
Device Bias During Irradiation (Insitu Bias) is = VG = -10, VD = 0

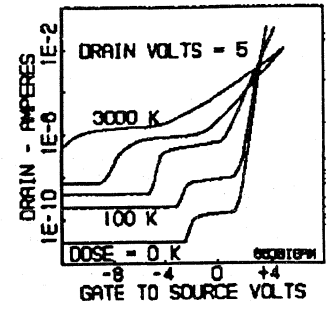












2N7295R, 2N7295H

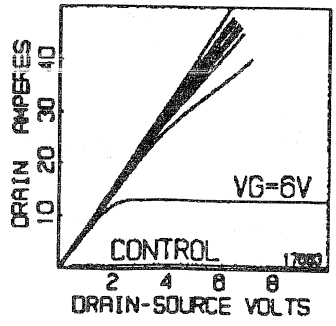
REGISTRATION PENDING

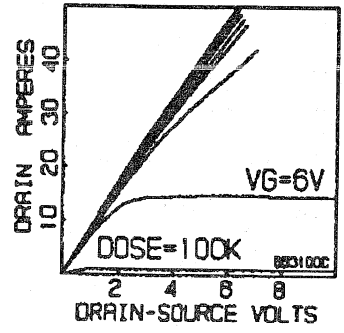
Available As FRK254 (R/H)

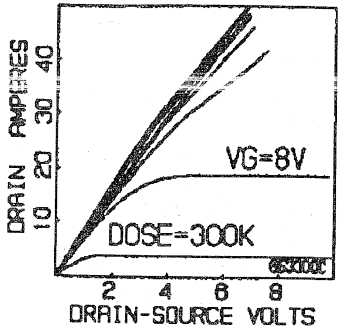
Typical Post Response Curves to Gamma (Total Dose), Cont'd.

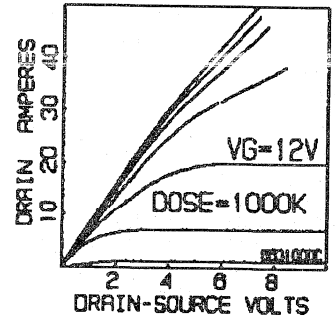
Device Bias During Irradiation (Insitu Bias) is = VG = 0, VD = 0

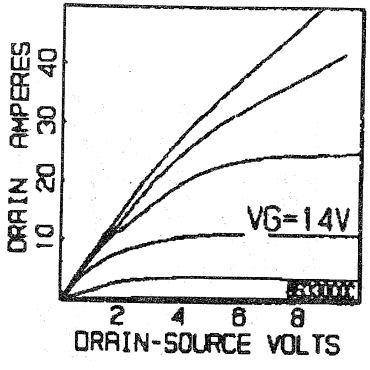
VG=0, VD=0

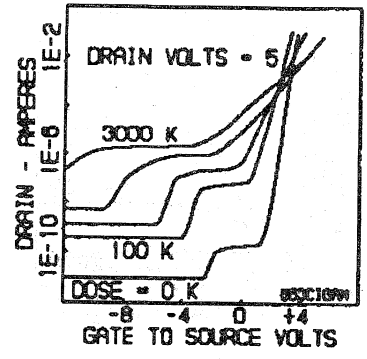






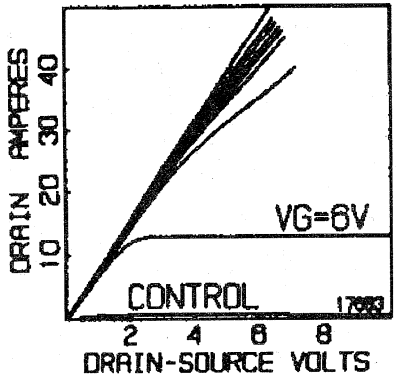


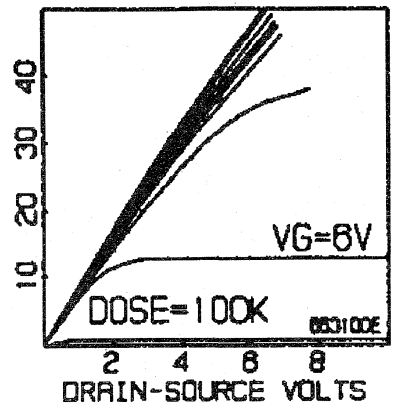


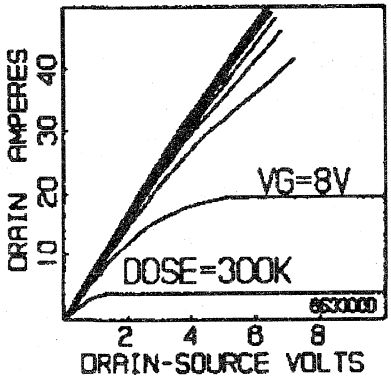


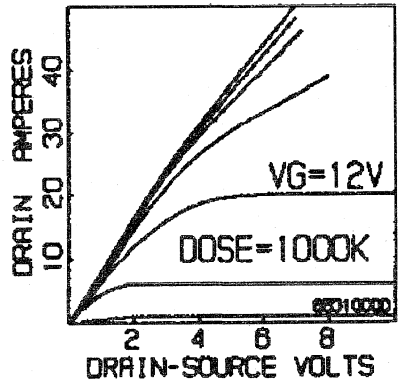
Typical Post Response Curves to Gamma (Total Dose), Cont'd.

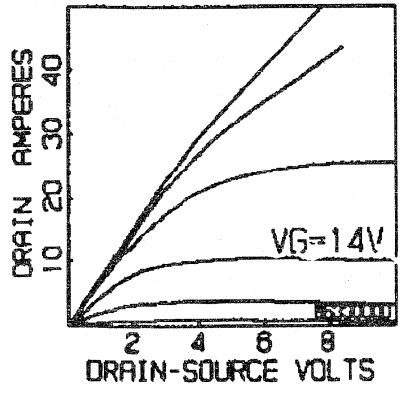
Device Bias During Irradiation (Insitu Bias) is = VG = -10, VD = 200

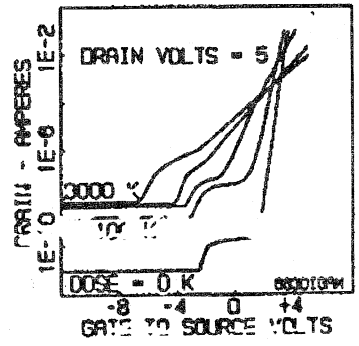












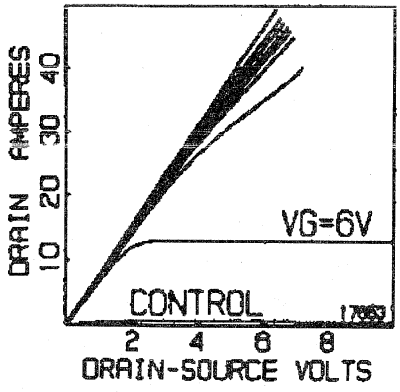
2N7295R, 2N7295H

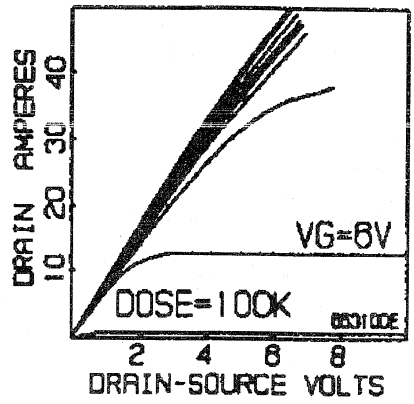
REGISTRATION PENDING

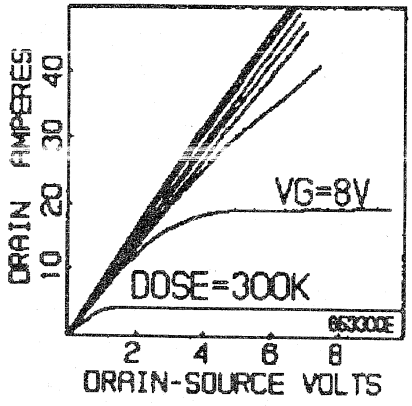
Available As FRK254 (R/H)

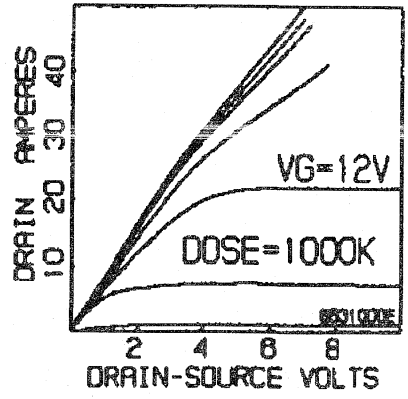
Typical Post Response Curves to Gamma (Total Dose), Cont'd.

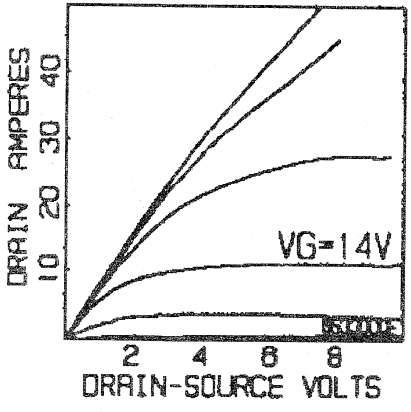
Device Bias During Irradiation (Insitu Bias) is = VG = 0, VD = 200

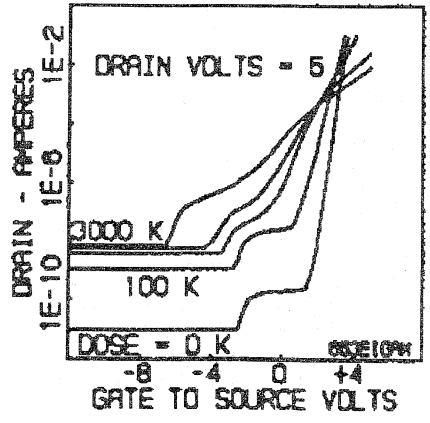












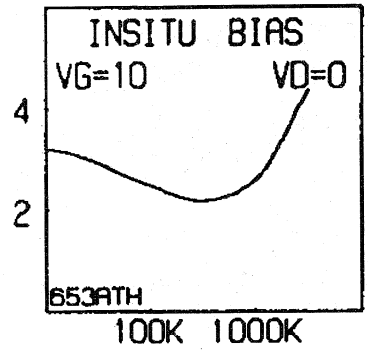
2N7295R, 2N7295H

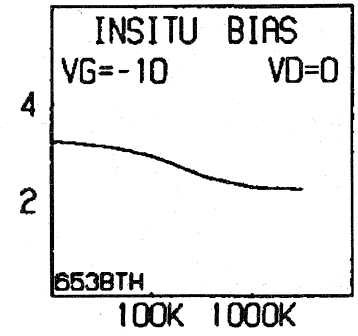
REGISTRATION PENDING

Available As FRK254 (R/H)

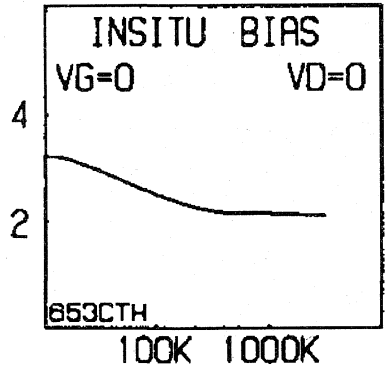
Typical Response Curves to Gamma (Total Dose)

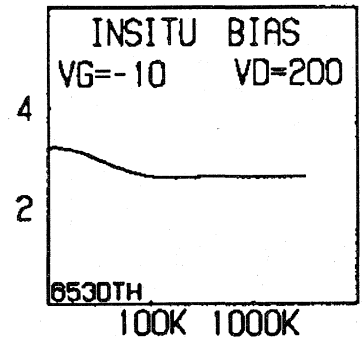
Threshold Volts VS Total Dose RAD (Si) = VGS = VDS, ID = 1ma

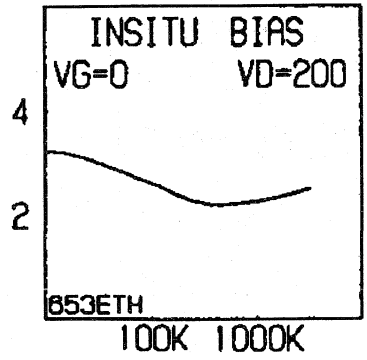




THRESHOLD VOL







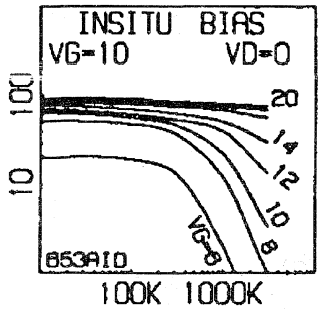
2N7295R, 2N7295H

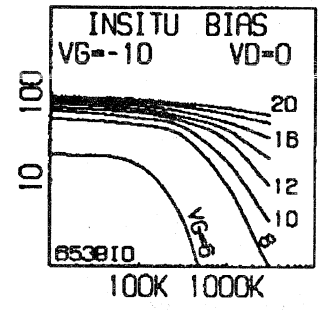
REGISTRATION PENDING

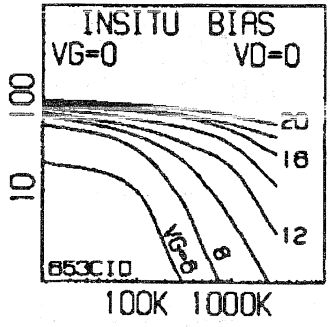
Available As FRK254 (R/H)

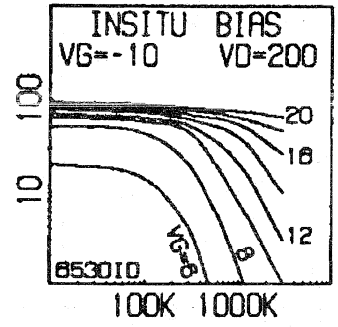
Typical Response Curves to Gamma (Total Dose), Cont'd.

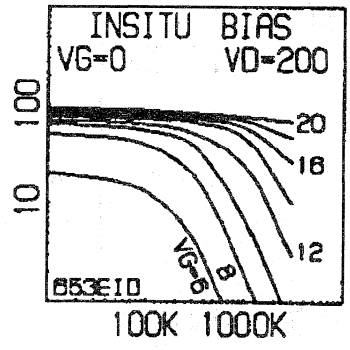
Drain Amperes IDS (on) VS Total Dose Rad (Si) = VDS = VGS = 6, 8, 10, 12, 14, 16, 18, 20 VOLTS











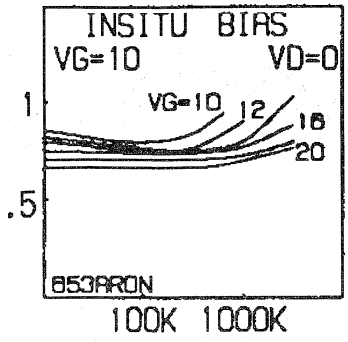
2N7295R, 2N7295H

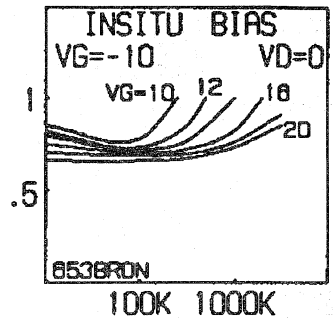
REGISTRATION PENDING

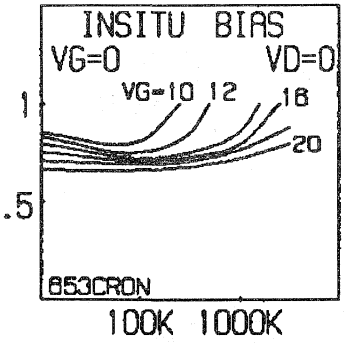
Available As FRK254 (R/H)

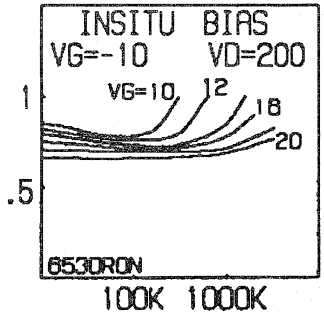
Typical Response Curves to Gamma (Total Dose), Cont'd.

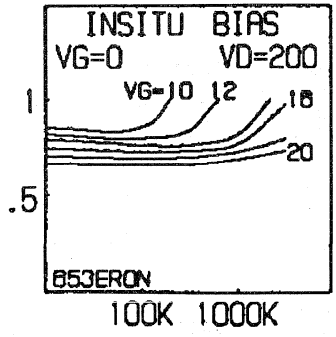
RDS (on) [Normalized to Rated RDS (on)] VS Total Dose RAD (Si) = Id = 20A; Vgs = 10, 12, 14, 16, 18, 20 Volts











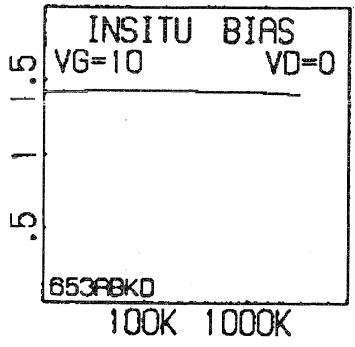
2N7295R, 2N7295H

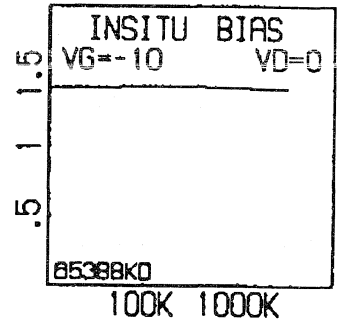
REGISTRATION PENDING

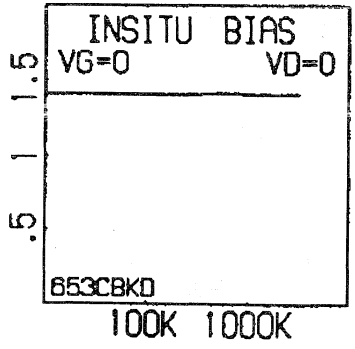
Available As FRK254 (R/H)

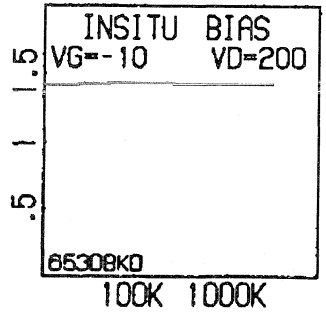
Typical Response Curves to Gamma (Total Dose), Cont'd.

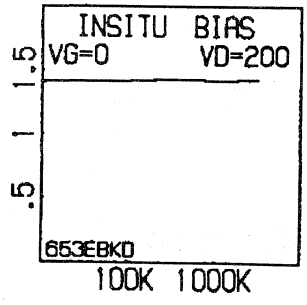
BVdss (Normalized To Rated Bvdss) VS Total Dose Rad (Si) Id = 1mA











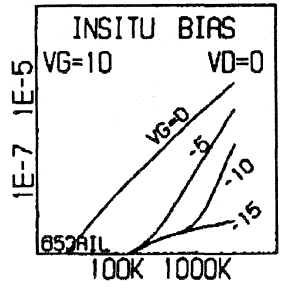
2N7295R, 2N7295H

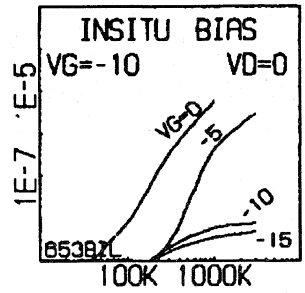
REGISTRATION PENDING

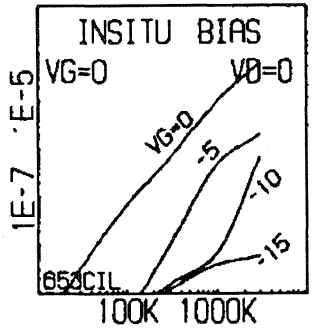
Available As FRK254 (R/H)

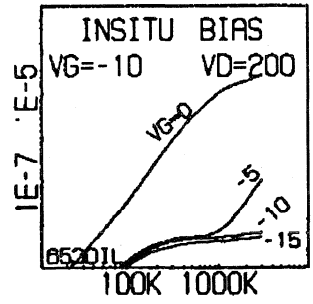
Typical Response Curves to Gamma (Total Dose), Cont'd.

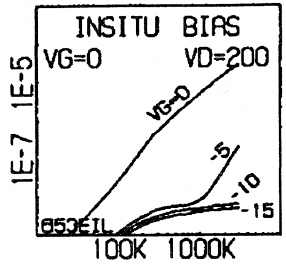
Drain Leakage Amperes vs Total Dose Rad(Si) Vgs=0,-5,-10;Vds=5 Volts











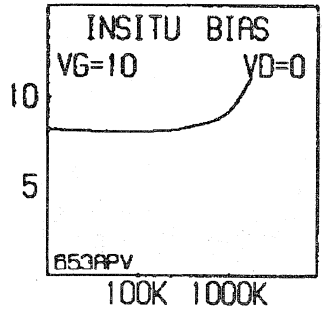
2N7295R, 2N7295H

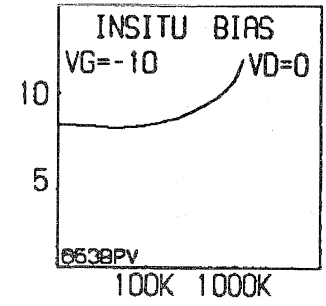
REGISTRATION PENDING

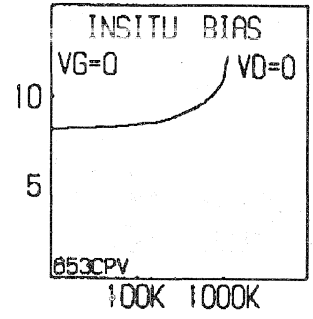
Available As FRK254 (R/H)

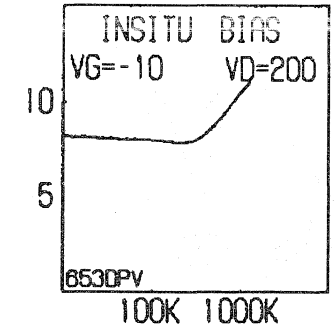
Typical Response Curves to Gamma (Total Dose), Cont'd.

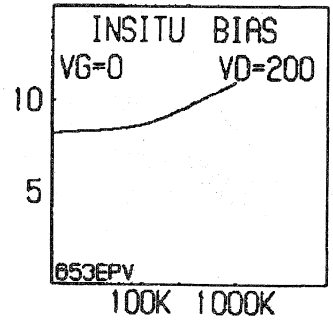
VGP Gate Plateau Volts vs Total Dose Rad(Si) Id=20A; Vd=10 Volts











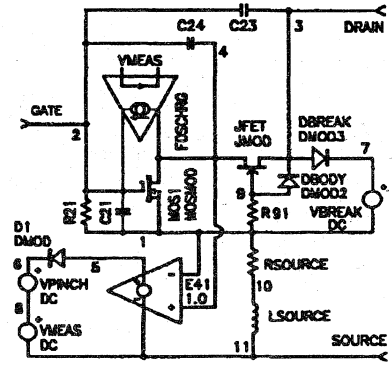
2N7295R, 2N7295H

REGISTRATION PENDING

OFFERED AS FRK254(R/H)

Spice Parameters and Sub Circuit

```
.SUBCKT FRK250 3 2 11; REV 6/15/90
R21 2 1 1E9
R91 9 1 0.00654
C21 2 1 4800p
C23 2 3 200p
C24 2 4 9400p
FDCHRG 4 2 VMEAS 1.0
MOS1 4 2 1 1 mosmod L = 1u  W = 1u
JFET 3 9 4 JMOD 1
DBODY 9 3 DMOD2
RSOURCE 1 10 0.01827
LSOURCE 10 11 7.500n
E41 5 11 4 1 1.0
D1 5 6 DMOD
VPINCH 6 8 DC 8.000
VMEAS 8 11 DC 0
DBREAK 3 7 DMOD3
VBREAK 7 1 DC 240.0
.MODEL MOSMOD NMOS VTO = 4.463  KP = 12.162  TOX = 1.OE+06U
.MODEL JMOD NJF VTO = 8.000  BETA = 1216.2  IS = 8.7E-019  RD = 0.05983
.MODEL DMOD D IS = 1.OE-13  N = 0.03  RS = .001
.MODEL DMOD2 D CJO = 4200p  TT = 1000n  IS = 8.7E-013
.MODEL DMOD3 D IS = 1.OE-13  RS = 1.111  N = 1.0
.ENDS
```



Verified on PSPICE

Reference: C.F. Wheatley, Jr., H.R. Ronan, Jr., G.M. Dolny, "Spicing-Up Spice II Software For Power MOSFET Modeling", Harris Application Note AN-8610, 4-87

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

2N7296R, 2N7296H

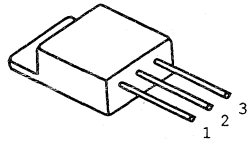
REGISTRATION PENDING

Available As FRF254R, FRF254H

17A, 250V

RDS(on)=0.185Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-254AA

Features:

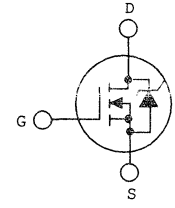
- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

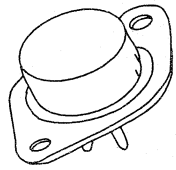
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
3Continuous Drain Current, Id @Tc = 25°C	17	A
@Tc = 100°C	11	A
Pulsed Drain Current, I_{DM}	51	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	51	A
Continuous Source Current (Body diode), Is	17	A
Pulsed Source Current (Body diode), Ism	51	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY 2N7297R, 2N7297H

REGISTRATION PENDING
Available As FRM450R, FRM450H
10A, 500V
RDS(on)=0.60Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AA

Features:

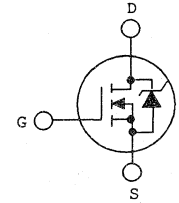
- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	500	V
3Continuous Drain Current, Id @Tc = 25°C	10	A
@Tc = 100°C	6	A
Pulsed Drain Current, I_{DM}	30	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	30	A
Continuous Source Current (Body diode), Is	10	A
Pulsed Source Current (Body diode), Ism	30	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

PRELIMINARY 2N7298R, 2N7298H

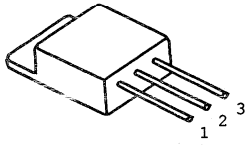
REGISTRATION PENDING

Available As FRF450R, FRF450H

9A, 500V

RDS(on)=0.615Ω

Radiation-Hardened N-Channel Power MOSFETs



TO-254AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

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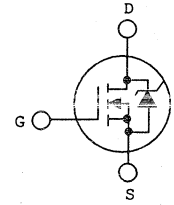


SYMBOL

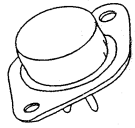
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	500	V
3Continuous Drain Current, Id @Tc = 25°C	9	A
@Tc = 100°C	6	A
Pulsed Drain Current, I_{DM}	27	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	27	A
Continuous Source Current (Body diode), Is	9	A
Pulsed Source Current (Body diode), Ism	27	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7299R, 2N7299H

REGISTRATION PENDING
Available As FRK160R, FRK160H
66A, 100V
RDS(on)=0.04Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AE

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
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The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

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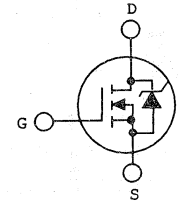

SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	100	V
3Continuous Drain Current, Id @Tc = 25°C	66	A
@Tc = 100°C	42	A
Pulsed Drain Current, I_{DM}	100	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	100	A
Continuous Source Current (Body diode), Is	66	A
Pulsed Source Current (Body diode), Ism	100	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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2N7301R, 2N7301H

REGISTRATION PENDING

Available As FRK260R, FRK260H

46A, 200V

RDS(on)=0.07Ω

Radiation-Hardened N-Channel Power MOSFETs

TO–204AE

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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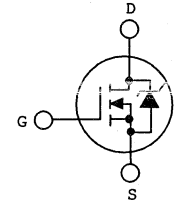


SYMBOL

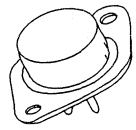
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	200	V
3Continuous Drain Current, Id @Tc = 25°C	46	A
@Tc = 100°C	29	A
Pulsed Drain Current, I_{DM}	100	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	100	A
Continuous Source Current (Body diode), Is	46	A
Pulsed Source Current (Body diode), Ism	100	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7303R, 2N7303H

REGISTRATION PENDING
Available As FRK264R, FRK264H
34A, 250V
RDS(on)=0.12Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AE

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

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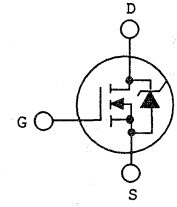

SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	250	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	250	V
3Continuous Drain Current, Id @Tc = 25°C	34	A
@Tc = 100°C	21	A
Pulsed Drain Current, I_{DM}	100	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	100	A
Continuous Source Current (Body diode), Is	34	A
Pulsed Source Current (Body diode), Ism	100	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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PRELIMINARY

2N7305R, 2N7305H

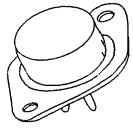
REGISTRATION PENDING

Available As FRK460R, FRK460H

17A, 500V

RDS(on)=0.40Ω

Radiation-Hardened N-Channel Power MOSFETs



TO–204AE

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/dose typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 µm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

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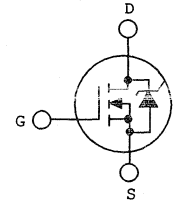


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	500	V
3Continuous Drain Current, Id @Tc = 25°C	17	A
@Tc = 100°C	11	A
Pulsed Drain Current, I_{DM}	51	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	51	A
Continuous Source Current (Body diode), Is	17	A
Pulsed Source Current (Body diode), Ism	51	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7307R, 2N7307H

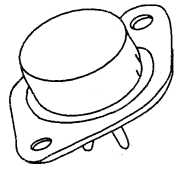
REGISTRATION PENDING

Available As FRM9130R, FRM9130H

6A, –100V

RDS(on)=0.55Ω

Radiation-Hardened P-Channel Power MOSFETs



TO–204AA

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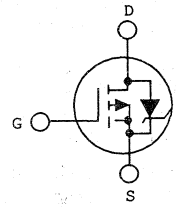
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–100	V
3Continuous Drain Current, Id @Tc = 25°C	6	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	18	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	18	A
Continuous Source Current (Body diode), Is	6	A
Pulsed Source Current (Body diode), Ism	18	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

2N7308R, 2N7308H

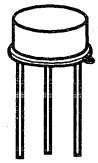
REGISTRATION PENDING

Available As FRL9130R, FRL9130H

5A, –100V

RDS(on)=0.55Ω

Radiation-Hardened P-Channel Power MOSFETs



JEDEC TO–205AF

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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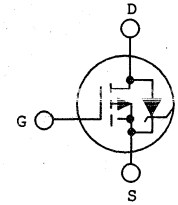


SYMBOL

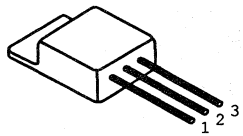
Maximum Ratings, *Absolute-Maximum Values (T_C = 25°C):*

Drain-Source Voltage, V_{DS}	–100	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	–100	V
3Continuous Drain Current, Id @Tc = 25°C	5	A
@Tc = 100°C	3	A
Pulsed Drain Current, I_{DM}	15	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	15	A
Continuous Source Current (Body diode), Is	5	A
Pulsed Source Current (Body diode), Ism	15	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY 2N7309R, 2N7309H

REGISTRATION PENDING
Available As FRS9130R, FRS9130H
6A, –100V
RDS(on)=0.565Ω

Radiation-Hardened P-Channel Power MOSFETs



TO-257AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
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The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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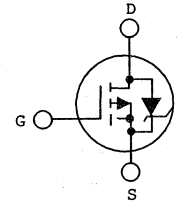


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–100	V
3Continuous Drain Current, Id @Tc = 25°C	6	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	18	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	18	A
Continuous Source Current (Body diode), Is	6	A
Pulsed Source Current (Body diode), Ism	18	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

2N7310R, 2N7310H

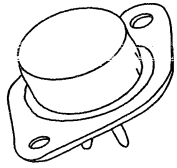
REGISTRATION PENDING

Available As FRM9230R, FRM9230H

4A, –200V

RDS(on)=1.30Ω

Radiation-Hardened P-Channel Power MOSFETs



TO–204AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
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The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

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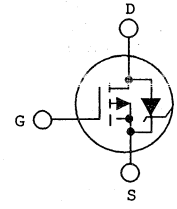

SYMBOL

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
3Continuous Drain Current, Id @Tc = 25°C	4	A
@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}	12	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	12	A
Continuous Source Current (Body diode), Is	4	A
Pulsed Source Current (Body diode), Ism	12	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
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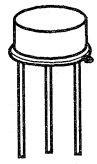
2N7311R, 2N7311H

REGISTRATION PENDING
Available As FRL9230R, FRL9230H
3A, –200V
RDS(on)=1.30Ω

Radiation-Hardened P-Channel Power MOSFETs



JEDEC TO–205AF

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
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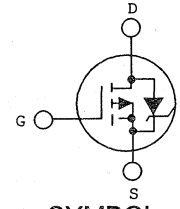
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
3Continuous Drain Current, Id @Tc = 25°C	3	/A
@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}	9	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	9	A
Continuous Source Current (Body diode), Is	3	A
Pulsed Source Current (Body diode), Ism	9	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
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PRELIMINARY 2N7312R, 2N7312H

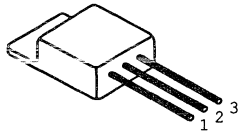
REGISTRATION PENDING

Available As FRS9230R, FRS9230H

4A, –200V

RDS(on)=1.32Ω

Radiation-Hardened P-Channel Power MOSFETs



TO-257AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
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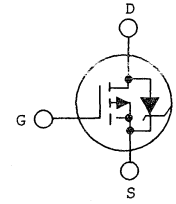

SYMBOL

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
3Continuous Drain Current, Id @Tc = 25°C	4	A
@Tc = 100°C	2	A
Pulsed Drain Current, I_{DM}	12	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
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Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	12	A
Continuous Source Current (Body diode), Is	4	A
Pulsed Source Current (Body diode), Ism	12	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
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OBJECTIVE 2N7313R, 2N7313H

REGISTRATION PENDING

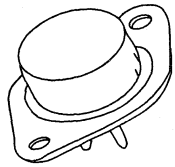
Available As FRM9430R, FRM9430H

1.5A, –500V

RDS(on)=7.60Ω

This Objective Data Sheet Represents the Proposed Device Performance.

Radiation-Hardened P-Channel Power MOSFETs



TO–204AA

Features:

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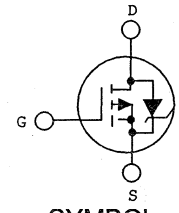

SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
3Continuous Drain Current, Id @Tc = 25°C	1.5	A
@Tc = 100°C	1	A
Pulsed Drain Current, I_{DM}	4.5	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	4.5	A
Continuous Source Current (Body diode), Is	1.5	A
Pulsed Source Current (Body diode), Ism	4.5	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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OBJECTIVE 2N7314R, 2N7314H

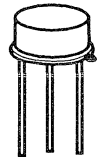
REGISTRATION PENDING

Available As FRL9430R, FRL9430H

1A, –500V

RDS(on)=7.60Ω

This Objective Data Sheet Represents the Proposed Device Performance.



JEDEC TO–205AF

Radiation-Hardened P-Channel Power MOSFETs

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 µm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

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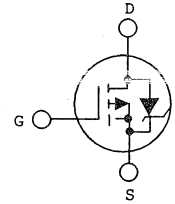


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
3Continuous Drain Current, Id @Tc = 25°C	1	A
@Tc = 100°C	0.5	A
Pulsed Drain Current, I_{DM}	3	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	25	W
At Tc = 100°C	10	W
Derated above 25°C	0.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	3	A
Continuous Source Current (Body diode), Is	1	A
Pulsed Source Current (Body diode), Ism	3	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): TL		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

OBJECTIVE 2N7315R, 2N7315H

REGISTRATION PENDING

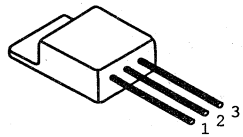
Available As FRS9430R, FRS9430H

1.5A, –500V

RDS(on)=7.62Ω

This Objective Data Sheet Represents the Proposed Device Performance.

Radiation-Hardened P-Channel Power MOSFETs



TO-257AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

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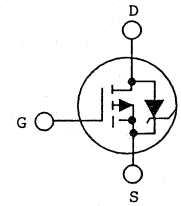

SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
3Continuous Drain Current, Id @Tc = 25°C	1.5	A
@Tc = 100°C	1	A
Pulsed Drain Current, I_{DM}	4.5	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	50	W
At Tc = 100°C	20	W
Derated above 25°C	0.40	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	4.5	A
Continuous Source Current (Body diode), Is	1.5	A
Pulsed Source Current (Body diode), Ism	4.5	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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2N7316R, 2N7316H

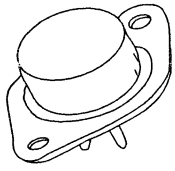
REGISTRATION PENDING

Available As FRM9140R, FRM9140H

11A, –100V

RDS(on)=0.30Ω

Radiation-Hardened P-Channel Power MOSFETs



TO–204AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
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- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
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- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
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- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

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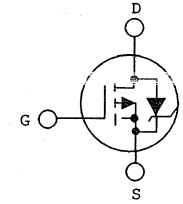


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

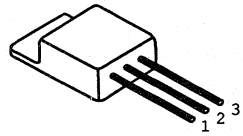
Drain-Source Voltage, V_{DS}	–100	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	–100	V
3Continuous Drain Current, Id @Tc = 25°C	11	A
@Tc = 100°C	7	A
Pulsed Drain Current, I_{DM}	33	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	33	A
Continuous Source Current (Body diode), Is	11	A
Pulsed Source Current (Body diode), Ism	33	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

PRELIMINARY

2N7317R, 2N7317H

REGISTRATION PENDING
Available As FRS9140R, FRS9140H
11A, –100V
RDS(on)=0.315Ω

Radiation-Hardened P-Channel Power MOSFETs



TO-257AA

Features:

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- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
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- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 uμm at 80% BVDSS.

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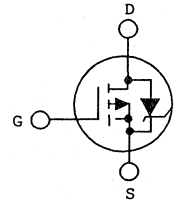

SYMBOL

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–100	V
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3Continuous Drain Current, Id @Tc = 25°C	11	A
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Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
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Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	33	A
Continuous Source Current (Body diode), Is	11	A
Pulsed Source Current (Body diode), Ism	33	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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2N7318R, 2N7318H

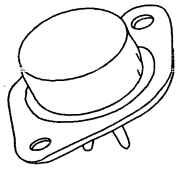
REGISTRATION PENDING

Available As FRM9240R, FRM9240H

7A, –200V

RDS(on)=0.72Ω

Radiation-Hardened P-Channel Power MOSFETs



TO–204AA

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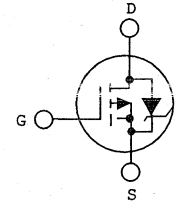

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
3Continuous Drain Current, Id @Tc = 25°C	7	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	21	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	21	A
Continuous Source Current (Body diode), Is	7	A
Pulsed Source Current (Body diode), Ism	21	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

PRELIMINARY 2N7319R, 2N7319H

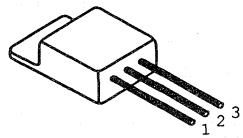
REGISTRATION PENDING

Available As FRS9240R, FRS9240H

7A, –200V

RDS(on)=0.735Ω

Radiation-Hardened P-Channel Power MOSFETs



TO-257AA

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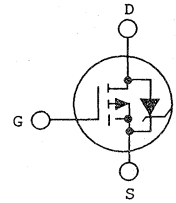

SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (R_{GS} = 20 kΩ)	–200	V
3Continuous Drain Current, Id @Tc = 25°C	7	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	21	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	21	A
Continuous Source Current (Body diode), Is	7	A
Pulsed Source Current (Body diode), Ism	21	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
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OBJECTIVE 2N7320R, 2N7320H

REGISTRATION PENDING

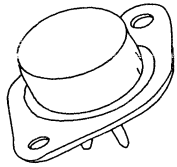
Available As FRM9440R, FRM9440H

2.5A, –500V

RDS(on)=4.20Ω

This Objective Data Sheet Represents the Proposed Device Performance.

Radiation-Hardened P-Channel Power MOSFETs



TO–204AA

Features:

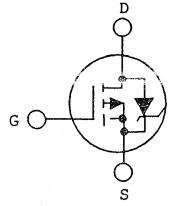
- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 µm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
3Continuous Drain Current, Id @Tc = 25°C	2.5	A
@Tc = 100°C	1.5	A
Pulsed Drain Current, I_{DM}	7.5	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, PT: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	7.5	A
Continuous Source Current (Body diode), Is	2.5	A
Pulsed Source Current (Body diode), Ism	7.5	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): TL		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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OBJECTIVE 2N7321R, 2N7321H

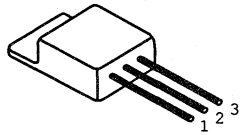
REGISTRATION PENDING

Available As FRS9440R, FRS9440H

2.5A, –500V

RDS(on)=4.22Ω

This Objective Data Sheet Represents the Proposed Device Performance.



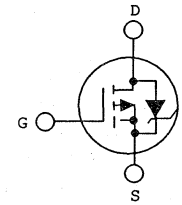
TO-257AA

Radiation-Hardened P-Channel Power MOSFETs

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
3Continuous Drain Current, Id @Tc = 25°C	2.5	A
@Tc = 100°C	1.5	A
Pulsed Drain Current, I_{DM}	7.5	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	75	W
At Tc = 100°C	30	W
Derated above 25°C	0.60	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	7.5	A
Continuous Source Current (Body diode), Is	2.5	A
Pulsed Source Current (Body diode), Ism	7.5	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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2N7322R, 2N7322H

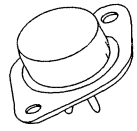
REGISTRATION PENDING

Available As FRK9150R, FRK9150H

26A, –100V

RDS(on)=0.125Ω

Radiation-Hardened P-Channel Power MOSFETs



TO–204AE

Features:

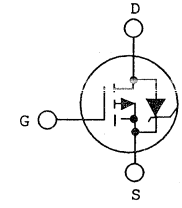
- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 µm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.



SYMBOL

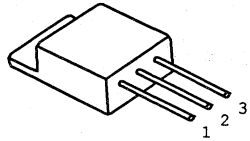
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–100	V
3Continuous Drain Current, Id @Tc = 25°C	26	A
@Tc = 100°C	17	A
Pulsed Drain Current, I_{DM}	78	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 µH, I_{LM} (See Test Figure)	78	A
Continuous Source Current (Body diode), Is	26	A
Pulsed Source Current (Body diode), Ism	78	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7323R, 2N7323H

REGISTRATION PENDING
Available As FRF9150R, FRF9150H
23A, −100V
RDS(on)=0.14Ω

Radiation-Hardened P-Channel Power MOSFETs

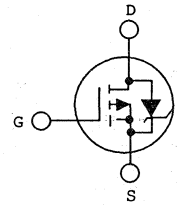


TO-254AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	−100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	−100	V
3Continuous Drain Current, Id @Tc = 25°C	23	A
@Tc = 100°C	15	A
Pulsed Drain Current, I_{DM}	69	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	69	A
Continuous Source Current (Body diode), Is	23	A
Pulsed Source Current (Body diode), Ism	69	A
Operating and Storage Temperature, Tjc, Tstg	−55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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2N7324R, 2N7324H

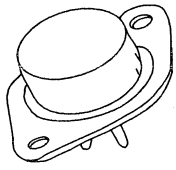
REGISTRATION PENDING

Available As FRM9250R, FRM9250H

16A, –200V

RDS(on)=0.30Ω

Radiation-Hardened P-Channel Power MOSFETs



TO–204AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

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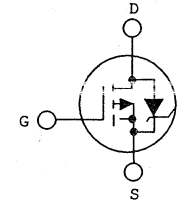


SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
3Continuous Drain Current, Id @Tc = 25°C	16	A
@Tc = 100°C	10	A
Pulsed Drain Current, I_{DM}	48	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	48	A
Continuous Source Current (Body diode), Is	16	A
Pulsed Source Current (Body diode), Ism	48	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7325R, 2N7325H

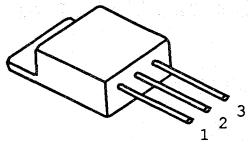
REGISTRATION PENDING

Available As FRF9250R, FRF9250H

14A, –200V

RDS(on)=0.315Ω

Radiation-Hardened P-Channel Power MOSFETs



TO-254AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 1E13 neutrons/cm2.
  —usable to 1E14 neutrons/cm2.
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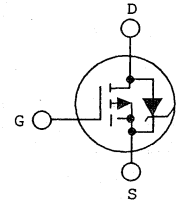

SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
3Continuous Drain Current, Id @Tc = 25°C	14	A
@Tc = 100°C	9	A
Pulsed Drain Current, I_{DM}	42	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	42	A
Continuous Source Current (Body diode), Is	14	A
Pulsed Source Current (Body diode), Ism	42	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

OBJECTIVE 2N7326R, 2N7326H

REGISTRATION PENDING

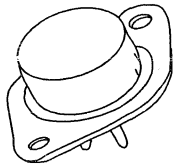
Available As FRM9450R, FRM9450H

6A, –500V

RDS(on)=1.80Ω

This Objective Data Sheet Represents the Proposed Device Performance.

Radiation-Hardened P-Channel Power MOSFETs

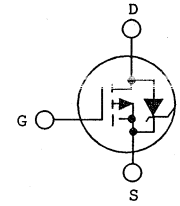


TO–204AA

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.



SYMBOL

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
3Continuous Drain Current, Id @Tc = 25°C	6	A
@Tc = 100°C	4	A
Pulsed Drain Current, I_{DM}	18	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	18	A
Continuous Source Current (Body diode), Is	6	A
Pulsed Source Current (Body diode), Ism	18	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

OBJECTIVE 2N7327R, 2N7327H

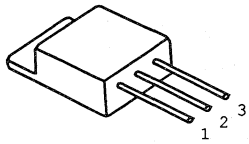
REGISTRATION PENDING

Available As FRF9450R, FRF9450H

5A, –500V

RDS(on)=1.82Ω

This Objective Data Sheet Represents the Proposed Device Performance.



TO-254AA

Radiation-Hardened P-Channel Power MOSFETs

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E12 neutrons/cm2.
  —usable to 3E13 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, syncronous rectification, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

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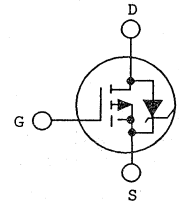

SYMBOL

Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
3Continuous Drain Current, Id @Tc = 25°C	5	A
@Tc = 100°C	3	A
Pulsed Drain Current, I_{DM}	15	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	125	W
At Tc = 100°C	50	W
Derated above 25°C	1.00	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	15	A
Continuous Source Current (Body diode), Is	5	A
Pulsed Source Current (Body diode), Ism	15	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR

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2N7328R, 2N7328H

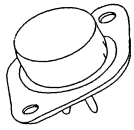
REGISTRATION PENDING

Available As FRK9160R, FRK9160H

40A, –100V

RDS(on)=0.085Ω

Radiation-Hardened P-Channel Power MOSFETs



TO–204AE

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
- Neutron —pre-rad specifications for 3E13 neutrons/cm2.
  —usable to 3E14 neutrons/cm2.
- Single Event —typically survives 1E5 ions/cm2 having an LET ≤ 35MeV/mg/cm2 and a range ≥ 30 μm at 80% BVDSS.

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 6 amperes, and on resistance as low as 25 milliohm. Total dose hardness is offered at 100K and 1000K RAD (Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 Rad(Si)/sec without current limiting and 2E12 Rad(Si)/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

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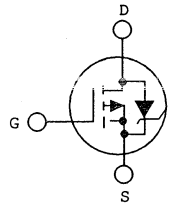


SYMBOL

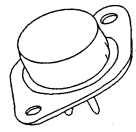
Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–100	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–100	V
3Continuous Drain Current, Id @Tc = 25°C	40	A
@Tc = 100°C	26	A
Pulsed Drain Current, I_{DM}	100	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	100	A
Continuous Source Current (Body diode), Is	40	A
Pulsed Source Current (Body diode), Ism	100	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

2N7330R, 2N7330H

REGISTRATION PENDING
Available As FRK9260R, FRK9260H
26A, –200V
RDS(on)=0.20Ω

Radiation-Hardened P-Channel Power MOSFETs



TO–204AE

Features:

- Second Generation Rad Hard MOSFET results from new design concepts.
- Gamma —meets pre-rad specifications to 100 KRad(Si).
  —defined end-point specs at 300 and 1000 KRad(Si).
  —performance permits limited use to 3000 KRad(Si).
- Gamma Dot —survives 3E9 Rad(Si)/sec at 80% BVDSS typically.
  —survives 2E12 Rad(Si)/sec typically if current-limited to IDM.
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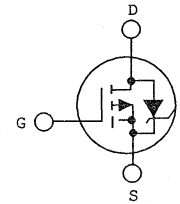

SYMBOL

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–200	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–200	V
3Continuous Drain Current, Id @Tc = 25°C	26	A
@Tc = 100°C	17	A
Pulsed Drain Current, I_{DM}	78	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	78	A
Continuous Source Current (Body diode), Is	26	A
Pulsed Source Current (Body diode), Ism	78	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

HARRIS SEMICONDUCTOR
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OBJECTIVE 2N7332R, 2N7332H

REGISTRATION PENDING

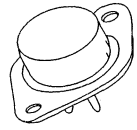
Available As FRK9460R, FRK9460H

10A, –500V

RDS(on)=1.20Ω

This Objective Data Sheet Represents the Proposed Device Performance.

Radiation-Hardened P-Channel Power MOSFETs



TO–204AE

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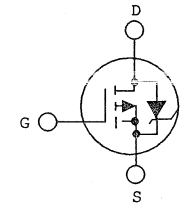

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Maximum Ratings, *Absolute-Maximum Values (Tc = 25°C):*

Drain-Source Voltage, V_{DS}	–500	V
Drain-Gate Voltage, V_{DGR} (Rgs = 20 kΩ)	–500	V
3Continuous Drain Current, Id @Tc = 25°C	10	A
@Tc = 100°C	6	A
Pulsed Drain Current, I_{DM}	30	A
Gate-Source Voltage, V_{GS}	±20	V
Power Dissipation, P_T: At Tc = 25°C	150	W
At Tc = 100°C	60	W
Derated above 25°C	1.20	W/°C
Inductive Current, Clamped, L = 100 μH, I_{LM} (See Test Figure)	30	A
Continuous Source Current (Body diode), Is	10	A
Pulsed Source Current (Body diode), Ism	30	A
Operating and Storage Temperature, Tjc, Tstg	–55 to +150	°C
Lead Temperature (During soldering): T_L		
Distance > 0.063 in. (1.6 mm) from case, 10 s max	300	°C

RAD-HARD 4

OPERATIONAL AMPLIFIERS

HARRIS

HS-3516RH

High Slew Rate, Wideband, Radiation Hardened, Operational Amplifier

July 1990

Features

- Radiation Environment
  - Neutron Fluence (ϕ) ..... 5×10^{12} n/cm^2 ($E \geq 10$KeV)
  - Gamma Rate ($\dot{\gamma}$) ..... 1×10^{9} RAD (Si)/s
  - Gamma Dose (γ) ..... 1×10^{6} RAD (Si)
- High Slew Rate ..... > ±22V/µs
- Fast Settling Time 130ns
- Unity Gain Bandwidth (Typ) 12MHz
- Low Offset Voltage ..... ±3mV
- Low Power Supply Current 6.5mA
- Dielectrically Isolated Device Islands

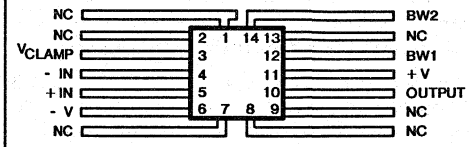
Description

The HS-3516RH is a monolithic, high slew rate, wideband, radiation resistant, operational amplifier. It provides a bandwidth (unity gain stable) of greater than 10MHz and a slew rate in excess of 22V/µsec. Optional frequency compensation adjustment is provided. The HS-3516RH has an internal unity gain frequency compensation capacitor which is internally connected. A clamp node feature enables the user to clamp the output voltage via pin 3 which can source or sink up to 3mA for high frequency clamped switching purposes.

This device is designed to operate from -55°C to +125°C and in strategic-level radiation environments.

Pinout

CERAMIC FLATPACK
TOP VIEW



4 OPERATIONAL AMPLIFIERS

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal ..... V+ to V-
Output Short Circuit Duration (Note 5) ..... Indefinite
Junction Temperature (T_J) ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
ESD Rating ..... <2000V
Lead Temperature (Soldering 10 sec) ..... 275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic CERPAK	82°C/W	16.9°C/W

Package Power Dissipation at +75°C for $T_J \leq +175°C$
Ceramic 1.2W
Package Power Dissipation Derating Factor Above +75°C
Ceramic Package ..... 12.2mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ±5V to ±15V

$V_{INCm} \leq 1/2 (V+ - V-)$
$R_L \geq 2k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$. Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-3.0	3.0	mV
			2	+125°C	-5.0	5.0	mV
			3	-55°C	-10.0	10.0	mV
Input Bias Current	$+I_B$	$V_{CM} = 0V$ $+R_S = 10k\Omega$ $-R_S = 100\Omega$	1	+25°C	-100	100	nA
			2	+125°C	-100	100	nA
			3	-55°C	-500	500	nA
	$-I_B$	$V_{CM} = 0V$ $+R_S = 100\Omega$ $-R_S = 10k\Omega$	1	+25°C	-100	100	nA
			2	+125°C	-100	100	nA
			3	-55°C	-500	500	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$ $+R_S = 10k\Omega$ $-R_S = 10k\Omega$	1	+25°C	-100	100	nA
			2	+125°C	-150	150	nA
			3	-55°C	-500	500	nA
Common Mode Range	+CMR	V+ = +5V V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	$+A_{VOL}$	$V_{OUT} = 0V$ and $+10V$ $R_L = 2k\Omega$	4	+25°C	90	-	dB
			5, 6	+125°C, -55°C	90	-	dB
	$-A_{VOL}$	$V_{OUT} = 0V$ and $-10V$ $R_L = 2k\Omega$	4	+25°C	90	-	dB
			5, 6	+125°C, -55°C	90	-	dB
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +10V$ +V = +5V -V = -25V $V_{OUT} = -10V$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-CMRR	$\Delta V_{CM} = -10V$ +V = +25V -V = -5V $V_{OUT} = +10V$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V. Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT}$	R_L = 2kΩ	1	+25°C	12.5	-	V
			2	+125°C	12.5	-	V
			3	-55°C	12.0	-	V
	$+V_{OUT}$	R_L = 2kΩ	1	+25°C	-	-11.0	V
			2	+125°C	-	-11.0	V
			3	-55°C	-	-11.0	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	1	+25°C	12	-	mA
			2, 3	+125°C, -55°C	12	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	1	+25°C	-	12	mA
			2, 3	+125°C, -55°C	-	12	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	6.5	mA
			2	+125°C	-	6.5	mA
			3	-55°C	-	8.7	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-6.5	-	mA
			2	+125°C	-6.5	-	mA
			3	-55°C	-8.7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Output Short Circuit Current	IOSC	V_{OUT} = 0V	1	+25°C	-	45	mA
			2	+125°C	-	45	mA
			3	-55°C	-	60	mA
Output Clamp Voltage Tolerance	V_{OC1+}	V_{IN} = 1V, V_{CLAMP} = -3.0V V_{OC1+} = V_{OUT} - V_{CLAMP}	1	+25°C	-0.4	0.4	V
	V_{OC2+}	V_{IN} = 1V, V_{CLAMP} = -6.0V V_{OC2+} = V_{OUT} - V_{CLAMP}	1	+25°C	-0.4	0.4	V
	V_{OC1-}	V_{IN} = 1V, V_{CLAMP} = 3.0V V_{OC1-} = V_{OUT} - V_{CLAMP}	1	+25°C	-0.4	0.4	V
	V_{OC2-}	V_{IN} = 1V, V_{CLAMP} = 6.0V V_{OC2-} = V_{OUT} - V_{CLAMP}	1	+25°C	-0.4	0.4	V
Input Clamp Current	I_{CNL-}	V_{IN} = -1V, V_{CLAMP} = 3.0V	1	+25°C	-3.3	-0.25	mA
			2	+125°C	-3.3	-0.18	mA
			3	-55°C	-3.5	-0.30	mA
	I_{CNH-}	V_{IN} = -1V, V_{CLAMP} = 6.0V	1	+25°C	-3.3	-0.25	mA
			2	+125°C	-3.3	-0.18	mA
			3	-55°C	-3.5	-0.30	mA
	I_{CNL+}	V_{IN} = 1V, V_{CLAMP} = -3.0V	1	+25°C	+0.5	+3.0	mA
			2	+125°C	+0.3	+3.0	mA
			3	-55°C	+0.3	+3.2	mA
	I_{CNH+}	V_{IN} = 1V, V_{CLAMP} = -6.0V	1	+25°C	+0.5	+3.0	mA
			2	+125°C	+0.3	+3.0	mA
			3	-55°C	+0.3	+3.2	mA

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 100pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -5V to +5V	4	+25°C	22	-	V/µs
	-SR	V_{OUT} = +5V to -5V	4	+25°C	22	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to 1V 10% ≤ T_R ≤ 90%	4	+25°C	-	35	ns
	T_F	V_{OUT} = 0 to -1V 10% ≤ T_F ≤ 90%	4	+25°C	-	35	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 100pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	10	-	MΩ
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	350	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	70	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	195	mW
Overshoot	+OS	V_{OUT} = 0 to +1.0V	1	+25°C	-	10	%
	-OS	V_{OUT} = 0 to -1.0V	1	+25°C	-	10	%
Settling Time	T_S	To ±5% for a 1V Step	1	+25°C	-	130	ns
Overdrive Recovery Time	T_{OR}		1, 4	+25°C	-	5	µs
Gain Bandwidth Product	GBWP	f_O = 1MHz, V_O = 200mV, A_{VCL} = 10 V/V	1	+25°C	11	-	MHz

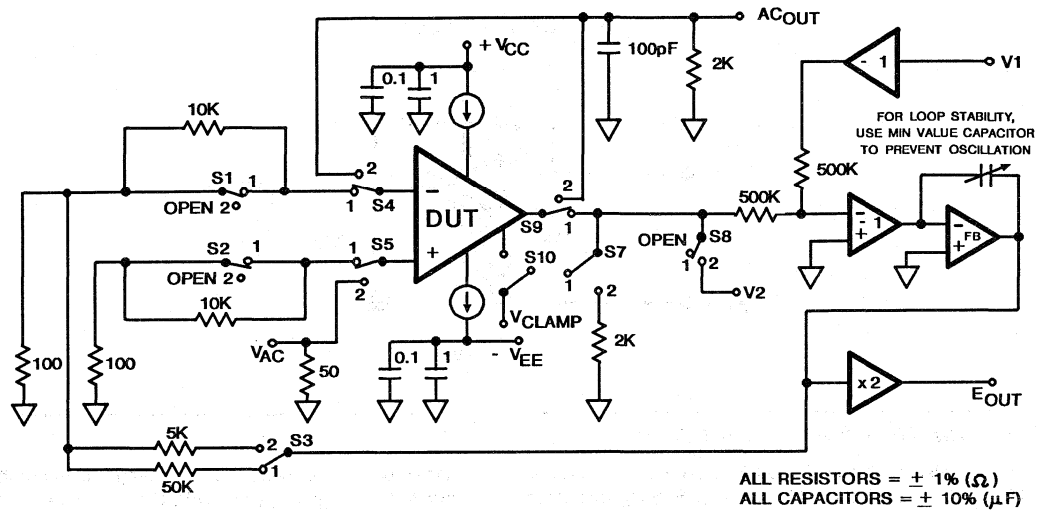
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Overdrive recovery time is the time required for the device to return to linear operation after being overdriven into saturation.
5. Caution: Continuous long duration output short-circuit operation may degrade the operating life of the device.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

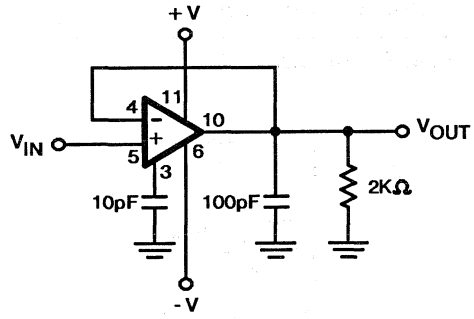
* PDA applies to Subgroup 1 only.

Test Circuit

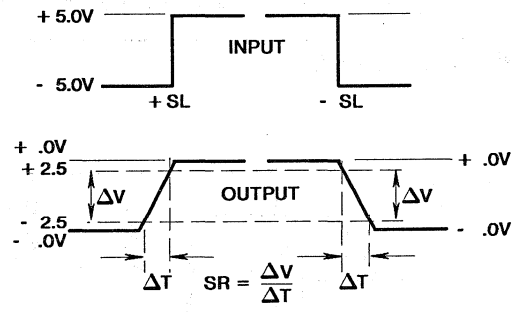


Simplified Test Circuits and Waveforms

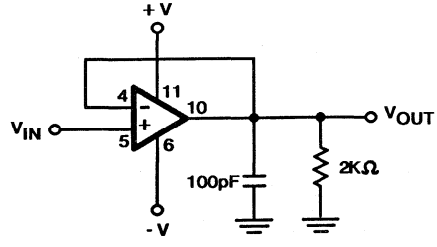
SLEW RATE CIRCUIT



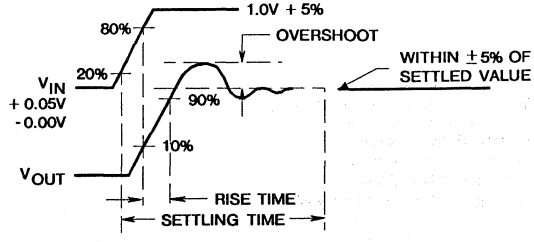
SLEW RATE WAVEFORMS



OVERSHOOT, RISE/FALL/SETTLING TIME CIRCUIT

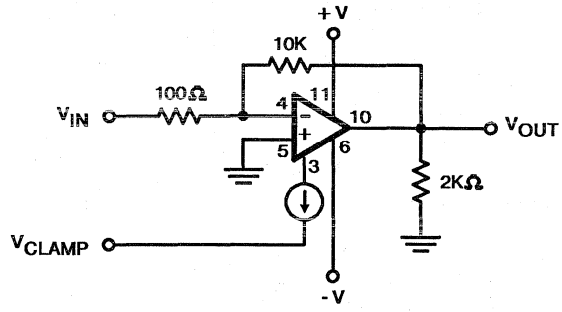


OVERSHOOT, RISE/SETTLING TIME WAVEFORMS



Simplified Test Circuits and Waveforms (Continued)

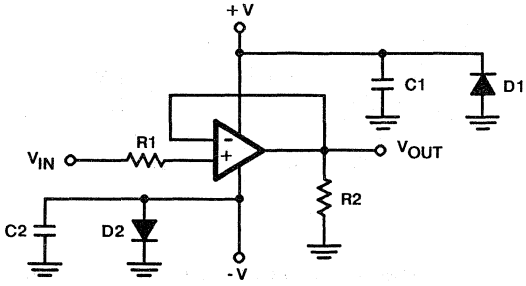
VOLTAGE CLAMP CIRCUIT



Radiation Screening Procedure

1. Die samples shall be selected for total dose testing per MIL-STD-883, Method 5005, Group E, Subgroup 2 for steady-state, total dose irradiation.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1×10^6 Rad(Si) ±10% from a Gammacell 220 Cobalt 60 source or equivalent. The devices will be powered in a voltage configuration illustrated with $V_{SUPPLY} = \pm 15V$. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. A_{VOL} and V_{IO}, with $I_{SET} = 15\mu A$, $V_{SUPPLY} = \pm 15V$, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of $A_{VOL} \geq 80dB$, $V_{IO} \leq \pm 5.0mV$ and $I_{BIAS} \leq \pm 400nA$ at room temperature.

Burn-In Circuit



NOTES:

$|(+V) - (-V)| = 31V \pm 1V$

V_{IN} = 50kHz Square Wave, 50% Duty Cycle, -4.0V to +4.0V (all tolerances ±10%)

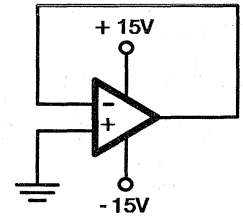
$R_1 = 47k\Omega$, 5%, ¼W (Min.)

$R_2 = 510\Omega$, 5%, ¼W (Min.)

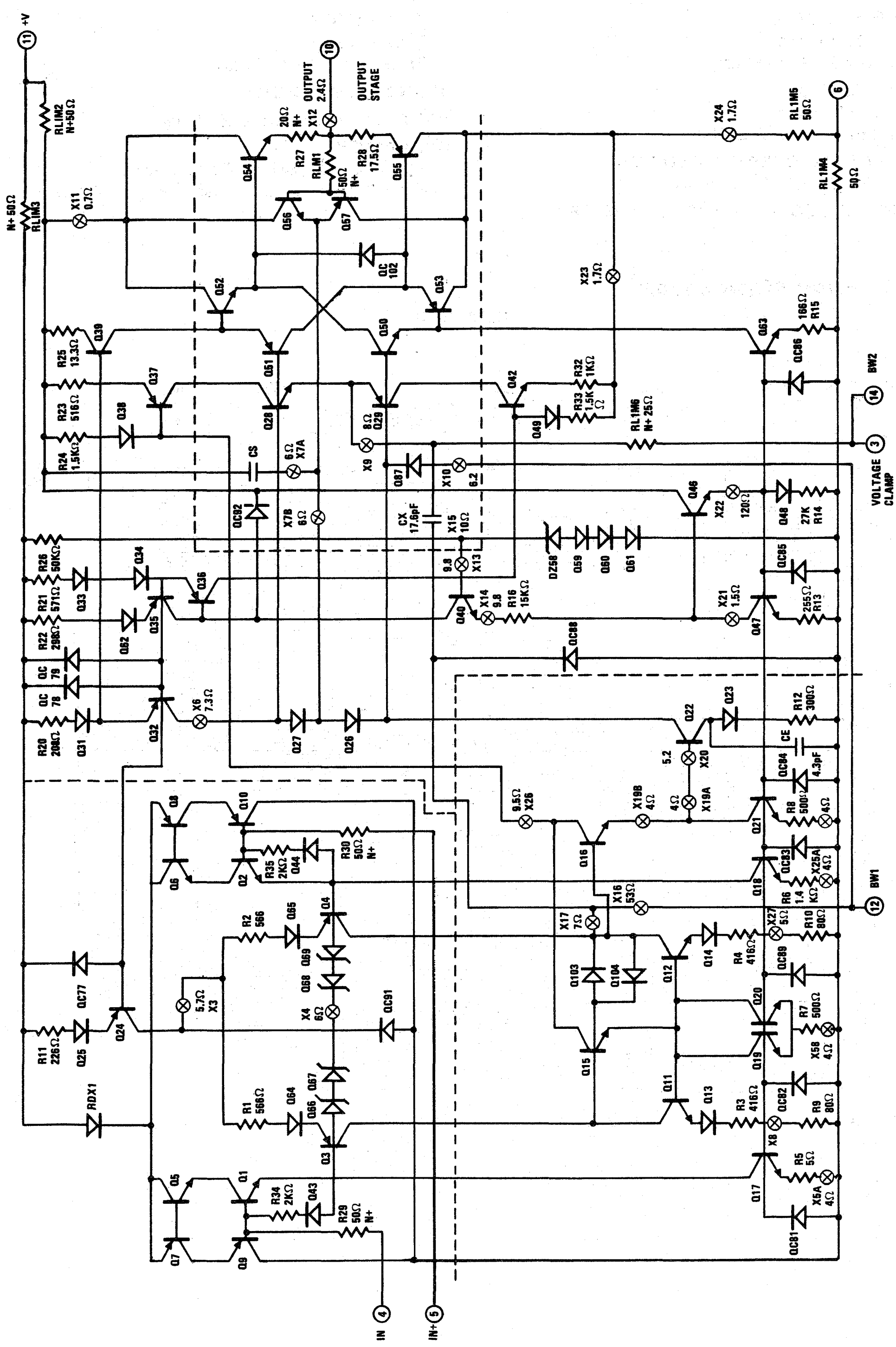
$C_1 = C_2 = 0.01\mu F$ (Min.)

$D_1 = D_2$ = IN4002 or Equivalent/Board

Irradiation Circuit



Schematic



4

OPERATIONAL AMPLIFIERS

Metallization Topology

DIE DIMENSIONS:
93 x 93 11 mils
(2360 x 2360 x 280µm)

METALLIZATION:
Type: Aluminum
Thickness: 12.5kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.385 \times 10^5 A/cm^2$ at 12mA

SUBSTRATE POTENTIAL (POWERED UP): -V

GLASSIVATION:
Type: Silox
Thickness: 8kÅ to 1.0kÅ

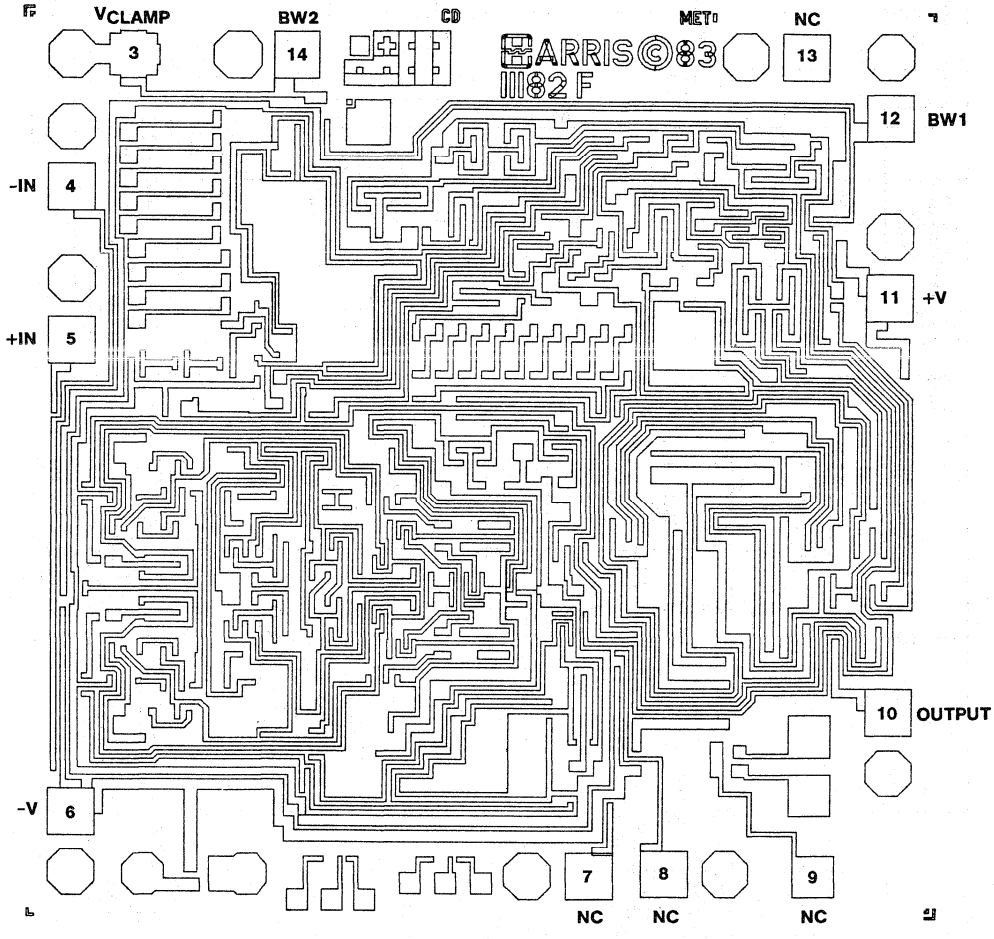
TRANSISTOR COUNT: 84

PROCESS: High Frequency Linear

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic Flatpack - 400°C (Max.)

Metallization Mask Layout

HS-3516RH



HARRIS

HS-3530RH

Low Power-Radiation Hardened Programmable Operational Amplifier

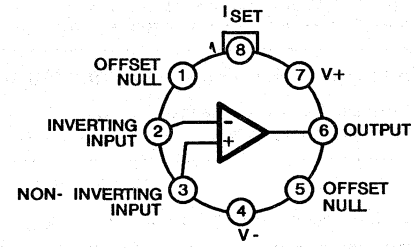
July 1990

Features

- Radiation Environment
  - Neutron Fluence (ϕ) ..... 5×10^{12} n/cm^2 (E $\geq$ 10KeV)
  - Gamma Rate ($\dot{\gamma}$) ..... 1×10^{9} RAD (Si)/s
  - Gamma Dose (γ) ..... 1×10^{6} RAD (Si)
- Wide Range AC Programming
  - Slew Rate ..... 0.06 to 3V/μs
  - Gain X Bandwidth ..... 100KHz to 5.0MHz
- Wide Range DC Programming
  - Power Supply Range ..... $\pm$3.0V to $\pm$15V
  - Supply Current ..... 10μA to 1.2mA
- Dielectrically Isolated Device Islands
- Short Circuit Protection

Pinout

METAL CAN
TOP VIEW



NOTE: CASE TIED TO V-

Description

The HS-3530RH is a Low Power Operational Amplifier which is an internally compensated monolithic device offering a wide range of performance specifications. Parameters such as power dissipation, slew rate, bandwidth, noise and input DC parameters are programmed by selecting an external resistor or current source. Supply voltages as low as $\pm$3 volts may be used with little degradation of AC performance. The HS-3530RH has been specifically designed to meet exposure to radiation environments. Operation from -55^{o}C to +125^{o}C is guaranteed.

A major advantage of the HS-3530RH is that operating characteristics remain virtually constant over a wide supply range ($\pm$3V to $\pm$15V), allowing the amplifier to offer maximum performance in almost any system, including battery operated equipment. A primary application for this device is in active filtering and conditioning for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the set current, it can be used for designs such as current controlled oscillators/modulators, sample and hold circuits and variable active filters.

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage..... 20V
Voltage at Either Input Terminal..... V+ to V-
I_{SET} (Current at I_{SET}) 500µA
V_{SET} (Voltage to GND at I_{SET}) .....(V+ -2.0V) < V_{SET} < V+
Output Short Circuit Duration (Note 6) ..... Indefinite
Junction Temperature (T_J) ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
ESD Rating ..... <2000V
Lead Temperature (Soldering 10 sec) ..... 275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Metal Can Package	75°C/W	12°C/W

Package Power Dissipation at +75°C for TJ ≤ +175°C
Metal Can Package 0.9W

Package Power Dissipation Derating Factor Above +75°C
Metal Can Package ..... 9mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ±3V to ±15V

$V_{INCm} \leq 1/2$ (V+ - V-)
$R_L \geq 2k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS I_{SET} = 1.5µA MIN	LIMITS I_{SET} = 1.5µA MAX	LIMITS I_{SET} = 15µA MIN	LIMITS I_{SET} = 15µA MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-3	3	-3	3	mV
			2, 3	+125°C, -55°C	-5	5	-5	5	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 100Ω	1	+25°C	-	-	-20	20	nA
			2, 3	+125°C, -55°C	-	-	-40	40	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 100Ω $-R_S$ = 10kΩ	1	+25°C	-	-	-20	20	nA
			2, 3	+125°C, -55°C	-	-	-40	40	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 10kΩ $-R_S$ = 10kΩ	1	+25°C	-	-	-5	5	nA
			2, 3	+125°C, -55°C	-	-	-10	10	nA
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V Note 4	4	+25°C	65	-	80	-	kV/V
			5, 6	+125°C, -55°C	25	-	50	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -10V Note 4	4	+25°C	65	-	80	-	kV/V
			5, 6	+125°C, -55°C	25	-	50	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +5V +V = +10V -V = -20V V_{OUT} = -5V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
	-CMRR	ΔV_{CM} = -5V +V = +20V -V = -10V V_{OUT} = +5V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
Output Voltage Swing	$+V_{OUT}$	Note 4	1	+25°C	12.5	-	12.5	-	V
			2, 3	+125°C, -55°C	10.5	-	10.5	-	V
	$-V_{OUT}$	Note 4	1	+25°C	-	12.5	-	-12.5	V
			2, 3	+125°C, -55°C	-	-10.5	-	-10.5	V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS I_{SET} = 1.5µA MIN	LIMITS I_{SET} = 1.5µA MAX	LIMITS I_{SET} = 15µA MIN	LIMITS I_{SET} = 15µA MAX	UNITS
Output Current	$+I_{OUT}$	R_L = 2kΩ	1	+25°C	0.25	-	0.25	-	mA
	$-I_{OUT}$	R_L = 2kΩ	1	+25°C	-	-0.25	-	-0.25	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	15	-	150	µA
			2, 3	+125°C, -55°C	-	15	-	160	µA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-15	-	-150	-	µA
			2, 3	+125°C, -55°C	-15	-	-160	-	µA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V, +V = +10V, -V = -15V, +V = +20V, -V = -15V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
	-PSRR	ΔV_{SUP} = 10V, +V = +15V, -V = -10V, +V = +15V, -V = -20V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±3V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS I_{SET} = 1.5µA MIN	LIMITS I_{SET} = 1.5µA MAX	LIMITS I_{SET} = 15µA MIN	LIMITS I_{SET} = 15µA MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25°C	-3	3	-3	3	mV
			2, 3	+125°C, -55°C	-5	5	-5	5	mV
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +1V, Note 4	4	+25°C	25	-	25	-	kV/V
			5, 6	+125°C, -55°C	15	-	25	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and -1V, Note 4	4	+25°C	25	-	25	-	kV/V
			5, 6	+125°C, -55°C	15	-	25	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +1.5V, +V = +1.5V, -V = -4.5V, V_{OUT} = -1.5V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
	-CMRR	ΔV_{CM} = -1.5V, +V = +4.5V, -V = -1.5V, V_{OUT} = +1.5V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
Output Voltage Swing	$+V_{OUT}$	Note 4	1	+25°C	2.0	-	2.0	-	V
			2, 3	+125°C, -55°C	2.0	-	2.0	-	V
	$-V_{OUT}$	Note 4	1	+25°C	-	-2.0	-	-2.0	V
			2, 3	+125°C, -55°C	-	-2.0	-	-2.0	V
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	15	-	150	µA
			2, 3	+125°C, -55°C	-	15	-	160	µA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-15	-	-150	-	µA
			2, 3	+125°C, -55°C	-15	-	-160	-	µA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 1.5V, +V = +3V, -V = -3V, +V = +4.5V, -V = -3V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
	-PSRR	ΔV_{SUP} = 1.5V, +V = +3V, -V = -3V, +V = +3V, -V = -4.5V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: R_{SOURCE} = 50Ω, C_L = 100pF, AVCL = +1, R_L = 5kΩ, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS I_{SET} = 1.5µA MIN	LIMITS I_{SET} = 1.5µA MAX	LIMITS I_{SET} = 15µA MIN	LIMITS I_{SET} = 15µA MAX	UNITS
V_{SUPPLY} = ±15V									
Slew Rate	+SR	V_{OUT} = -10V to +10V	4	+25°C	0.025	-	0.25	-	V/µs
Note 5	-SR	V_{OUT} = +10V to -10V	4	+25°C	0.025	-	0.25	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +400mV 10% < T_R < 90%	4	+25°C	-	8.0	-	0.8	µs
	T_F	V_{OUT} = 0 to -400mV 10% < T_F < 90%	4	+25°C	-	6.0	-	0.6	µs
Overshoot	+OS	V_{OUT} = 0 to +400mV	4	+25°C	-	35	-	35	%
	-OS	V_{OUT} = 0 to -400mV	4	+25°C	-	35	-	35	%
V_{SUPPLY} = ±3V									
Slew Rate	+SR	V_{OUT} = -2V to +2V	4	+25°C	0.01	-	0.1	-	V/µs
Note 5	-SR	V_{OUT} = 2V to -2V	4	+25°C	0.01	-	0.1	-	V/µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: R_{SOURCE} = 50Ω, C_L = 100pF, AVCL = +1, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS I_{SET} = 1.5µA MIN	LIMITS I_{SET} = 1.5µA MAX	LIMITS I_{SET} = 15µA MIN	LIMITS I_{SET} = 15µA MAX	UNITS
V_{SUPPLY} = ±15V									
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	50	-	50	-	MΩ
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	0.4	-	4	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+1	-	+1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	10	-	10	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	4.8	-	4.8	mW
Output Short-Circuit Current	I_{OSC}	V_{OUT} = 0V	1, 6	+25°C	-14	38	-27	42	mA
Gain Bandwidth Product	GBWP	AVCL = 10V/V V_O = 200mV, f_O = 10kHz	1	+25°C	45	-	750	-	kHz
V_{SUPPLY} = ±3V									
Gain Bandwidth Product	GBWP	AVCL = 10V/V V_O = 200mV, f_O = 10kHz	1	+25°C	30	-	600	-	kHz

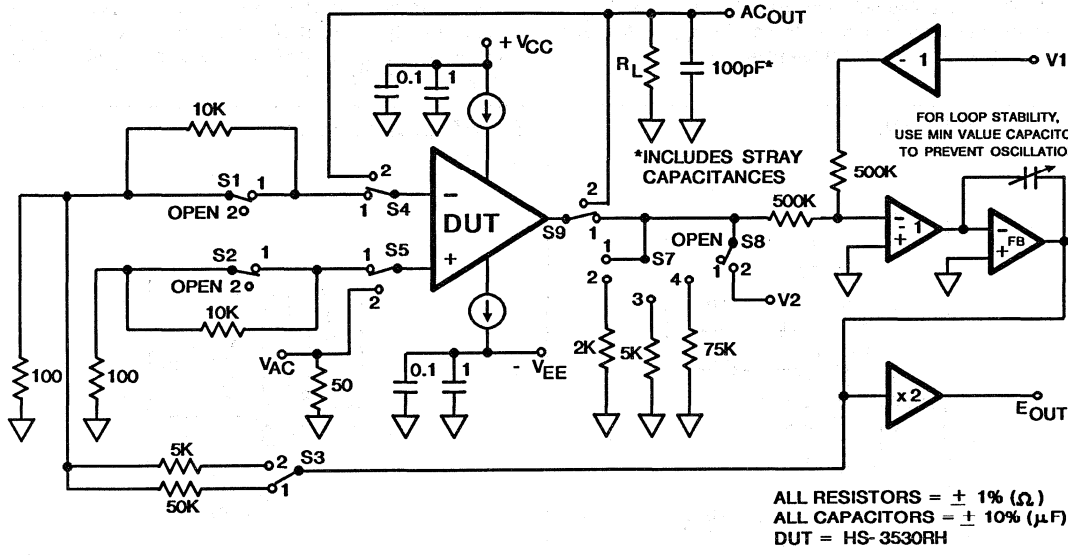
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/(2πV_{PEAK}).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs).
4. R_L = 75kΩ at I_{SET} = 1.5µA, R_L = 5kΩ at I_{SET} = 15µA.
5. R_L = 20kΩ at I_{SET} = 1.5µA.
6. Caution: Continuous long-duration short-circuit operation may degrade the operating life of the device.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

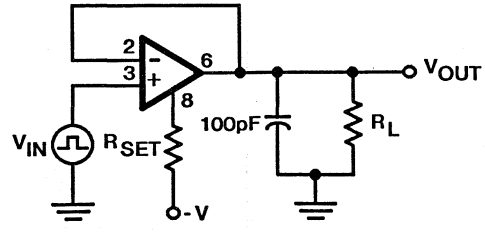
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C and D Endpoints	1

*PDA applies to Subgroup 1 only.

Test Circuit



Simplified Transient Response/Slew Rate Circuit



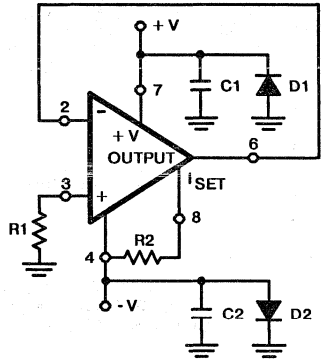
Radiation Screening Procedure

1. Die samples shall be selected for total dose testing per MIL-STD-883, Method 5005, Group E, Subgroup 2 for steady-state, total dose irradiation.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1×10^6 Rad(Si) ±10% from a Gammacell 220 Cobalt 60 source or equivalent. The devices will be powered in a voltage follower configuration, with I_{SET} = 15µA and V_{SUPPLY} = ±15V. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. A_{VOL} and V_{IO}, with I_{SET} = 15µA, V_{SUPPLY} = ±15V and R_L = 25K, will be measured and recorded for each device within one hour after irradiation. The wafer/wafer lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of A_{VOL} > 20K V/V and V_{IO} < 3.5mV at room temperature.

Radiation Effects

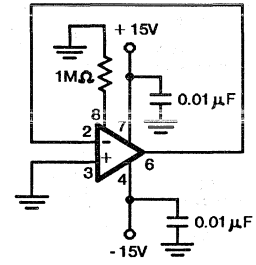
1. TOTAL DOSE:
   Very little degradation of any of the parameters will be seen up to $\gamma = 10^4$ Rad(Si). Moderate degradation of open loop gain, bias current, and offset current begins at greater than 10^5 and less than 10^6 Rad(Si).
2. DOSE RATE:
   During transient ionizing at a level of 1×10^9 rad(Si)/s, the peak level of supply current will be about 150 to 200mA. After about 0.1 to 0.5µs this current drops about 10%. Maximum recovery time will be about 6 to 8µs. Devices are constructed in DI and consequently are latch-up free.
3. NEUTRON FLUENCE:
   Large signal voltage gain degrades rapidly for low supply voltages and low set currents. For V_{SUPPLY} = +15V and I_{SET} > 10µA, large signal voltage gain degrades by only about 50%. Input bias current doubles for $\phi = 5 \times 10^{12} n/cm^2$.

Burn-In Circuit

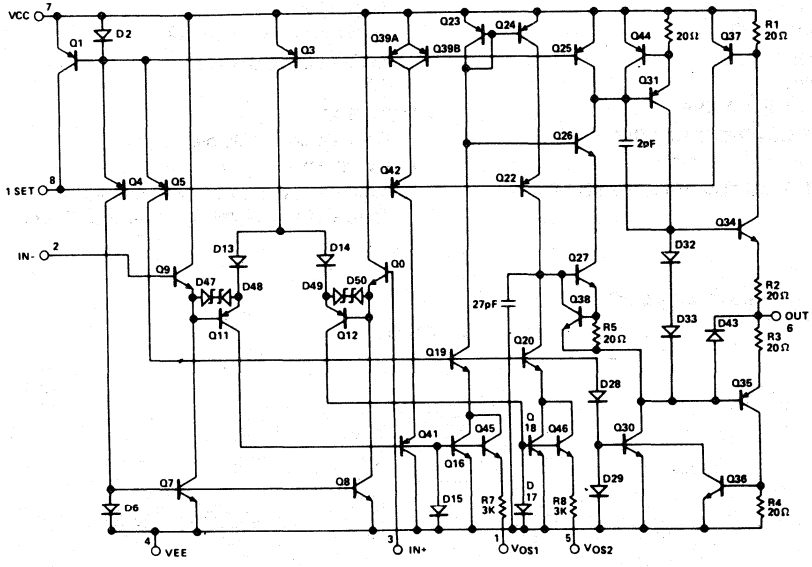


NOTES:
|(V+)-(V-)| = 31V ± 1V
C1 = C2 = 0.01µF/Socket (Min)
D1 = D2 = IN4002 or Equivalent/Board
R1 = 1MV, 5%, 1/4W (Min)
R2 = 2MV, 5%, 1/4W (Min)
T_A = +125°C Minimum

Irradiation Circuit



Schematic


VCC 7
D2
Q1
Q3
Q39A
Q39B
Q23
Q24
Q25
Q44
20Ω
Q37
R1 20Ω
Q31
Q26
2pF
1 SET 8
Q4
Q5
Q42
Q22
Q34
IN- 2
D13
D14
D32
Q9
Q0
Q27
R2 20Ω
D47
D48
D49
D50
27pF
Q38
OUT 6
Q11
Q12
R5 20Ω
D33
D43
R3 20Ω
Q19
Q20
D28
Q35
Q41
Q45
Q 18
Q46
Q30
Q16
Q7
Q8
D29
Q36
D6
D15
R7 3K
D 17
R8 3K
R4 20Ω
4 VEE
3 IN+
1 VOS1
5 VOS2

Metallization Topology

DIE DIMENSIONS:
54 x 67 x 11.5 mils
(1370 x 1700 x 290 µm)

METALLIZATION:
Type: Aluminum
Thickness: 12.5kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
0.544 x 10^5A/cm^2 at 2.5mA

SUBSTRATE POTENTIAL (POWERED UP):
-V

GLASSIVATION:
Type: Silox
Thickness: 8kÅ to 1.0kÅ

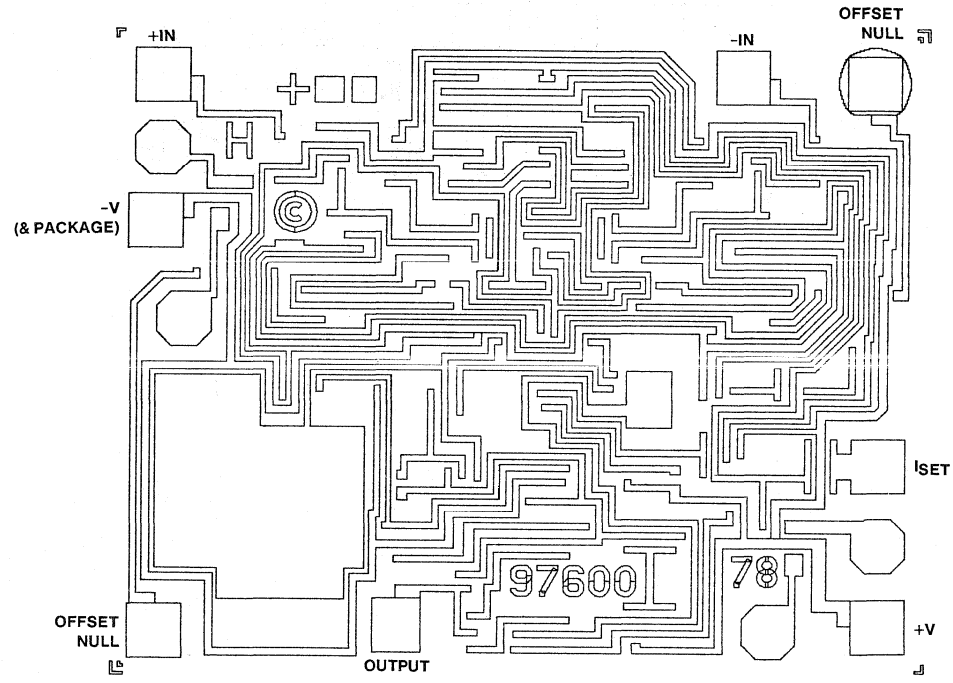
TRANSISTOR COUNT:
49

PROCESS:
Complimentary Bipolar

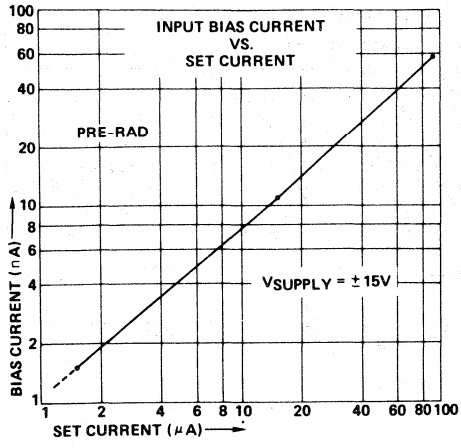
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Metal Can - 420°C (Max.)

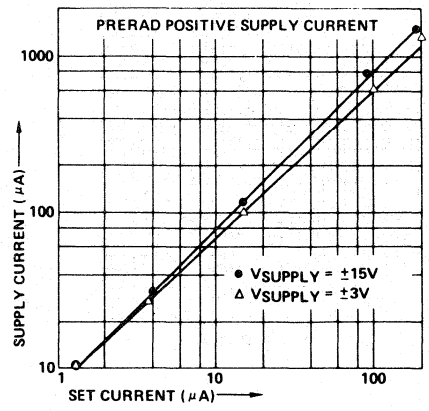
Metallization Mask Layout

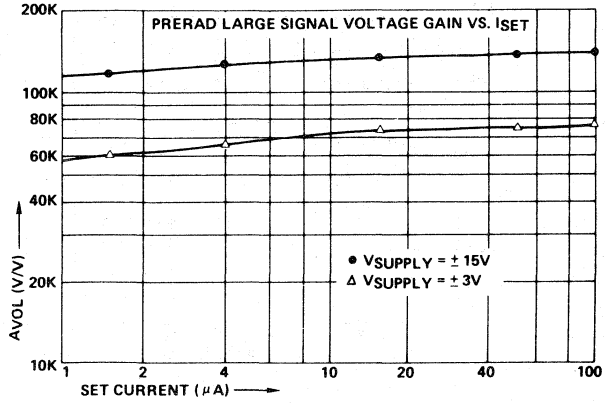
HS-3530RH

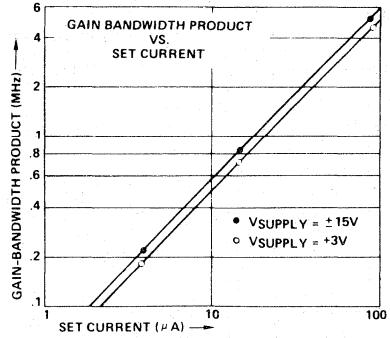


Typical Performance Curves

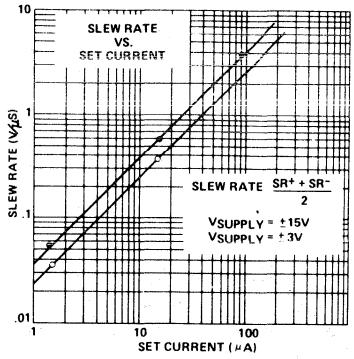


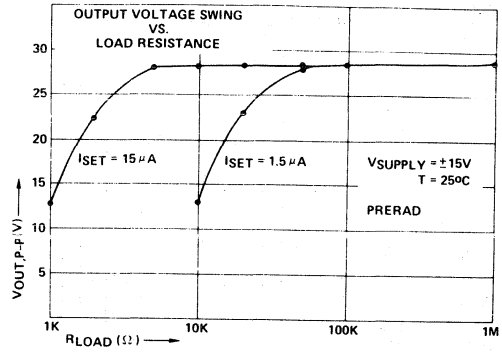


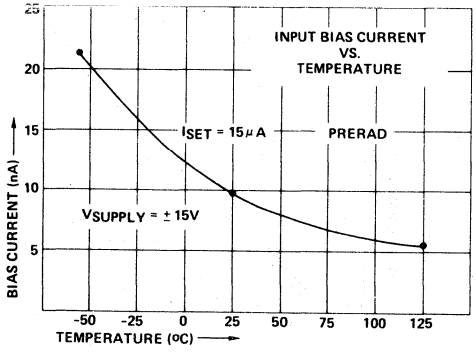


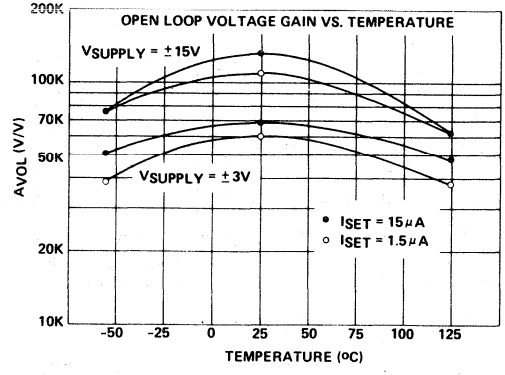


Typical Performance Curves









HARRIS

HS-5104RH

Radiation Hardened Low Noise Quad Operational Amplifier

July 1990

Features

- Radiation Environment
  - Neutron Fluence (ϕ) ..... 5×10^{12} n/cm^2 (E $\geq$ 10KeV)
  - Gamma Rate ($\dot{\gamma}$) ..... 1×10^{9} RAD (Si)/s
  - Gamma Dose (γ) ..... 1×10^{5} RAD (Si)
- Low Noise
  - @ 1kHz ..... 0.5nV/$\sqrt{Hz}$ (Typ)
  - @ 1kHz ..... 3.5pA/$\sqrt{Hz}$ (Typ)
- Low Offset Voltage 3.0mV
- High Slew Rate ..... 2.0V/μs (Typ)
- Gain Bandwidth Product ..... 6.5MHz (Typ)
- Dielectrically Isolated Bipolar Technology
- Single 5V Supply Capability

Applications

- High Q, Active Filters
- Audio Amplifiers
- Voltage Regulators
- Integrators
- Signal Generators
- Voltage References
- Space and Reactor Environments

Description

The HS-5104RH is a radiation hardened, dielectrically isolated bipolar monolithic quad operational amplifier that provides low noise operation in a radiation hardened design. The predominant feature of the HS-5104RH is its excellent noise characteristics, typically only 0.5nV/$\sqrt{Hz}$ and 3.5pA/$\sqrt{Hz}$ at 1kHz. This general purpose amplifier also offers an array of dynamic specifications ranging from a typical 2V/μs slew rate and a 6.5MHz unity gain bandwidth to a minimum output drive current of 10mA.

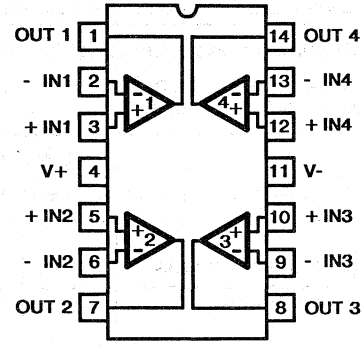
The HS-5104RH shows almost no change in offset voltage and current after exposure to 100K rad(Si) gamma radiation, with only a minor increase in bias current. Complementing these specifications is a post radiation open loop gain in excess of 40K.

This impressive combination of features makes this amplifier ideally suited for a variety of applications such as active filter design, signal conditioning, and instrumentation circuits. Designed to meet exposure in radiation environments, this amplifier is a necessity for satellite, spacecraft, and nuclear power systems where its unique properties will prolong the useful life of a system.

This quad operational amplifier is available in an industry standard pinout allowing for immediate interchangeability with most other quad operational amplifiers.

Pinout

HS1-5104RH
(CERAMIC SIDEBRAZED DIP)
TOP VIEW



4 OPERATIONAL AMPLIFIERS

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal ..... V+ to V-
Peak Output Current (Note 5) ..... Indefinite
(One Amplifier Shorted to GND)
Junction Temperature (T_J) ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
ESD Rating ..... <2000V
Lead Temperature (Soldering 10 sec) ..... 275°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic Side Braze	75°C/W	12°C/W

Package Power Dissipation at +75°C for $T_J \leq +175°C$
Ceramic Side Braze 1.3W
Package Power Dissipation Derating Factor Above +75°C
Ceramic Side Braze ..... 13mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ±5V to ±15V

$V_{INCM} \leq 1/2\ (V+ - V-)$
$R_L \geq 2k\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 100k\Omega$, $V_{OUT} = 0V$. Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-3.0	3.0	mV
			2,3	+125°C, -55°C	-15.0	15.0	mV
Input Bias Current	$+I_B$	$V_{CM} = 0V$ $+R_S = 10k\Omega$ $-R_S = 100\Omega$	1	+25°C	-300	300	nA
			2,3	+125°C, -55°C	-550	550	nA
	$-I_B$	$V_{CM} = 0V$ $+R_S = 100\Omega$ $-R_S = 10k\Omega$	1	+25°C	-300	300	nA
			2,3	+125°C, -55°C	-550	550	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$ $+R_S = 10k\Omega$ $-R_S = 10k\Omega$	1	+25°C	-300	300	nA
			2,3	+125°C, -55°C	-400	400	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25°C	12	-	V
			2,3	+125°C, -55°C	12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25°C	-	-12	V
			2,3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	$V_{OUT} = 0V$ and $+10V$ $R_L = 2k\Omega$	1	+25°C	75	-	kV/V
			2	+125°C	100	-	kV/V
			3	-55°C	55	-	kV/V
	$-A_{VOL}$	$V_{OUT} = 0V$ and $-10V$ $R_L = 2k\Omega$	1	+25°C	75	-	kV/V
			2	+125°C	100	-	kV/V
			3	-55°C	55	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +12V$ +V = +3V -V = -27V $V_{OUT} = -12V$	1	+25°C	80	-	dB
			2,3	+125°C, -55°C	80	-	dB
	-CMRR	$\Delta V_{CM} = -12V$ +V = +27V -V = -3V $V_{OUT} = +12V$	1	+25°C	80	-	dB
			2,3	+125°C, -55°C	80	-	dB

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V. Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	$+V_{OUT2}$	R_L = 10kΩ	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	$-V_{OUT1}$	R_L = 2kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	$-V_{OUT2}$	R_L = 10kΩ	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Output Current	$+I_{OUT}$	V_{OUT} = -5V	1	+25°C	10	-	mA
			2, 3	+125°C, -55°C	10	-	mA
	$-I_{OUT}$	V_{OUT} = +5V	1	+25°C	-	-10	mA
			2, 3	+125°C, -55°C	-	-10	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	6.0	mA
			2, 3	+125°C, -55°C	-	6.0	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-6.0	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V. Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V	4	+25°C	1	-	V/µs
	-SR	V_{OUT} = +3V to -3V	4	+25°C	1	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	4	+25°C	-	150	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	4	+25°C	-	150	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	4	+25°C	-	45	%
	-OS	V_{OUT} = 0 to -200mV	4	+25°C	-	45	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V. Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	250	-	kΩ
Input Noise Voltage Density	E_n	R_S = 20Ω, f_o = 1000Hz	1	+25°C	-	4	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 20MΩ, f_o = 1000Hz	1	+25°C	-	1	$pA/\sqrt{Hz}$
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	15	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	200	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	180	mW
Channel Separation	CS	R_S = 1kΩ, A_{VCL} = 100V/V, V_{IN} = 100mV_{RMS} @ 10kHz Referred to Input	1	+25°C	90	-	dB
Settling Time	T_S	A_{VCL} = -1	1, 4	+25°C	-	5	µs

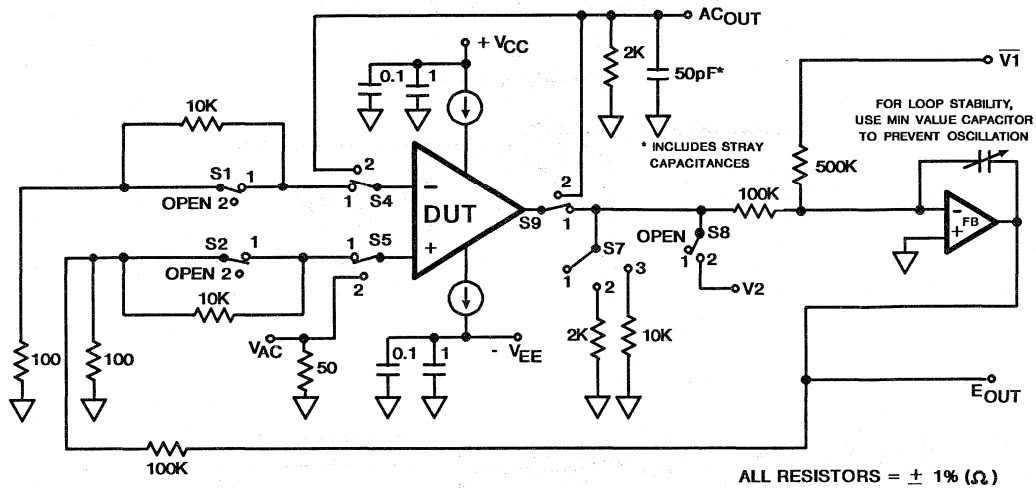
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/(2πV_{PEAK}).
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Settling time measured from the 90% point of a 10V input pulse to within 10mV of the settled value.
5. Caution: Continuous long-duration short-circuit operation may degrade the operating life of the device.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

Test Circuits (Applies to Tables 1 and 2)

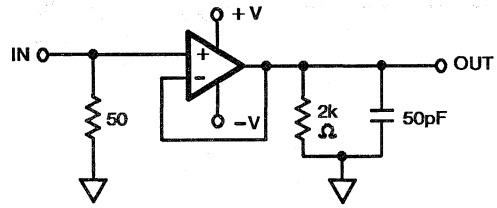


ONE OF FOUR TEST LOOPS FOR THE HS-5104RH

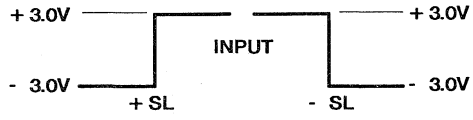
ALL RESISTORS = ± 1% (Ω)
ALL CAPACITORS = ± 10% (µF)
DUT = 1/4 OF HS- 5104RH

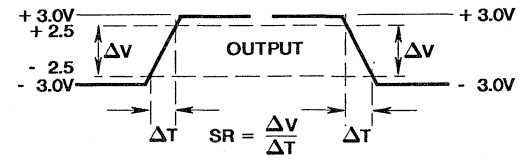
Test Circuits and Waveforms

SIMPLIFIED TEST CIRCUIT (Applies to Tables 2 and 3)

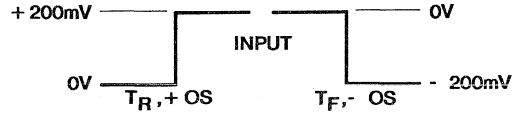


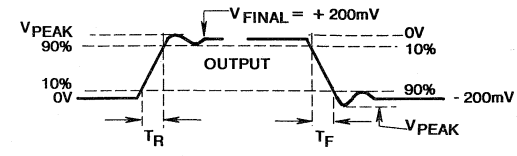
SLEW RATE WAVEFORMS





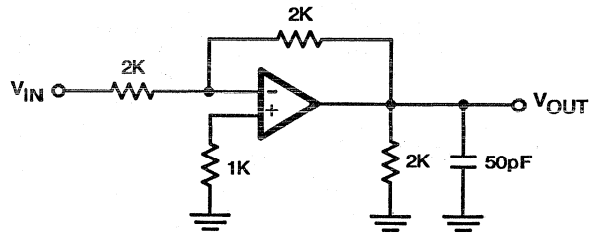
OVERSHOOT, RISE/FALL TIME WAVEFORMS

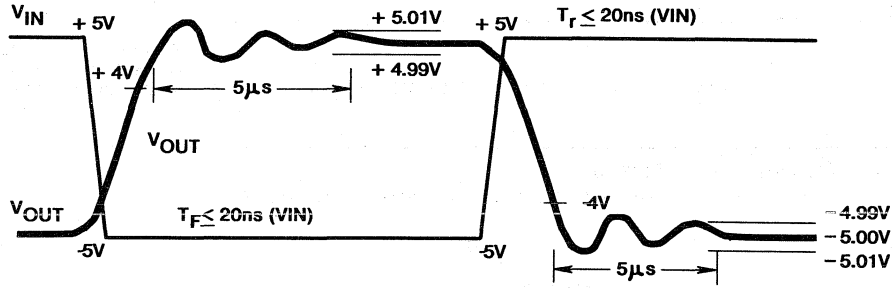




Test Circuits and Waveforms (Continued)

SETTLING TIME TEST CIRCUIT AND WAVEFORM





Radiation Screening Procedure

1. Die samples shall be selected for total dose testing per MIL-STD-883, Method 5005, Group E, Subgroup 2 for steady-state, total dose irradiation.
2. The sample die shall be assembled and tested for proper functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad-Si (±10%) from a Gammacell 220 Cobalt 60 source or equivalent. The samples will be powered in the configuration illustrated with V_{SUPPLY} = ±15V. The dose rate shall be between 100 rad/sec and 300 rad/sec.
4. A_{VOL}, V_{IO}, I_{BIAS}, and I_{IO} with V_{SUPPLY} = ±15V, will be measured and recorded for each device within one hour after irradiation. The wafer/wafer lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of A_{VOL} > 40K, V_{IO} < 3.0mV, I_{BIAS} < 1µA, and I_{IO} < 300nA at room temperature.

Radiation Effects

1. TOTAL DOSE:

   Very little degradation of any of the parameters will be seen up to $\gamma = 10^4$ Rad(Si). Moderate degradation of open loop gain, bias current, and offset current begins at greater than 10^5 and less than 10^6 Rad(Si).

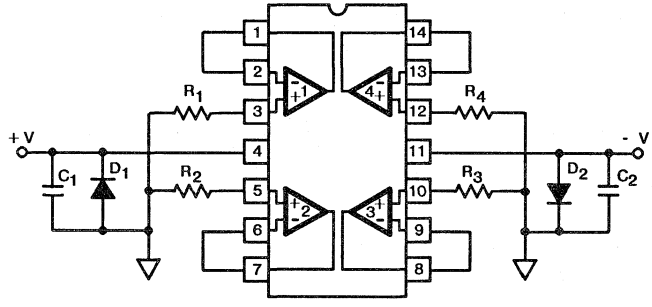
2. DOSE RATE:

   During transient ionizing at a level of 1 x 10^9 rad(Si)/s, the peak level of supply current will be about 150 to 200mA. After about 0.1 to 0.5µs this current drops about 10%. Maximum recovery time will be about 6 to 8µs. Devices are constructed in DI and consequently are latch-up free.

3. NEUTRON FLUENCE:

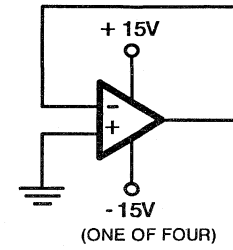
   Large signal voltage gain degrades rapidly for low supply voltages and low set currents. For V_{SUPPLY} = +15V and I_{SET} > 10µA, large signal voltage gain degrades by only about 50%. Input bias current doubles for $\phi = 5 \times 10^{12} n/cm^2$.

Burn-In Circuit

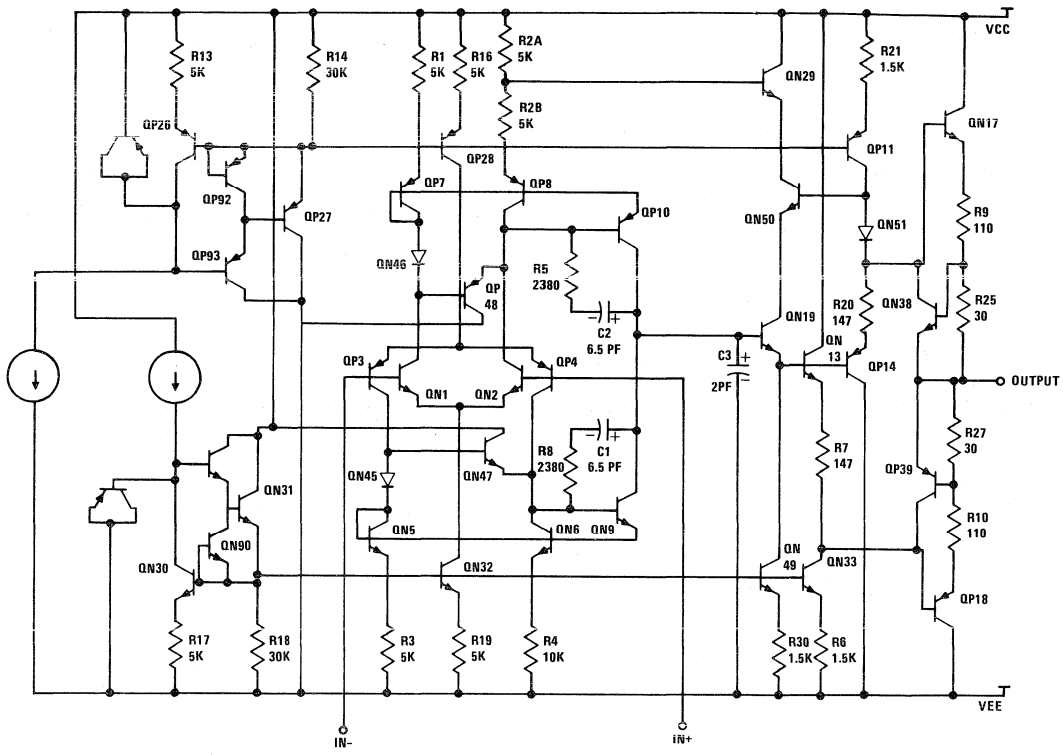


NOTES:
$R_1 = R_2 = R_3 = R_4$ = 1MΩ, 5%, 1/4W (Min)
$C_1 = C_2$ = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
$D_1 = D_2$ = IN4002 or Equivalent/Board
|(V+) - (V-)| = 31V ± 1V

Irradiation Circuit



Schematic



(ONE OF FOUR)

Metallization Topology

DIE DIMENSIONS:
124 x 108 x 11 mils
(3160 x 2740 x 280 µm)

METALLIZATION:
Type: Aluminum
Thickness: 12.5kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
1.45 x 10^5A/cm^2 at 10mA

SUBSTRATE POTENTIAL (POWERED UP):
V-

GLASSIVATION:
Type: Silox
Thickness: 8kÅ to 1.0kÅ

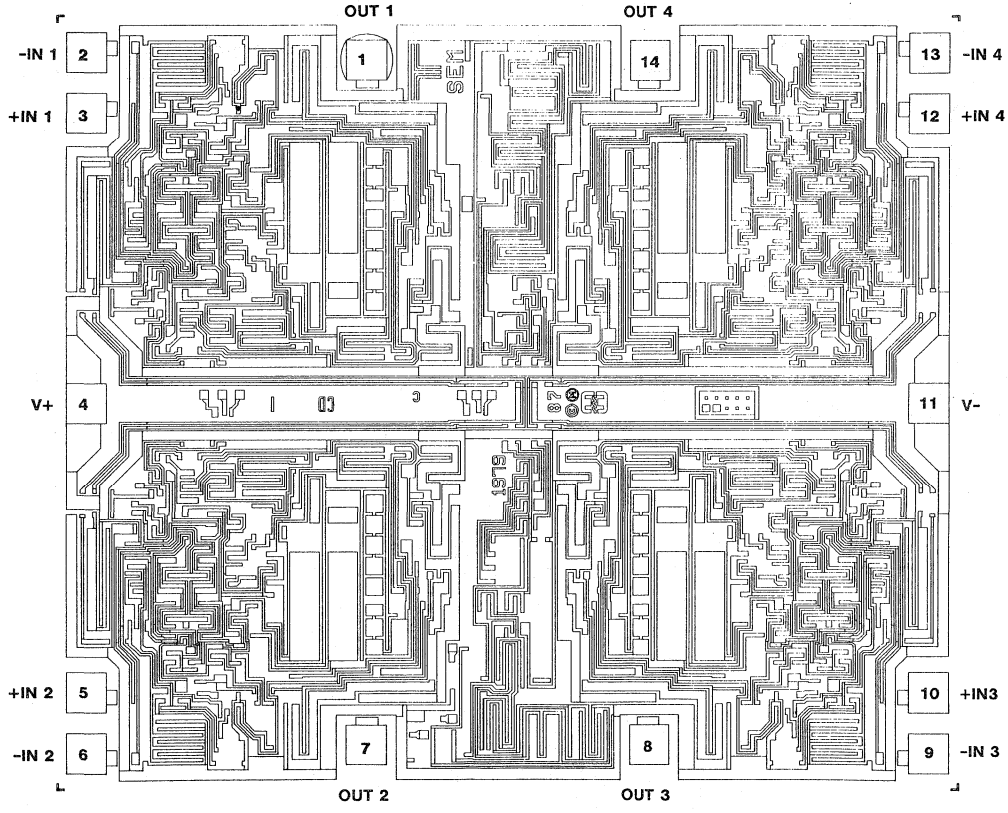
TRANSISTOR COUNT:
175

PROCESS:
High Frequency Linear

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic Side Braze - 460°C (Max.)

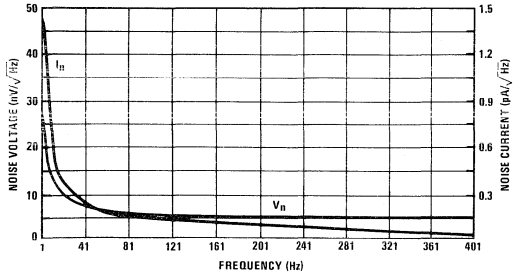
Metallization Mask Layout

HS-5104RH

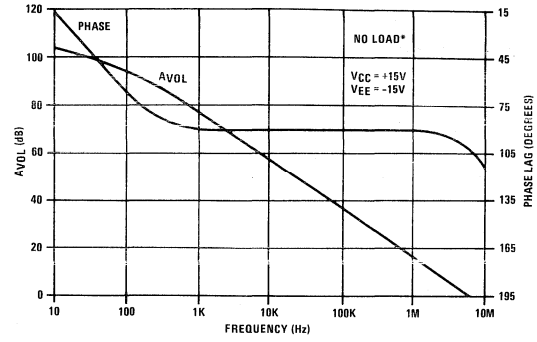


Typical Performance Curves

TYPICAL NOISE VOLTAGE AND CURRENT VS. FREQUENCY

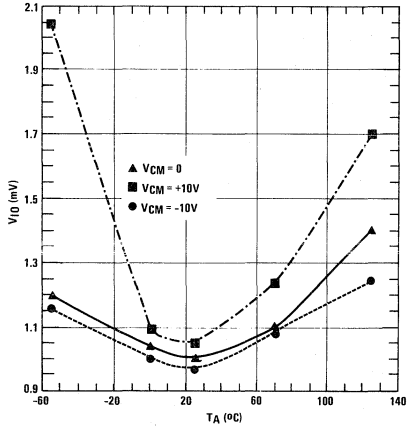


OPEN LOOP GAIN AND PHASE VS. FREQUENCY

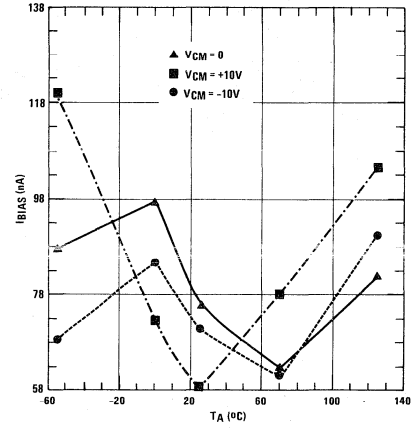


*Derate 4dB for R_L = 2K

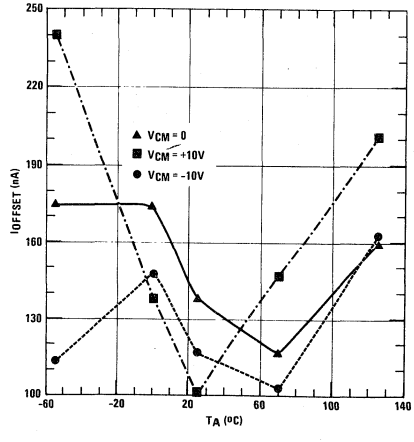
INPUT OFFSET VOLTAGE VS. COMMON VOLTAGE AND TEMPERATURE



BIAS CURRENT VS. COMMON MODE VOLTAGE AND TEMPERATURE

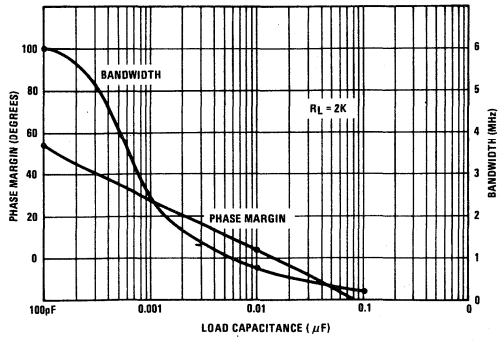


OFFSET CURRENT VS. COMMON MODE VOLTAGE AND TEMPERATURE

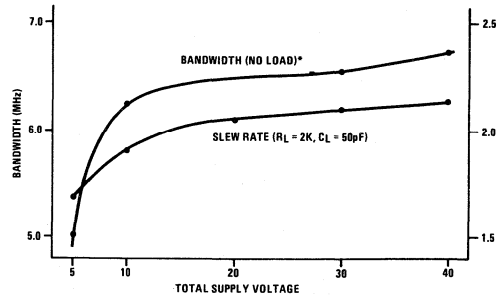


Typical Performance Curves (Continued)

BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE

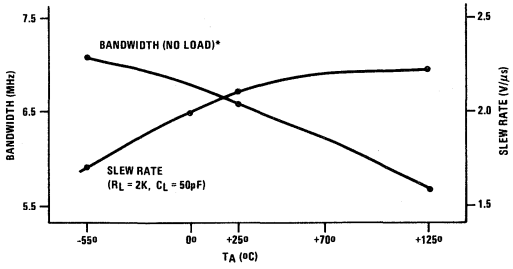


SLEW RATE AND BANDWIDTH VS. SUPPLY VOLTAGE



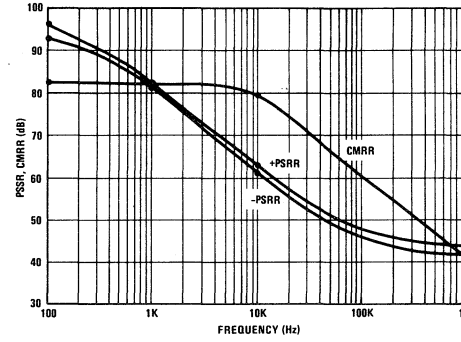
*Derate 0.5MHz for R_L = 2K

SLEW RATE AND BANDWIDTH VS. TEMPERATURE

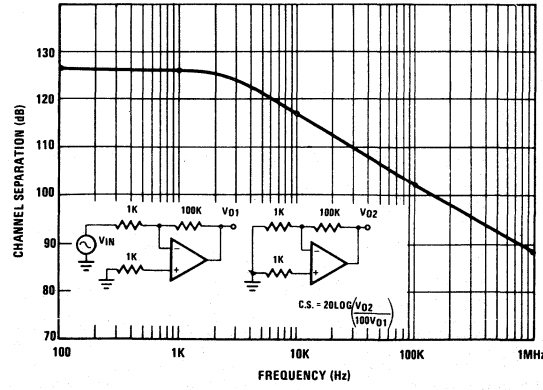


*Derate 0.5MHz for R_L = 2K

COMMON MODE REJECTION RATIO AND POWER SUPPLY REJECTION RATIO VS. FREQUENCY



CHANNEL SEPARATION VS. FREQUENCY



RAD-HARD 5

MULTIPLEXERS

HARRIS HS-508ARH/883S

July 1990

Radiation Hardened 8 Channel CMOS Analog Multiplexer With Overvoltage Protection

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Radiation Environment
  - Gamma Rate ($\dot{\gamma}$) ..... 1×10^8 Rad (Si)/s
  - Gamma Dose (γ) ..... 1×10^5 Rad (Si)
- Analog/Digital Overvoltage Protection
- Fail Safe with Power Loss (No Latchup)
- Break-Before-Make Switching
- DTL/TTL and CMOS Compatible
- Analog Signal Range ..... ±15V
- Access Time (Max) 1.0µs
- Supply Current at 1MHz Address Toggle (Typ.) 4mA
- Standby Power (Typ.) 7.5mW
- Dielectrically Isolated Device Islands

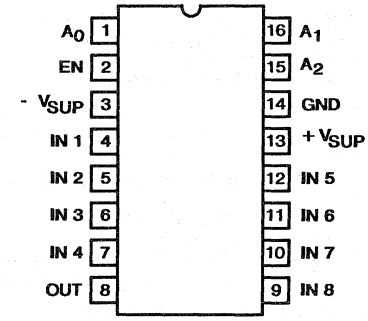
Description

The HS-508ARH/883S is a dielectrically isolated, radiation hardened, CMOS analog multiplexer incorporating an important feature; it withstands analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, it can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage current combine to produce low errors. Reference Application Notes 520 and 521, available from the Analog Products Division of Harris, for further information on the HS-508ARH/883S multiplexer in general.

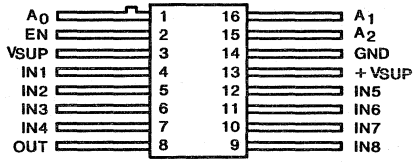
The HS-508ARH/883S has been specifically designed to meet exposure to radiation environments. Operation from -55°C to +125°C is guaranteed.

Pinouts

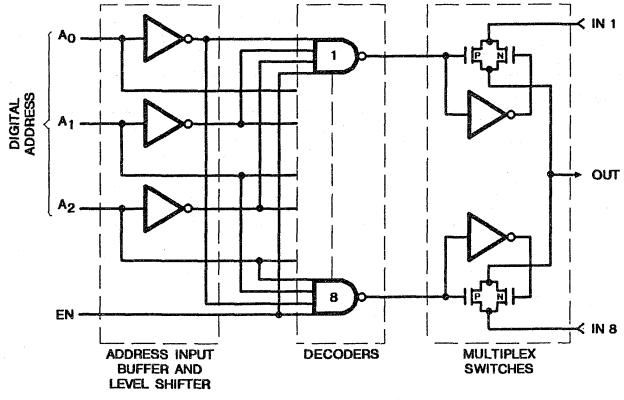
SIDEBRAZE
TOP VIEW



FLATPACK
TOP VIEW



Functional Diagram



Truth Table

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

5 MULTIPLEXERS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage Between Pins 1 and 27 ..... +40V
$+V_{SUPPLY}$ to Ground ..... +20V
$-V_{SUPPLY}$ to Ground ..... -20V
Analog Input Overvoltage:
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Digital Input Overvoltage:
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
Peak Current, S or D
Pulsed at 1ms, 10% Duty Cycle Maximum 40mA
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +275°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Sidebraze Package	84.9°C/W	22.8°C/W
Flatpack Package	85.0°C/W	11.1°C/W

Total Power Dissipation 725mW
Gate Count 253

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied.

Recommended Operating Conditions

Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... ±15V
Operating Temperature Range ..... -55°C to +125°C
Logic Low Level (V_{AL}) ..... +0.8V
Logic High Level (V_{AH}) ..... +4.0V

TABLE 1. HS-508ARH/883S D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address, or Enable Pins	I_{AH}	Measure Inputs Sequentially Ground All Unused Pins	1,2,3	+25°C, +125°C, -55°C	-1000	1000	nA
	I_{AL}						
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, All Unused Inputs & Output = -10V, V_{EN} = 0.8V	1	+25°C,	-10	10	nA
			2, 3	+125°C, -55°C	-50	50	nA
	$-I_{S(OFF)}$	V_S = -10V, All Unused Inputs & Output = +10V, V_{EN} =0.8V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-50	50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V All Unused Inputs = -10V	1	+25°C,	-10	10	nA
			2, 3	+125°C, -55°C	-250	250	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V All Unused Inputs = +10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-250	250	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch With Overvoltage Applied	$+I_{D(OFF)}$ Overvoltage	V_S =+25V, Measure V_D, V_{EN} = 0.8V, All Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-2000	2000	nA
	$-I_{D(OFF)}$ Overvoltage	V_S = -25V, Measure V_D, V_{EN} = 0.8V, All Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-2000	2000	nA
Leakage Current from an "ON" Driver into the Switch (Drain & Source)	$+I_{D(On)}$	$V_S = V_D$ = +10V, V_{EN} = 4.0V All Unused Inputs = -10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-250	250	nA
	$-I_{D(On)}$	$V_S = V_D$ = -10V, V_{EN} = 4.0V All Unused Inputs = +10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-250	250	nA
Analog Signal Range	V_S		7, 8A, 8B	+25°C, +125°C, -55°C	-15	+15	V

TABLE 1. HS-508ARH/883S D.C. ELECRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = 15V, V+ = +15V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch On Resistance	$+R_{(On)}$	V_S = +10V, I_{OUT} = -100µA, V_{EN} = 4.0V	1	+25°C	-	1500	ohms
			1, 2	-55°C, +125°C	-	1800	ohms
	$-R_{(On)}$	V_S = -10V, I_{OUT} = +4mA, V_{EN} = 4.0V	1	+25°C	-	1500	ohms
			1, 2	-55°C, +125°C	-	1800	ohms
Positive Supply Current	$I_{(+)}$	V_{EN} = 4.0V	1, 2, 3	-55°C, +25°C, +125°C	-	2	mA
Negative Supply Current	$I_{(-)}$	V_{EN} = 4.0V	1, 2, 3	-55°C, +25°C, +125°C	-1	-	mA
Positive Standby Supply Current	$+I_{max}$	V_{EN} = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	-	2	mA
Negative Standby Supply Current	$-I_{max}$	V_{EN} = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	-1	-	mA

TABLE 2. HS-508ARH/883S A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = 15V, V+ = +15V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	T_D	R_L = 1000 ohms, C_L = 50pF	9	+25°C	25	-	ns
			10, 11	-55°C, +125°C	5	-	ns
Propogation Delay Times: Address Inputs to I/O Channels	$T_{On(A)}$	R_L = 1M ohms, C_L = 50pF	9	+25°C	-	600	ns
	$T_{Off(A)}$		10, 11	-55°C, +125°C	-	1000	ns
Enable to I/O	$T_{On(EN)}$	R_L = 1000 ohms, C_L = 50pF	9	+25°C	-	600	ns
	$T_{Off(EN)}$		10, 11	-55°C, +125°C	-	1000	ns

TABLE 3. HS-508ARH/883S ELECTRICAL PERFORMANCE CHARACTERISTICS

Unless Otherwise Specified: V- = 15V, V+ = +15V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Address Input	C_A	V_{S+} = V_{S-} = 0V, f = 1MHz	3	+25°C	-	7	pF
Capacitance Channel Input	$C_{S(Off)}$	V_{S+} = V_{S-} = 0V, f = 1MHz	3	+25°C	-	7	pF
Capacitance Channel Output	$C_{D(Off)}$	V_{S+} = V_{S-} = 0V, f = 1MHz	3	+25°C	-	25	pF
Off Isolation	V_{ISO}	V_{EN} = 0.8V, f = 500KHz, C_L = 7pF, R_L = 1K ohms, V_S = 3.0V_{RMS}	3, 4	+25°C	45	-	dB

NOTES: 3. The parameters listed in this table are controlled via design or process parameters and not directly tested. These parameters are characterized upon initial design changes which would affect these characteristics.

4. Worst case isolation occurs on channel 4 due to proximity of the output pins.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	METHOD	GROUP A SUBGROUPS PER METHOD 5005, TABLE'S 1 AND 2
Interim Electrical Parameters	5004	1
Final Electrical Test Parameters	5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11 (Functional Tests) [1]
Group A Test Requirements	5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B5 Endpoint Electrical Parameters	5005	1, 2, 3 [2]
Group B6 Endpoint Electrical Parameters	5005	1, 7
Groups D Endpoint Electrical Parameters	5005	1, 7
Group E2 Endpoint Electrical Parameters	5005	1, 7 [3]

[1] PDA applies to subgroup 1 and delta limits.
[2] Subgroups 1, 2, 3 are datalogged.
[3] Endpoints are datalogged pre- and post-irradiation testing.

TABLE 5. HS-508ARH/883S POST 100K RAD (si) ELECTRICAL SPECIFICATIONS

Tested, per MIL-STD 883. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{AH} = +4.5V, V_{AL} = 0.5V

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address, or Enable Pins	I_{AH}	Measure Inputs Sequentially, Ground All Unused Pins	1	+25°C	-1000	1000	nA
	I_{AL}						
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, All Unused Inputs & Output = -10V, V_{EN} = 0.8V	1	+25°C	-50	50	nA
	$-I_{S(OFF)}$	V_S = -10V, All Unused Inputs & Output = +10V, V_{EN} = 0.8V	1	+25°C	-50	50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V All Unused Inputs = -10V	1	+25°C,	-250	250	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V All Unused Inputs = +10V	1	+25°C	-250	250	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch With Overvoltage Applied	$+I_{D(OFF)}$ Overvoltage	V_S = +25V, Measure V_D, V_{EN} = 0.8V, All Unused Inputs tied to GND	1	+25°C	-2000	2000	nA
	$-I_{D(OFF)}$ Overvoltage	V_S = -25V, Measure V_D, V_{EN} = 0.8V, All Unused Inputs tied to GND	1	+25°C	-2000	2000	nA
Leakage Current from an "ON" Driver into the Switch (Drain & Source)	$+I_{D(On)}$	V_S = V_D = +10V, V_{EN} = 4.0V All Unused Inputs = -10V	1	+25°C	-1000	1000	nA
	$-I_{D(On)}$	V_S = V_D = -10V, V_{EN} = 4.0V All Unused Inputs = +10V	1	+25°C	-1000	1000	nA
Switch On Resistance	$+R_{(On)}$	V_S = +10V, I_{OUT} = -100µA, V_{EN} = 4.0V	1	+25°C	-	1500	ohms
	$-R_{(On)}$	V_S = -5V, I_{OUT} = +4mA, V_{EN} = 4.0V	1	+25°C	-	1500	ohms

TABLE 5. HS508ARH/883S POST 100K RAD (si) ELECTRICAL SPECIFICATIONS (Continued)

Tested, per MIL-STD 883. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Positive Supply Current	$I_{(+)}$	V_{EN} = 4.0V	1	+25°C	-	2	mA
Negative Supply Current	$I_{(-)}$	V_{EN} = 4.0V	1	+25°C	-1	-	mA
Positive Standby Supply Current	$+I_{max}$	V_{EN} = 0.8V	1	+25°C	-	2	mA
Negative Standby Supply Current	$-I_{max}$	V_{EN} = 0.8V	1	+25°C	-1	-	mA

TABLE 6. HS-508ARH/883S DC POST BURN-IN DELTA ELECTRICAL SPECIFICATIONS (DC)

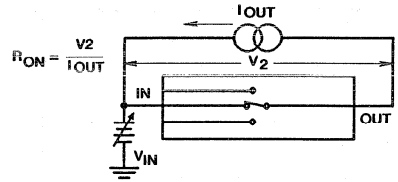
Guaranteed, per MIL-STD 883. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address, or Enable Pins	I_{AH}	Measure Inputs Sequentially, Ground All Unused Pins	1	+25°C	-100	100	nA
	I_{AL}						
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, All Unused Inputs & Output = -10V, V_{EN} = 0.8V	1	+25°C,	-20	20	nA
	$-I_{S(OFF)}$	V_S = -10V, All Unused Inputs & Output = +10V, V_{EN} =0.8V	1	+25°C	-20	20	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V All Unused Inputs = -10V	1	+25°C,	-20	20	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V All Unused Inputs = +10V	1	+25°C	-20	20	nA
Leakage Current from an "ON" Driver into the Switch (Drain & Source)	$+I_{D(On)}$	V_S = V_D = +10V, V_{EN} = 4.0V All Unused Inputs = -10V	1	+25°C	-20	20	nA
	$-I_{D(On)}$	V_S = V_D = -10V, V_{EN} = 4.0V All Unused Inputs = +10V	1	+25°C	-20	20	nA
Switch On Resistance	$+R_{(On)}$	V_S = +10V, I_{OUT} = -100µA, V_{EN} = 4.0V	1	+25°C	-150	-150	ohms
	$-R_{(On)}$	V_S = -10V, I_{OUT} = +4mA, V_{EN} = 4.0V	1	+25°C	-150	-150	ohms
Positive Supply Current	$I_{(+)}$	V_{EN} = 4.0V	1	+25°C	-200	200	µA
Negative Supply Current	$I_{(-)}$	V_{EN} = 4.0V	1	+25°C	-100	100	µA
Positive Standby Supply Current	$+I_{max}$	V_{EN} = 0.8V	1	+25°C	-200	200	µA
Negative Standby Supply Current	$-I_{max}$	V_{EN} = 0.8V	1	+25°C	-100	100	µA

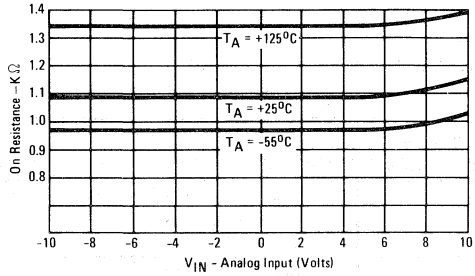
Performance Characteristics and Test Circuits

Unless otherwise specified: $T_A = +25^oC$, $V_{SUPPLY} = +15V$, $V_{AH} = +4V$, $V_{AL} = +0.8V$

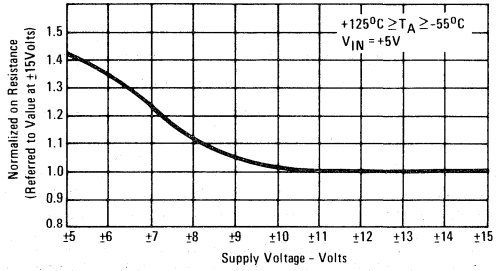
ON RESISTANCE VS. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



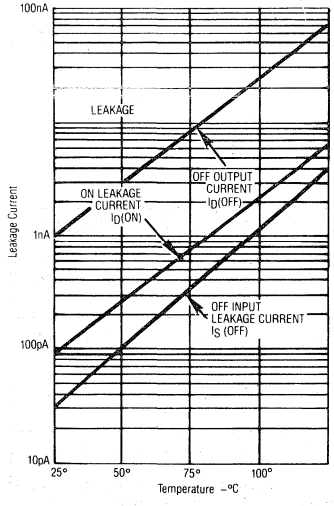
ON RESISTANCE VS. ANALOG INPUT VOLTAGE



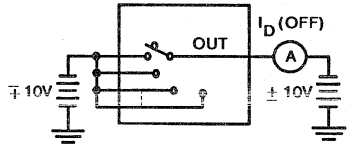
NORMALIZED ON RESISTANCE VS. SUPPLY VOLTAGE



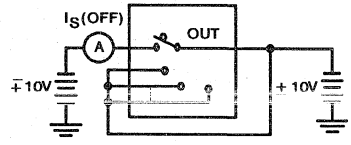
LEAKAGE CURRENT VS. TEMPERATURE



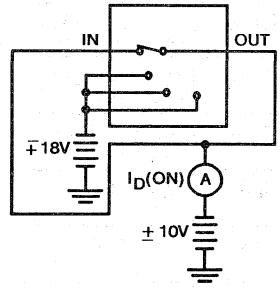
$I_{D(OFF)}$ LEAKAGE CURRENT VS. TEMPERATURE



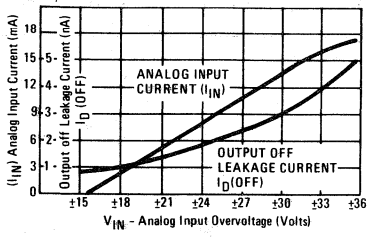
$I_{S(OFF)}$ LEAKAGE CURRENT VS. TEMPERATURE

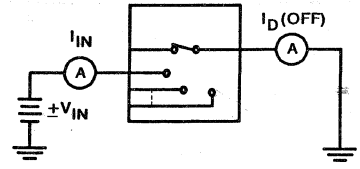


ON LEAKAGE CURRENT VS. TEMPERATURE



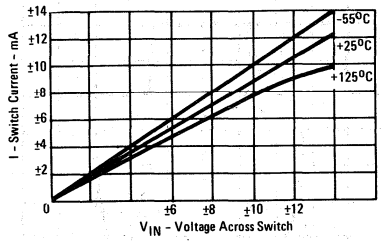
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



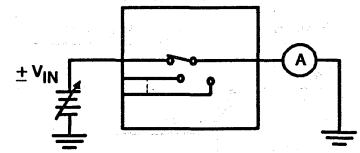


Performance Characteristics and Test Circuits

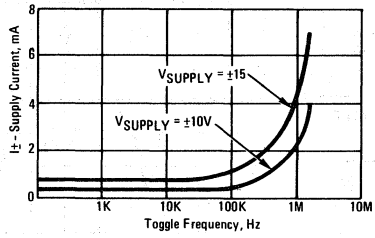
ON CHANNEL CURRENT VS. VOLTAGE



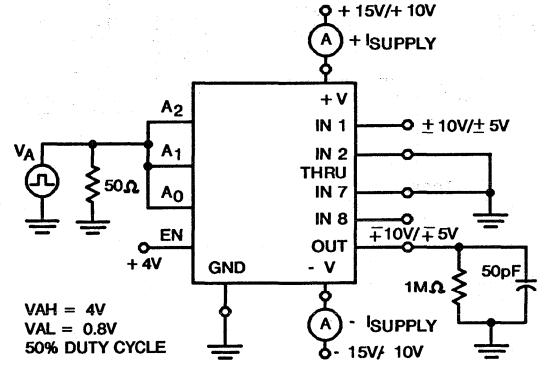
ON CHANNEL CURRENT VS. VOLTAGE



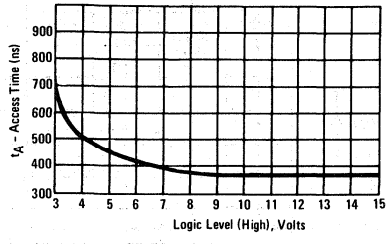
SUPPLY CURRENT VS. TOGGLE FREQUENCY



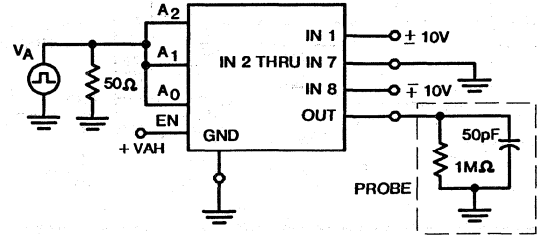
SUPPLY CURRENT VS. TOGGLE FREQUENCY



ACCESS TIME VS. LOGIC LEVEL (HIGH)



ACCESS TIME VS. LOGIC LEVEL (HIGH)

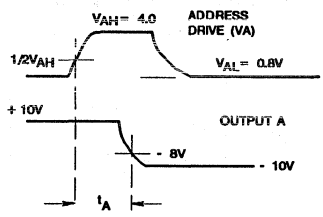


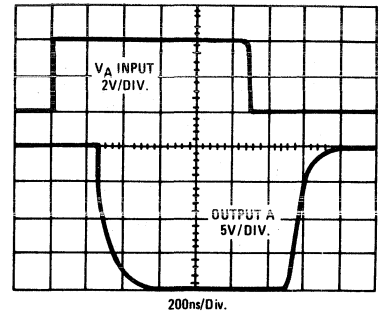
5

MULTIPLEXERS

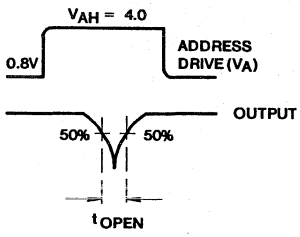
Switching Waveforms

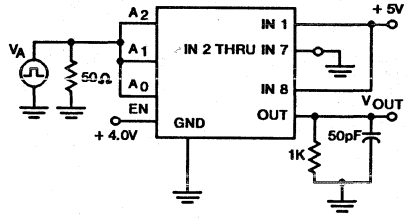
ACCESS TIME

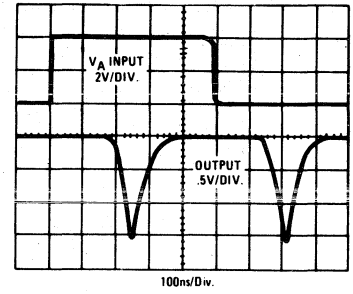




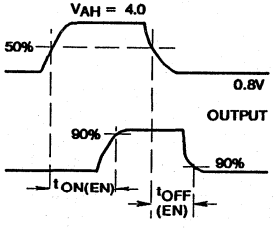
BREAK BEFORE MAKE DELAY (t_{OPEN})

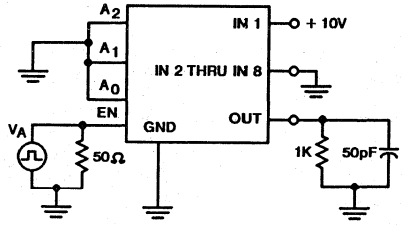


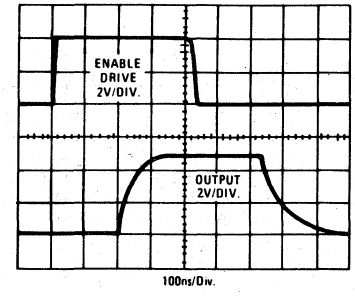




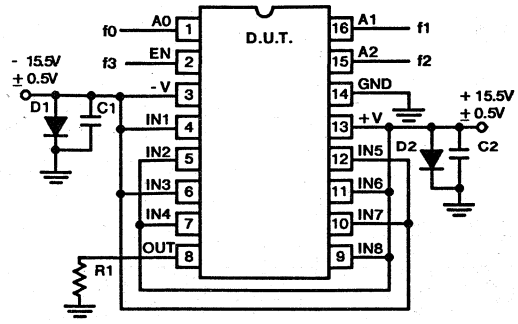
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)





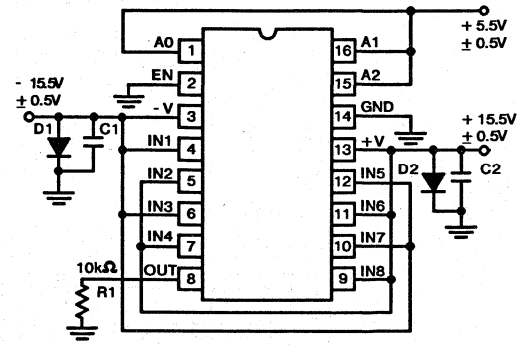


Burn-In Circuits



DYNAMIC BURN-IN AND LIFE TEST CIRCUIT

NOTES:
R1 = 10K ohms ±5%, ½ or ¼ watt (per socket)
C1 = C2 = 0.01µF minimum (per socket) or 0.1µF minimum (per row)
D1 = D2 = 1N4002 (or equivalent)
f0 = 100KHz; f1 = f0/2; f2 = f0/4; f3 = f0/8; 50% Duty Cycle
VIL = 0.8V max; VIH = 4.0V min.



STATIC BURN-IN TEST CIRCUIT

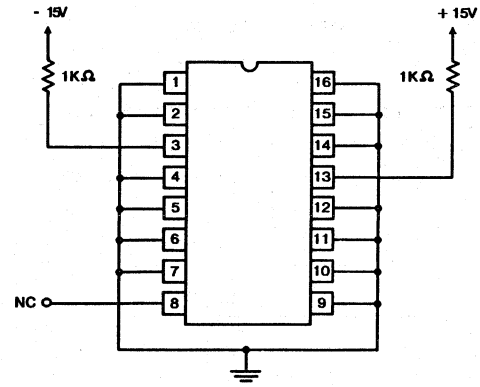
NOTES:
R1 = 10K ohms ±5%, ½ or ¼ watt (per socket)
C1 = C2 = 0.01µF minimum (per socket) or 0.1µF minimum (per row)
D1 = D2 = 1N4002 (or equivalent)

Radiation Qualifaction Procedure

1. SAMPLE SELECTION:
   Die Samples shall be selected for total dose testing per Mil-Std-883, Method 5005, Group E, Subgroup 2 for steady-state, total dose irradiation.
2. IRRADIATION QUALIFICATION PROCEDURE:
   All irradiation qualification testing is performed per Mil-Std-883, Method 1019.
3. RADIATION BIAS CIRCUIT:
   To the right is the radiation bias circuit used for this device qualification.

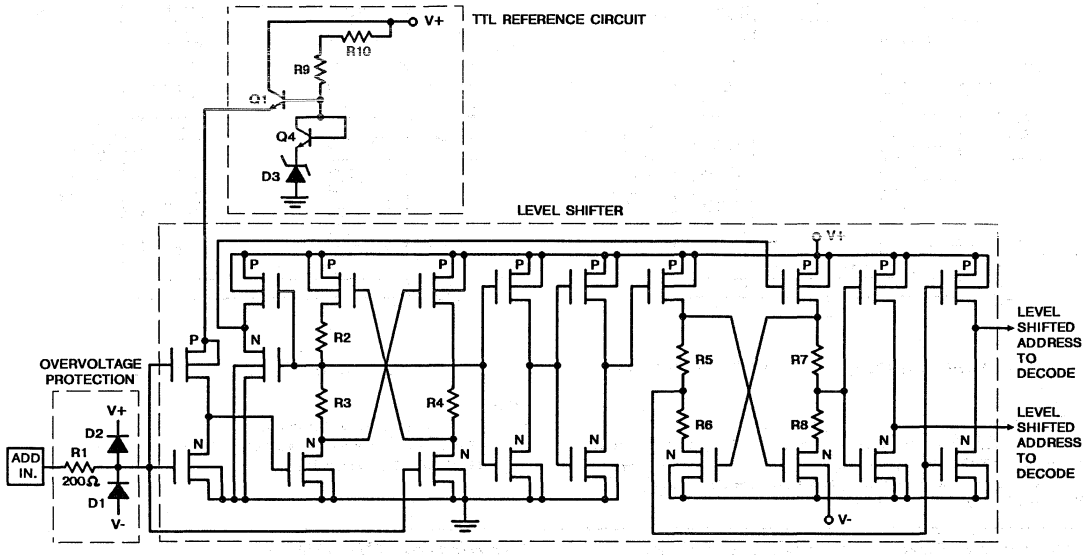
Irradiation Circuit

16 PIN DIP

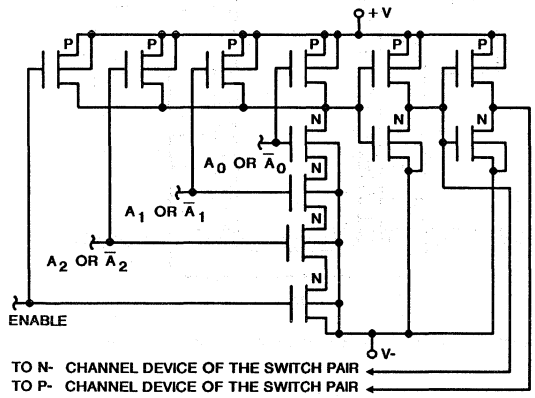


Schematic Diagrams

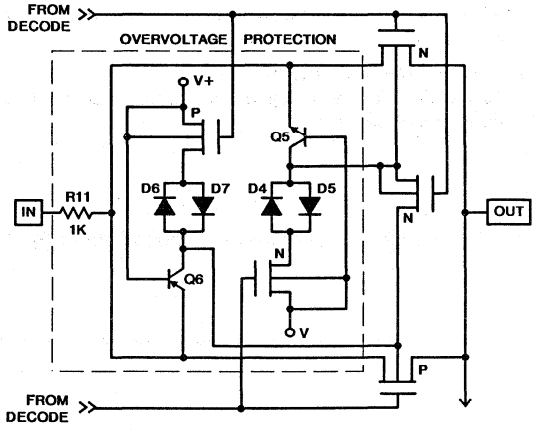
ADDRESS INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



Metallization Topology

DIE DIMENSIONS:
83 x 108 x 11 mils

METALLIZATION:
Type: Aluminum
Thickness: 12.5kÅ ± 2kÅ

GLASSIVATION:
Type: Silox
Thickness: 8kÅ ± 2kÅ

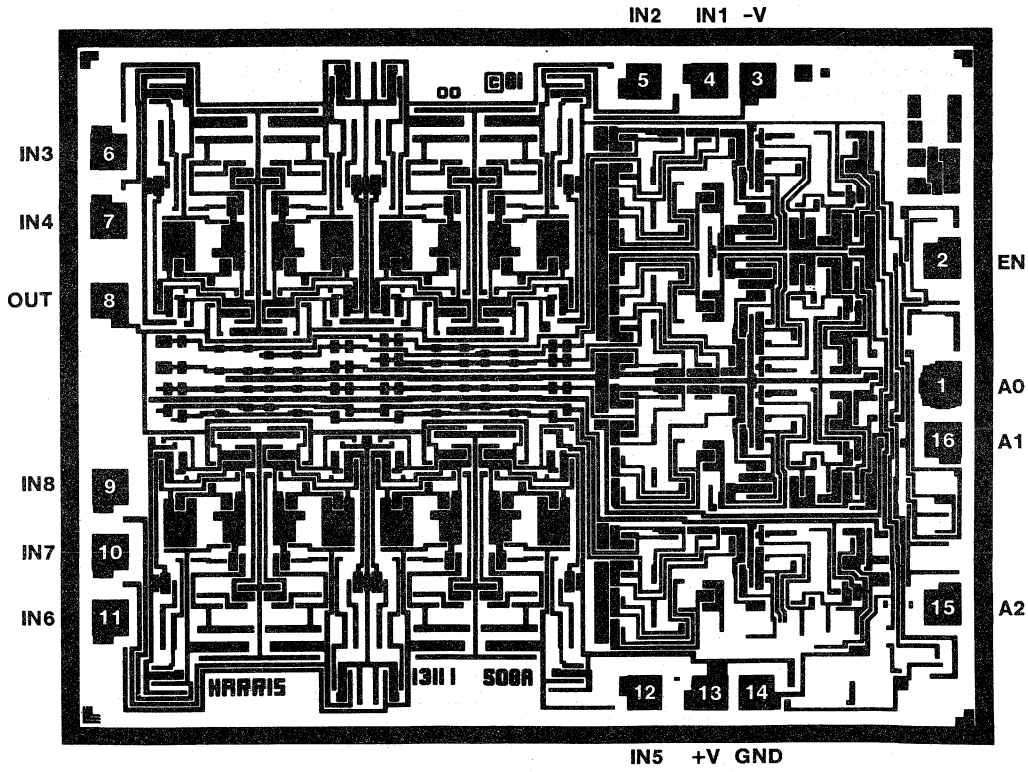
DIE ATTACH:
Material: Gold Eutectic
Temperature: Side Braze Dip ..... 335°C (MAX)
Flatpack ..... 460°C (MAX)

WORST CASE CURRENT DENSITY:
6.68e04 Amps/cm^2

PROCESS: CMOS-DI

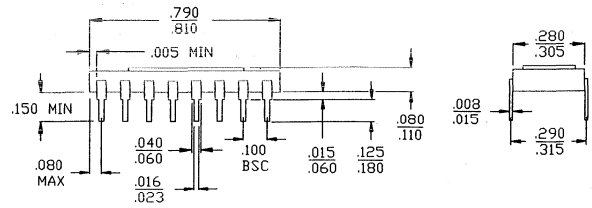
Metallization Mask Layout

HS-508ARH/883S



Packaging†

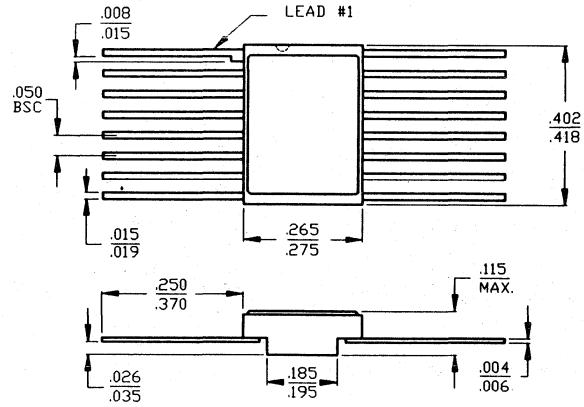
16 PIN CERAMIC SIDEBRAZE



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: D-2

16 PIN CERAMIC FLATPACK



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 F-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS HS-1840RH/883S

July 1990

Rad-Hard 16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

Features

- This Circuit is Processed in Accordance to MIL-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1 for Class S and Class B Devices
- Radiation Environment
  - Gamma Rate ($\dot{\gamma}$) ..... 1×10^8 Rad (Si)/s
  - Gamma Dose (γ) ..... 2×10^5 Rad (Si)
- Low Power Consumption 600µW
- Access Time 1000ns
- High Analog Input Impedance ..... 500MΩ During Power Loss (Open)
- Dielectrically Isolated Device Islands
- Excellent In Hi-Rel Redundant Systems
- Break-Before-Make Switching
- No Latch-Up

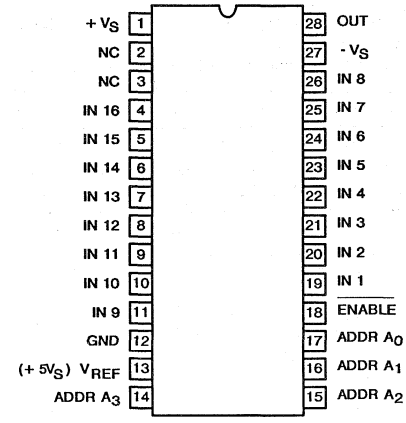
Description

The HS-1840RH/883S is a radiation hardened, monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. More significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection.

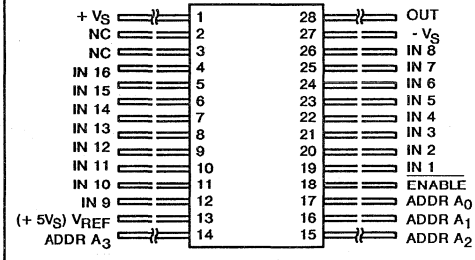
The HS-1840RH/883S has been specifically designed to meet exposure to radiation environments. It is available in a 28 pin Ceramic Sidebraze dual-in-line package and 28 pin Ceramic Flatpack. It is guaranteed operational from -55°C to +125°C.

Pinouts

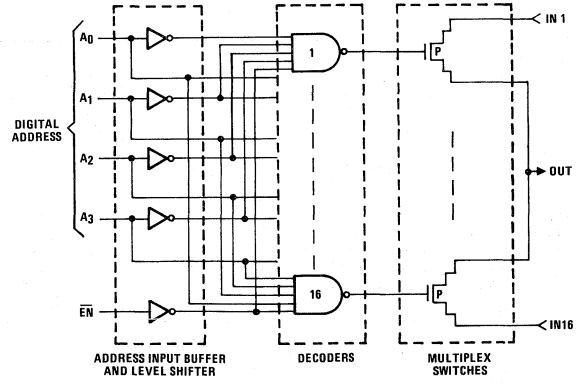
HS-1840RH/883S
(CERAMIC SIDEBRAZE DIP)
TOP VIEW



HS-1840RH/883S
(CERAMIC FLATPACK)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

Supply Voltage Between Pins 1 and 27 ..... +40V
$+V_{SUPPLY}$ to Ground ..... +20V
$-V_{SUPPLY}$ to Ground ..... -20V
V_{REF} to Ground ..... +20V
Analog Input Overvoltage:
$+V_S$ ..... +25V (Power On/Off)
$-V_S$ ..... -25V (Power On)
Digital Input Overvoltage:
$+V_{EN}$, $+V_A$ ..... V_{REF} +4V
$-V_{EN}$, $-V_A$ ..... GND -4V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (soldering 10 sec) ..... +275°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Sidebraze DIP Package	83.1°C/W	19.1°C/W
Ceramic Flatpack Package	49.1°C/W	16.5°C/W

Total Power Dissipation*:
Sidebraze DIP Package 1600mW
Ceramic Flatpack Package 1400mW
*For DIP Derate 20.4mW/°C above T_A = +95°C
For Flatpack Derate 18.5mW/°C above T_A = +95°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operations section of this specification is not implied.

Operating Conditions

Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... ±15V
Operating Temperature Range ..... -55°C to +125°C
V_{REC} (Pin 13) ..... +5V
Logic Low Level (V_{AL}) ..... +0.8V
Logic High Level (V_{DH}) ..... +4.0V

TABLE 1. HS-1840RH/883S D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{REF} = +5V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Analog Signal Range	V_S		7, 8A, 8B	-55°C, +25°C, +125°C	-5	+15	V
Input Leakage Current, Address, or Enable Pins	I_{AH} I_{AL}	Measure Inputs Sequentially Ground All Unused Pins V_{AL} = 0.8V, V_{AH} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	-1000	1000	nA
Leakage Current Into the Source Terminal of an "Off" Switch	$+I_{S(OFF)}$	V_S = +10V, All Unused Inputs & Output = -10V, V_{EN} = 4V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
	$-I_{S(OFF)}$	V_S = -10V, All Unused Inputs Output = +10V, V_{EN} = 4V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
Leakage Current into the Source Terminal of an "Off" Switch With Power "Off"	$+I_{S(OFF)}$ Power Off	V+, V-, V_{REF}, A_0, A_1, A_2, A_3, A_4, EN = GND, Unused Inputs Tied to GND, V_S = +25V	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-100	100	nA
Leakage Current Into the Source Terminal of an "Off" Switch With Overvoltage Applied	$+I_{S(OFF)}$ Overvoltage	V_S = +25V, V_D = 0V, V_{EN} = 4V All Unused Inputs Tied to GND	1, 2, 3	+25°C, +125°C, -55°C	-1000	1000	nA
	$-I_{S(OFF)}$ Overvoltage	V_S = -25V, V_D = 0V, V_{EN} = 4V All Unused Inputs Tied to GND	1, 2, 3	+25°C, +125°C, -55°C	-1000	1000	nA
Leakage Current Into the Drain Terminal of an "Off" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 4V All Unused Inputs = -10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 4V All Unused Inputs = +10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
Leakage Current Into the Drain Terminal of an "Off" Switch With Overvoltage Applied	$+I_{D(OFF)}$ Overvoltage	V_S = +25V, Measure V_D, V_{EN} = 4V All Unused Inputs to GND	1, 2, 3	+25°C, +125°C -55°C	-1000	1000	nA
	$-I_{D(OFF)}$ Overvoltage	V_S = -25V, Measure V_D, All Unused Inputs to GND	1, 2, 3	+25°C, +125°C -55°C	-1000	1000	nA
Leakage Current from an "On" Driver into the Switch (Drain and Source)	$+I_{D(ON)}$	V_S = +10V, V_D = +10V, V_{EN} = 0.8V All unused inputs = -10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
	$-I_{D(ON)}$	V_S = -10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = +10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA

TABLE 1. HS-1840RH/883S D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{REF} = +5V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch On Resistance	+15V $R_{(ON)}$	V_S = +15V, I_D = -1mA, V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C -55°C	50	1000	Ω
	-5V $R_{(ON)}$	V_S = -5V, I_D = +1mA, V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C -55°C	50	4000	Ω
Positive Supply Current	$I_{(+)}$	V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C -55°C	-	0.5	mA
Negative Supply Current	$I_{(-)}$	V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C -55°C	-0.5	-	mA
Positive Standby Supply Current	$+I_{SBY}$	V_{EN} = 4.0V	1, 2, 3	+25°C, +125°C -55°C	-	0.5	mA
Negative Standby Supply Current	$-I_{SBY}$	V_{EN} = 4.0V	1, 2, 3	+25°C, +125°C -55°C	-0.5	-	mA

TABLE 2. HS-1840RH/883S A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{REF} = +5V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	T_D	R_L = 1000Ω, C_L = 50pF	9	+25°C	25	-	ns
			10, 11	+125°C, -55°C	5	-	ns
Propagation Delay Times: Address Inputs to I/O Channels	$T_{ON(A)}$	R_L = 10MΩ, C_L = 50pF	9	+25°C	-	600	ns
	$T_{OFF(A)}$	R_L = 10MΩ, C_L = 50pF	10, 11	+125°C, -55°C	-	1000	ns
Enable to I/O	$T_{ON(EN)}$	R_L = 1000Ω, C_L = 50pF	9	+25°C	-	600	ns
	$T_{OFF(EN)}$	R_L = 1000Ω, C_L = 50pF	10, 11	+125°C, -55°C	-	1000	ns

TABLE 3. HS-1840RH/883S ELECTRICAL PERFORMANCE CHARACTERISTICS

Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{REF} = +5V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Address Input	C_A	$+V_S = -V_S$ = 0V, f = 1MHz	1	+25°C	-	7	pF
Capacitance Channel Input	$C_{S(OFF)}$	$+V_S = -V_S$ = 0V, f = 1MHz	1	+25°C	-	5	pF
Capacitance Channel Output	$C_{D(OFF)}$ $T_{OFF(EN)}$	$+V_S = -V_S$ = 0V, f = 1MHz	1	+25°C	-	50	pF
Off Isolation	V_{ISO}	V_{EN} = 4.0V, f = 500kHz, C_L = 7pF, R_L = 1kΩ, V_S = 3.0V_{RMS}	1	+25°C	45	-	dB

NOTE: 1. The parameters listed in Table 3 are controlled via design or process parameters and not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBBROUPS AND ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	GROUP A SUBGROUPS PER METHOD 5005 (SEE TABLES 1 & 2)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Test Parameters (Method 5004)	1, 2, 3, 9, 10,11 (Note 1) 7, 8A, 8B (Functional Tests)
Group A Test Requirements (Method 5005)	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B5 End-Point Electrical Parameters (Method 5005) (Class S Only)	1, 2, 3
Group B6 End-Point Electrical Parameters (Method 5005) (Class S Only)	1, 7
Group D End-Point Electrical Parameters (Method 5005)	1, 7
Group E2 End-Point Electrical Parameters	1, 7 (Note 2)

NOTES 1. PDA applies to subgroup 1 and delta limits.
2. Endpoints are datalogged pre- and post-irradiation testing.

TABLE 5. HS-1840RH/883S POST 200K RAD(Si) ELECTRICAL SPECIFICATIONS

Tested, per Mil-Std-883. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{REF} = +5V, V_{AH} = +4.5V, V_{AL} = 0.5V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address, or Enable Pins	I_{AH} I_{AL}	Measure Inputs Sequentially, Ground All Unused Pins	1	+25°C	-1000	1000	nA
Leakage Current into the Source Terminal of an "Off" Switch	$+I_{S(OFF)}$	V_S = +10V, All Unused Inputs & Output = -10V, V_{EN} = 4.5V	1	+25°C	-200	200	nA
	$-I_{S(OFF)}$	V_S = -10V, All Unused Inputs Output = +10V, V_{EN} = 4.5V	1	+25°C	-200	200	nA
Leakage Current into the Source Terminal of an "Off" Switch With Power "Off"	$+I_{S(OFF)}$ Power Off	V+, V-, V_{REF}, A_0, A_1, A_2, A_3, A_4, EN = GND, Unused Inputs Tied to GND, V_S = +25V	1	+25°C	-200	200	nA
Leakage Current Into the Source Terminal of an "Off" Switch With Overvoltage Applied	$+I_{S(OFF)}$ Overvoltage	V_S = +25V, V_D=0V, V_{EN}=4.5V All Unused Inputs Tied to GND	1	+25°C,	-2000	2000	nA
	$-I_{S(OFF)}$ Overvoltage	V_S = -25V, V_D=0V, V_{EN}=4.5V All Unused Inputs Tied to GND	1	+25°C,	-2000	2000	nA
Leakage Current Into the Drain Terminal of an "Off" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 4.5V All Unused Inputs = -10V	1	+25°C	-200	200	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 4.5V All Unused Inputs = +10V	1	+25°C	-200	200	nA
Leakage Current Into the Drain Terminal of an "Off" Switch With Overvoltage Applied	$+I_{D(OFF)}$ Overvoltage	V_S = +25V, Measure V_D, V_{EN} = 4.5V All Unused Inputs to GND	1	+25°C	-2000	2000	nA
	$-I_{D(OFF)}$ Overvoltage	V_S = -25V, Measure V_D, V_{EN} = 4.5V All Unused Inputs to GND	1	+25°C	-2000	2000	nA
Leakage Current from an "On" Driver into the Switch (Drain and Source)	$+I_{D(ON)}$	V_S=+10V, V_D = +10V, V_{EN} = 0.5V All Unused Inputs = -10V	1	+25°C	-200	200	nA
	$-I_{D(ON)}$	V_S = -10V, V_D = -10V, V_{EN} = 0.5V All Unused Inputs = +10V	1	+25°C	-200	200	nA

TABLE 5. HS-1840RH/883S POST 200K RAD(Si) ELECTRICAL SPECIFICATIONS (Continued)

Guaranteed, per Mil-Std-883 Method 1019. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{REF} = +5V, V_{AH} = 4.5V, V_{AL} = 0.5V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch On Resistance	+15V $R_{(ON)}$	V_S = +15V, I_D = -1mA, V_{EN} = 0.5V	1	+25°C	50	2000	Ω
	-5V $R_{(ON)}$	V_S = -5V, I_D = +1mA, V_{EN} = 0.5V	1	+25°C	50	7500	Ω
Positive Supply Current	$I_{(+)}$	V_{EN} = 0.5V	1	+25°C	-	0.75	mA
Negative Supply Current	$I_{(-)}$	V_{EN} = 0.5V	1	+25°C	-0.75	-	mA
Positive Standby Supply Current	$+I_{SBY}$	V_{EN} = 4.5V	1	+25°C	-	0.75	mA
Negative Standby Supply Current	$-I_{SBY}$	V_{EN} = 4.5V	1	+25°C	-0.75	-	mA

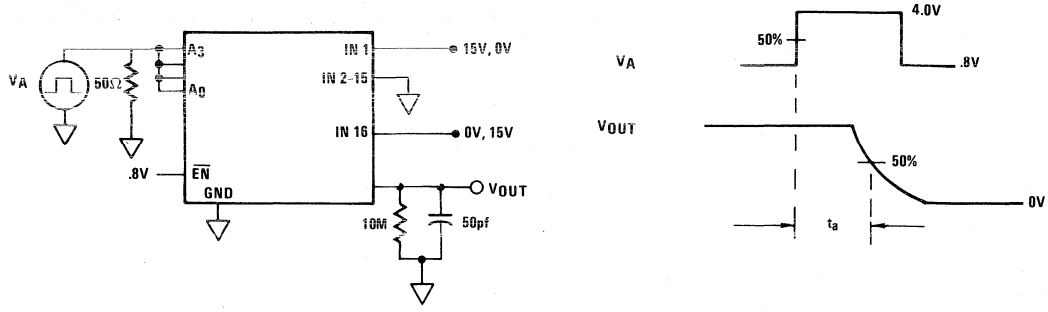
TABLE 6. HS-1840RH/883S DC POST BURN-IN DELTA ELECTRICAL SPECIFICATIONS

Guaranteed, per Mil-Std-883, Method 1019. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{REF} = +5V, V_{AH} = +4.0V, V_{AL} = 0.8V

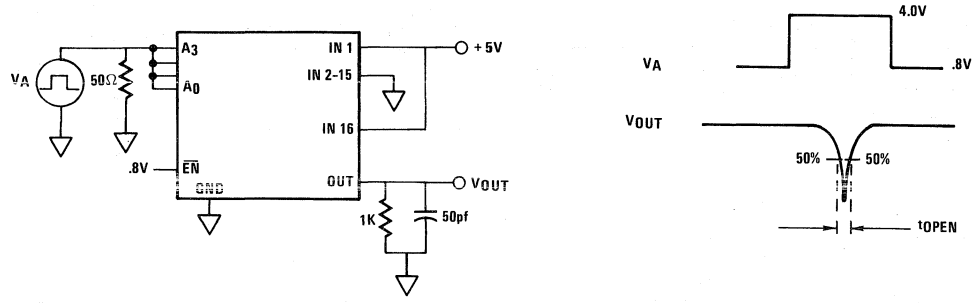
PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address, or Enable Pins	I_{AH} I_{AL}	Measure Inputs Sequentially, Ground All Unused Pins	1	+25°C	-100	100	nA
Leakage Current Into the Source Terminal of an "Off" Switch	$+I_{S(OFF)}$	V_S = +10V, All Unused Inputs & Output = -10V, V_{EN} = 4.0V	1	+25°C	-20	20	nA
	$-I_{S(OFF)}$	V_S = -10V, All Unused Inputs Output = +10V, V_{EN} = 4.0V	1	+25°C	-20	20	nA
Leakage Current Into the Drain Terminal of an "Off" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 4.0V All Unused Inputs = -10V	1	+25°C	-20	20	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 4.0V All Unused Inputs = +10V	1	+25°C	-20	20	nA
Leakage Current from an "On" Driver into the Switch (Drain and Source)	$+I_{D(ON)}$	V_S = +10V, V_D = +10V, V_{EN} = 0.8V All Unused Inputs = -10V	1	+25°C	-20	20	nA
	$-I_{D(ON)}$	V_S = -10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = +10V	1	+25°C	-20	20	nA
Switch On Resistance	+15V $R_{(ON)}$	V_S = +15V, I_D = -1mA, V_{EN} = 0.8V	1	+25°C	-100	100	Ω
	-5V $R_{(ON)}$	V_S = -5V, I_D = +1mA, V_{EN} = 0.8V	1	+25°C	-250	250	Ω
Positive Supply Current	$I_{(+)}$	V_{EN} = 0.8V	1	+25°C	-50	50	µA
Negative Supply Current	$I_{(-)}$	V_{EN} = 0.8V	1	+25°C	-50	50	µA
Positive Standby Supply Current	$+I_{SBY}$	V_{EN} = 4.0V	1	+25°C	-50	50	µA
Negative Standby Supply Current	$-I_{SBY}$	V_{EN} = 4.0V	1	+25°C	-50	50	µA

Performance Characteristics and Test Circuits

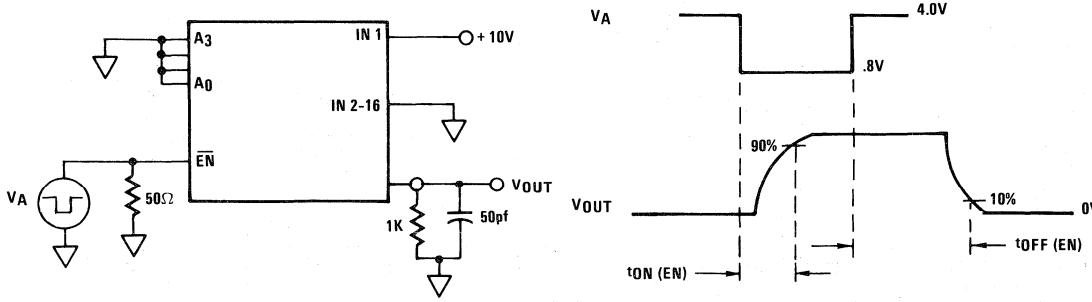
ACCESS TIME vs. LOGIC LEVEL (HIGH)



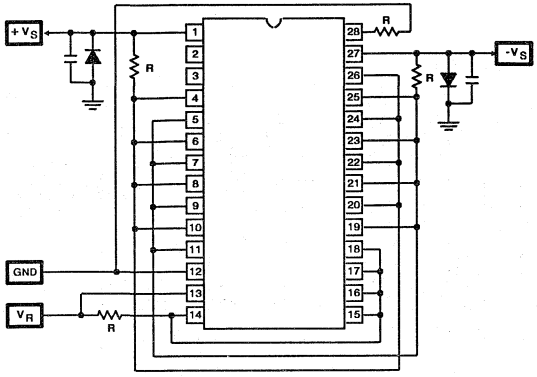
BREAK-BEFORE-MAKE DELAY



ENABLE DELAY tON(EN), tOFF(EN)

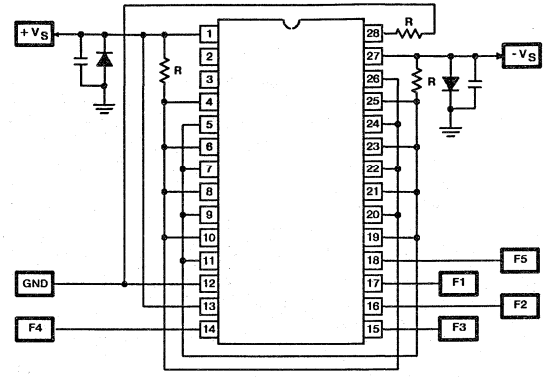


Burn-In/Life Test Circuits



STATIC BURN-IN TEST CIRCUIT

R1 - R4 = 1kΩ ± 5%, 1/4W, 4 per position
C1 = C2 = 0.01µF minimum, 1 each per socket, minimum
V_{S+} = 15.5V ± 0.5V, V_{S-} = -15.5V ± 0.5V, V_D = 15.5V ± 0.5V
I_{VS+}: 100µA per device; I_{VS-}: 100µA per device



DYNAMIC BURN-IN AND LIFE TEST CIRCUIT

R1 - R3 = 1kΩ ± 5%, 1/4W, 4 per position
C1 = C2 = 0.01µF ± 10%, 1 each per socket, minimum
D1 = D2 = IN4002, 1 each per board
Input signals: square wave, 50% duty cycle, 0 to 15V peak ± 10%.
F1 = 100kHz; F2 = F6/2; F3 = F1/4; F4 = F1/8; F5 = F1/16
t_{TLH} and t_{THL} < 1µs

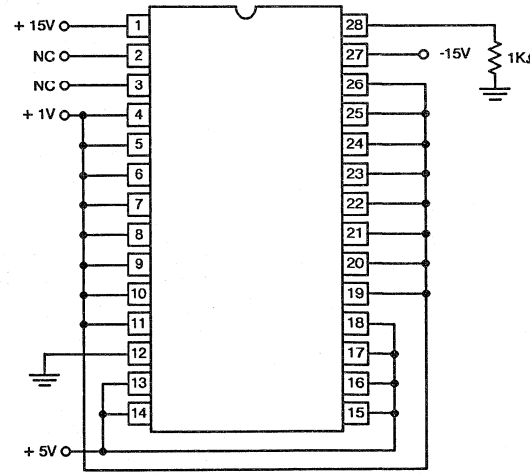
NOTES: 1. The above test circuits are utilized for both Sidebraze DIP and Ceramic Flatpack packages.
2. The Dynamic Test Circuit is utilized for all Life Testing.

Radiation Qualification Procedure

1. SAMPLE SELECTION:
   Die Samples shall be selected for total dose testing per Mil-Std-883, Method 5005, Group E, Subgroup 2 for steady-state, total dose irradiation.
2. IRRADIATION QUALIFICATION PROCEDURE:
   All irradiation qualification testing is performed per Mil-Std-883, Method 1019.
3. RADIATION BIAS CIRCUIT:
   To the right is the radiation bias circuit used for this device qualification.

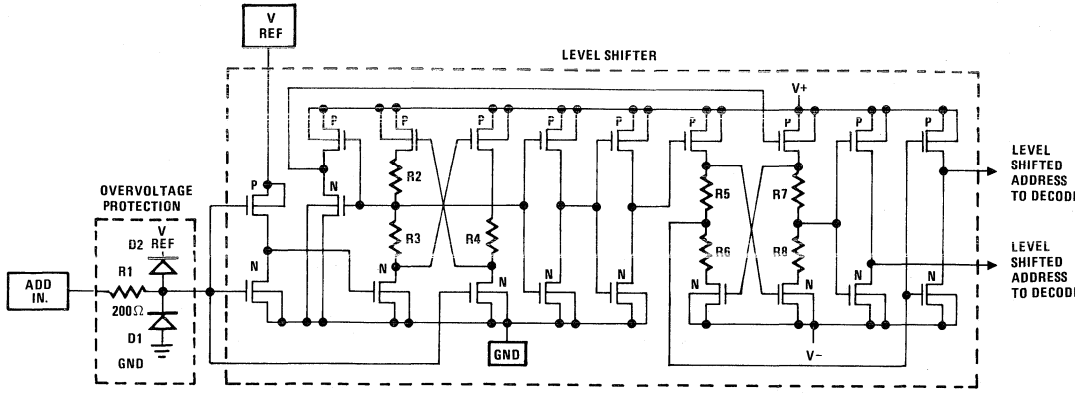
Irradiation Circuit

28 LEAD DIP

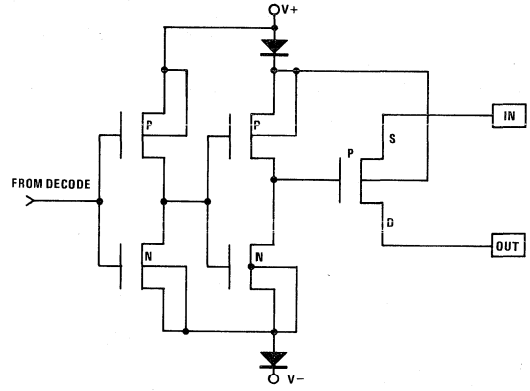


Schematic Diagrams

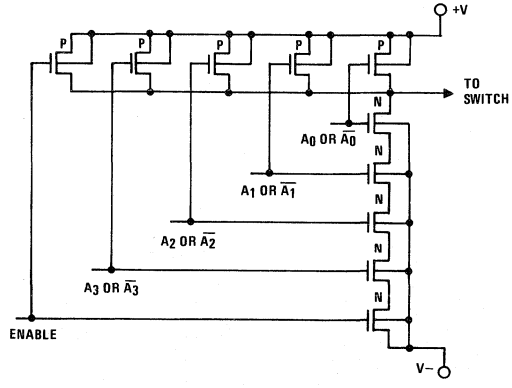
ADDRESS AND ENABLE INPUT BUFFER AND LEVER SHIFTER



MULTIPLEXER SWITCH



ADDRESS DECODER



Die Characteristics

DIE DIMENSIONS:
110 x 159 x 11 mils

METALLIZATION:
Type: Al
Thickness: 12.5kÅ ± 2kÅ

GLASSIVATION:
Type: Silox
Thickness: 8kÅ ± 2kÅ

DIE ATTACH:
Material: Gold Eutectic
Temperature: Sidebrazed Ceramic DIP — 460°C (Max)
Flatpack — 460°C

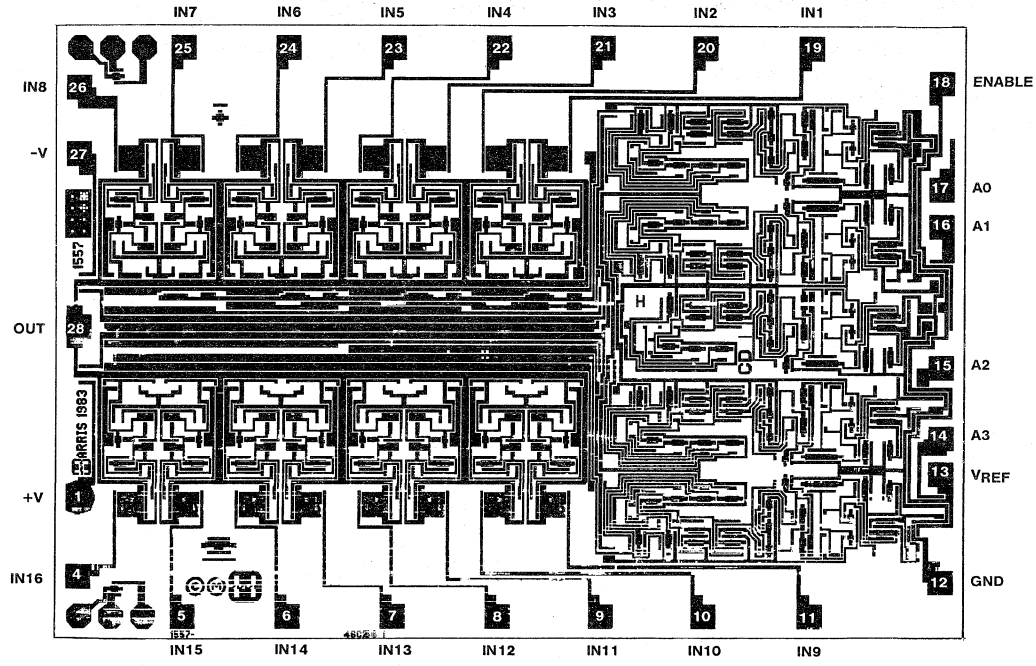
WORST CASE CURRENT DENSITY: 1.90e04 A/cm^2

LEAD TEMPERATURE (10 Seconds Soldering): < 275°C

PROCESS: CMOS - DI

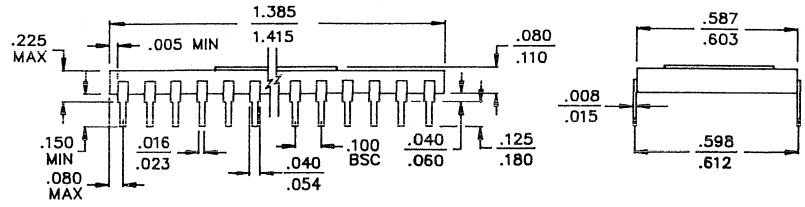
Metallization Mask Layout

HS-1840RH/883S



Packaging†

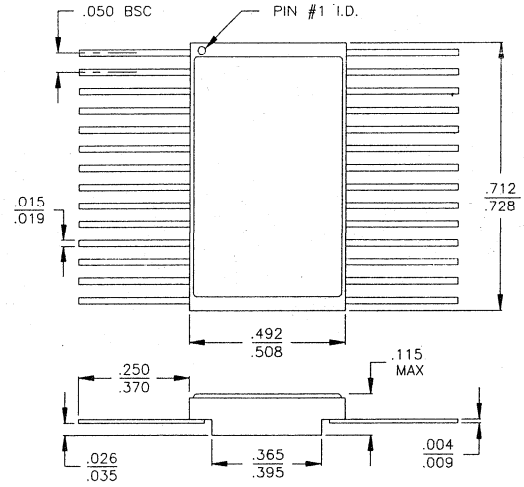
28 PIN CERAMIC SIDEBRAZE DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-10

28 PIN CERAMIC FLATPACK



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: F-11A

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

RAD-HARD 6

SWITCHES

HS-302RH/883S HS-303RH/883S HS-306RH/883S HS-307RH/883S HS-384RH/883S HS-390RH/883S

Radiation Hardened CMOS Analog Switches

July 1990

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1 for Class S and Class B Devices
- Radiation Hardened
  - Functional Total Dose Exceeds.....1×10^5 Rad Si
  - Low Leakage (Post Rad Typ. @ +25°C)..20nA Low
  - R_{ON} (Post Rad Typ. @ +25°C) 35Ω
- Pin for Pin Compatible with Harris HI-3XX Series Analog Switches
- Analog Signal Range ..... ±15V
- Low Leakage (Pre Rad Typ. @ +25°C) 90pA
- Low R_{ON} (Pre Rad Typ. @ +25°C)..... 30Ω
- No Latch Up
- Break-Before-Make Delay (Typ.) 65ns
- Versions for 5V and 15V Digital Systems
- Low Operating Power
- Military Temperature Range..... -55°C to +125°C

Applications

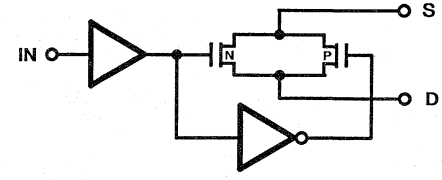
- Sample and Hold i.e. Low Leakage Switching
- Op Amp Gain Switching i.e. Low ON Resistance
- Switched Capacitor Filters
- Low Level Switching Circuits
- Satellites
- Nuclear Reactor Controls
- Military Environments

Description

The HS-3XXRH/883S family of analog switches are monolithic devices fabricated using Radiation Hardened CMOS technology and the Harris dielectric isolation process for latch-up free operation. Improved total dose hardness is obtained by layout (thin oxide tabs extending to a channel stop) and processing (hardened gate oxide). These switches offer low-resistance switching performance for analog voltages up to the supply rails. "ON" resistance is low and stays reasonably constant over the full range of operating voltage and current. "ON" resistance also stays reasonably constant when exposed to radiation, being typically 30Ω pre-rad and 35Ω post 100K Rad-Si. All devices provide break-before-make switching.

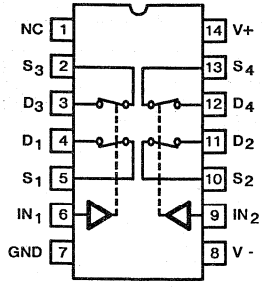
The 6 devices in this switch series are differentiated by type of switch action, pinout and digital logic levels. The HS-302/303/384/390RH/883S switches have 5V digital inputs while the HS-306/307RH/883S switches have 15V digital inputs. All devices are available in ceramic DIP packages. The HS-3XXRH/883S switches can directly replace the HI-3XX series devices.

Functional Diagram



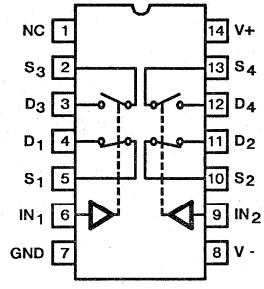
Pinouts (Switch States Are For Logic "1" Inputs) TOP VIEWS

DUAL DPST
HS-302RH/883S
HS-306RH/883S



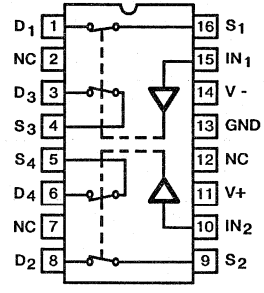
LOGIC	SWITCH 1 - 4
0	OFF
1	ON

DUAL SPDT
HS-303RH/883S
HS-307RH/883S



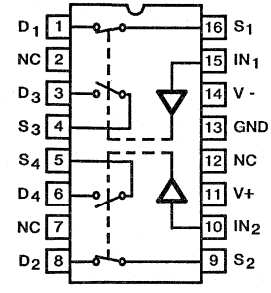
LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

DUAL DPST
HS-384RH/883S



LOGIC	SWITCH 1 - 4
0	OFF
1	ON

DUAL SPDT
HS-390RH/883S



LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage Between V+ and V- ..... +44V
$+V_{SUPPLY}$ to Ground ..... +22V
$-V_{SUPPLY}$ to Ground ..... -22V
Analog Input Overvoltage:
$+V_S$ ..... $+V_{SUPPLY}$ +1.5V
$-V_S$ ..... $-V_{SUPPLY}$ -1.5V
Digital Input Overvoltage:
$+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_A$ ..... $-V_{SUPPLY}$ -4V
Peak Current, S or D
Pulsed at 1ms, 10% Duty Cycle Max 40mA
Continuous Current 10mA
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (soldering 10 sec) ..... ≤ +300°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
14 Lead DIP	85.5°C/W	24.3°C/W
14 Lead Flatpack	85.0°C/W	11.5°C/W
16 Lead DIP	85.5°C/W	24.3°C/W
16 Lead Flatpack	85.0°C/W	11.5°C/W

Transistor Count 80
Total Power Dissipation:
14 Pin 588mW
16 Pin 685mW

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operations section of this specification is not implied.

Operating Conditions

Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... ±15V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. HS-302RH/303RH/384RH/390RH/883S D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"Switch On" Resistance	$+R_{DS}$	V_D = 10V, I_S = -10mA, S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
	$-R_{DS}$	V_D = -10V, I_S = 10mA, S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	$+I_{S(OFF)}$	V_S = +14V, V_D = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	$-I_{S(OFF)}$	V_S = -14V, V_D = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Leakage Current into the Drain Terminal of an "Off" Switch	$+I_{D(OFF)}$	V_S = -14V, V_D = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	$-I_{D(OFF)}$	V_S = +14V, V_D = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Leakage Current from an "On" Driver Into the Switch (Drain and Source)	$+I_{D(ON)}$	$V_S = V_D$ = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	$-I_{D(ON)}$	$V_S = V_D$ = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Address Current	I_{AL}	All Channels V_A = 0.8V	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-1	1	µA
High Level Input Address Current	I_{AH}	All Channels V_A = 0.8V	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-1	1	µA
Positive Supply Current	$I_{(+)}$	All Channels V_A = 0.8V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-	0.5	mA
			2, 3	-55°C to +125°C	-	1	mA
Negative Supply Current	$I_{(-)}$	All Channels V_A = 0.8V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA

TABLE 1. HS-306RH/307RH/883S D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{AH} = +11.0V, V_{AL} = 3.5V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"Switch On" Resistance	$+R_{DS}$	V_D = 10V, I_S = -10mA, S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
	$+R_{DS}$	V_D = -10V, I_S = 10mA, S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	$+I_{S(OFF)}$	V_S = +14V, V_D = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	$-I_{S(OFF)}$	V_S = -14V, V_D = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Leakage Current into the Drain Terminal of an "Off" Switch	$+I_{D(OFF)}$	V_S = -14V, V_D = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	$-I_{D(OFF)}$	V_S = +14V, V_D = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Leakage Current from an "On" Driver Into the Switch (Drain and Source)	$+I_{D(ON)}$	V_S = V_D = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	$-I_{D(ON)}$	V_S = V_D = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Address Current	I_{AL}	All Channels V_A = 3.5V	1	+25°C	-1	1	µA
			1, 2	-55°C to +125°C	-1	1	µA
High Level Input Address Current	I_{AH}	All Channels V_A = 11V	1	+25°C	-1	1	µA
			1, 2	-55°C to +125°C	-1	1	µA
Positive Supply Current	$I_{(+)}$	All Channels V_A = 0V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
		All Channels V_A = 0V	1	+25°C	-	10	µA
		All Channels V_A = 15V	2, 3	-55°C to +125°C	-	100	µA
Negative Supply Current	$I_{(-)}$	All Channels V_A = 0V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA
		All Channels V_A = 15V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA

TABLE 2. HS-302RH/303RH/384RH/390RH/883S A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{AH} = +4.0V, V_{AL} = 0V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay (HS-303RH & 390RH Only)	T_{OPEN}	R_L = 300Ω, C_L = 33pF, V_S = +3V, V_{AH} = 5V	9	+25°C	30	150	ns
			10, 11	-55°C to +125°C	-	300	ns
Switch Turn "On" Time	T_{ON}	R_L = 300Ω, C_L = 33pF, V_S = +3V	9	+25°C	-	300	ns
			10, 11	-55°C to +125°C	-	500	ns
Switch Turn "Off" Time	T_{OFF}	R_L = 300Ω, C_L = 33pF, V_S = +3V	9	+25°C	-	250	ns
			10, 11	-55°C to +125°C	-	450	ns

TABLE 2. HS-306RH/307RH/883S A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: $V- = -15V$, $V+ = +15V$, $V_{AH} = +15.0V$, $V_{AL} = 0V$

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay (HS-307RH Only)	T_{OPEN}	$R_L = 300\Omega$, $C_L = 33pF$, $V_S = +3V$	9	+25°C	30	150	ns
			10, 11	-55°C to +125°C	-	300	ns
Switch Turn "On" Time	T_{ON}	$R_L = 300\Omega$, $C_L = 33pF$, $V_S = +3V$	9	+25°C	-	300	ns
			10, 11	-55°C to +125°C	-	500	ns
Switch Turn "Off" Time	T_{OFF}	$R_L = 300\Omega$, $C_L = 33pF$, $V_S = +3V$	9	+25°C	-	250	ns
			10, 11	-55°C to +125°C	-	450	ns

TABLE 3. HS-302RH/303RH/306RH/307RH/384RH/390RH/883S ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Unless Otherwise Specified: HS-302RH/303RH/384RH/390RH/883S $V- = -15V$, $V+ = +15V$, $V_{AH} = +4.0V$, $V_{AL} = 0V$
HS-306RH/307RH/883S $V- = -15V$, $V+ = +15V$, $V_{AH} = +15.0V$, $V_{AL} = 0V$

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch Input Capacitance	$C_{IS(OFF)}$	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	C_{C1}	$V_A = 0V$	1	+25°C	-	10	pF
	C_{C2}	$V_A = 15V$	1	+25°C	-	10	pF
Switch Output	C_{OS}	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	V_{ISO}	$V_{GEN} = 1V_{p-p}$, f = 1MHz	1	+25°C	40	-	dB
Crosstalk	V_{CR}	$V_{GEN} = 1V_{p-p}$, f = 1MHz	1	+25°C	40	-	dB
Charge Transfer	V_{CTE}	$V_S = GND$, $C_L = 0.01\mu F$	1	+25°C	-	15	mV

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. HS-302RH/303RH/306RH/307RH/384RH/390RH/883S APPLICABLE SUBGROUPS

MIL-STD-883 TEST REQUIREMENTS	GROUP A SUBGROUPS PER METHOD 5005 (SEE TABLES 1 & 2)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Test Parameters (Method 5004)	1, 2, 3, 9, 10,11 (Note 2) 7, 8A, 8B (Functional Tests)
Group A Test Requirements (Method 5005)	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B5 End-Point Electrical Parameters (Method 5005) (Class S Only)	1, 2, 3, 9, 10, 11 (Note 3)
Group B6 End-Point Electrical Parameters (Method 5005) (Class S Only)	1
Group C End-Point Electrical Parameters (Method 5005) (Class B Only)	1
Group D End-Point Electrical Parameters (Method 5005)	1
Group E2 End-Point Electrical Parameters (Method 5005)	1, 7 (Note 4)

NOTES 2. PDA applies to subgroup 1 and delta limits.
3. Subgroups 1, 2, 3 are datalogged; 9, 10 & 11 are go-no-go tests.
4. Endpoints are datalogged pre- and post-irradiation testing.

TABLE 5. HS-302RH/303RH/306RH/307RH/384RH/390RH/883S D.C. POST 100K RAD (Si) ELECTRICAL PARAMETERS

Tested Per Mil-Std-883. Unless Otherwise Specified: HS-302RH/303RH/384RH/390RH/883S V- = -15V, V+ = +15V, V_{AH} = +4.0V, V_{AL} = 0.8V
HS-306RH/307RH/883S V- = -15V, V+ = +15V, V_{AH} = +11.0V, V_{AL} = 3.5V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"Switch On" Resistance	$+R_{DS}$	V_D = 10V, I_S = -10mA, S1/S2/S3/S4	1	+25°C	-	60	Ω
	$-R_{DS}$	V_D = -10V, I_S = 10mA, S1/S2/S3/S4	1	+25°C	-	60	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	$+I_{S(OFF)}$	V_S = +14V, V_D = -14V, S1/S2/S3/S4	1	+25°C	-100	100	nA
	$-I_{S(OFF)}$	V_S = -14V, V_D = +14V, S1/S2/S3/S4	1	+25°C	-100	100	nA
Leakage Current into the Drain Terminal of an "Off" Switch	$+I_{D(OFF)}$	V_S = -14V, V_D = +14V, S1/S2/S3/S4	1	+25°C	-100	100	nA
	$-I_{D(OFF)}$	V_S = +14V, V_D = -14V, S1/S2/S3/S4	1	+25°C	-100	100	nA
Leakage Current from an "On" Driver Into the Switch (Drain and Source)	$+I_{D(ON)}$	$V_S = V_D$ = +14V, S1/S2/S3/S4	1	+25°C	-100	100	nA
	$-I_{D(ON)}$	$V_S = V_D$ = -14V, S1/S2/S3/S4	1	+25°C	-100	100	nA

TABLE 6. HS-302RH/303RH/384RH/390RH/883S D.C. POST BURN-IN DELTA ELECTRICAL SPECIFICATIONS

Guaranteed, Per Mil-Std-883. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{AH} = +4.0V, V_{AL} = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"Switch On" Resistance	$+R_{DS}$	V_D = 10V, I_S = -10mA, S1/S2/S3/S4	1	+25°C	-5	5	Ω
	$-R_{DS}$	V_D = -10V, I_S = 10mA, S1/S2/S3/S4	1	+25°C	-5	5	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	$+I_{S(OFF)}$	V_S = +14V, V_D = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	$-I_{S(OFF)}$	V_S = -14V, V_D = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Leakage Current into the Drain Terminal of an "Off" Switch	$+I_{D(OFF)}$	V_S = -14V, V_D = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	$-I_{D(OFF)}$	V_S = +14V, V_D = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Leakage Current from an "On" Driver Into the Switch (Drain and Source)	$+I_{D(ON)}$	$V_S = V_D$ = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	$-I_{D(ON)}$	$V_S = V_D$ = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Low Level Input Address Current	I_{AL}	All Channels V_A = 0.8V	1	+25°C	-100	100	nA
High Level Input Address Current	I_{AH}	All Channels V_A = 4.0V	1	+25°C	-100	100	nA
Positive Supply Current	$I_{(+)}$	All Channels V_A = 0.8V	1	+25°C	-1	1	µA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-0.1	0.1	mA
Negative Supply Current	$I_{(-)}$	All Channels V_A = 0.8V	1	+25°C	-1	1	µA
		V_{A1} = 0V, V_{A2} = 4.0V and V_{A1} = 4.0V, V_{A2} = 0V	1	+25°C	-1	1	µA

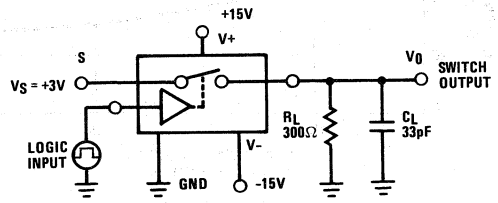
TABLE 6. HS-306RH/307RH/883S D.C. POST BURN-IN DELTA ELECTRICAL PARAMETERS (Continued)
Guaranteed, Per Mil-Std-883. Unless Otherwise Specified: V- = -15V, V+ = +15V, V_{AH} = +11.0V, V_{AL} = 3.5V

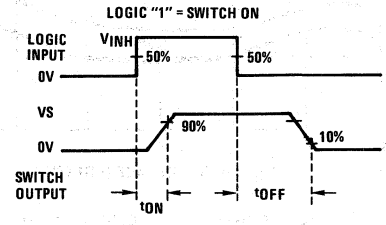
PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"Switch On" Resistance	$+R_{DS}$	V_D = 10V, I_S = -10mA, S1/S2/S3/S4	1	+25°C	-5	5	Ω
	$-R_{DS}$	V_D = -10V, I_S = 10mA, S1/S2/S3/S4	1	+25°C	-5	5	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	$+I_{S(OFF)}$	V_S = +14V, V_D = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	$-I_{S(OFF)}$	V_S = -14V, V_D = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Leakage Current into the Drain Terminal of an "Off" Switch	$+I_{D(OFF)}$	V_S = -14V, V_D = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	$-I_{D(OFF)}$	V_S = +14V, V_D = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Leakage Current from an "On" Driver Into the Switch (Drain and Source)	$+I_{D(ON)}$	V_S = V_D = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	$-I_{D(ON)}$	V_S = V_D = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Low Level Input Address Current	I_{AL}	All Channels V_A = 3.5V	1	+25°C	-100	100	nA
High Level Input Address Current	I_{AH}	All Channels V_A = 11V	1	+25°C	-100	100	nA
Positive Supply Current	$I_{(+)}$	All Channels V_A = 0V	1	+25°C	-1	1	µA
		All Channels V_A = 15V	1	+25°C	-1	1	mA
Negative Supply Current	$I_{(-)}$	All Channels V_A = 0V	1	+25°C	-1	1	µA
		All Channels V_A = 15V	1	+25°C	-1	1	µA

Test Circuits

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

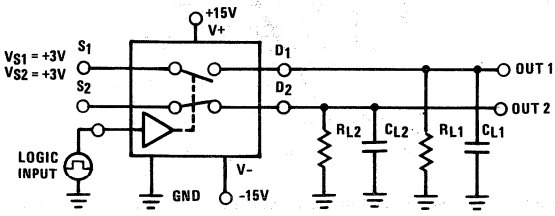
SWITCH TYPE	V_{INH}
HS-302RH/303RH/384RH/390RH/883S	4V
HS-306RH/307RH/883S	15V

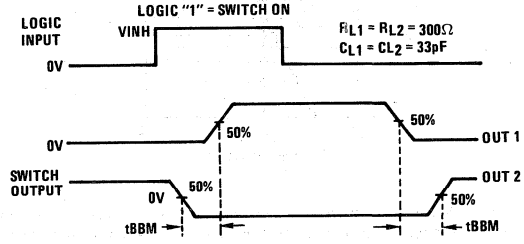




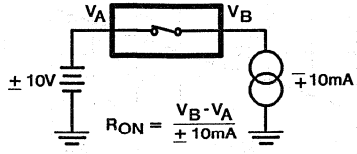
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

SWITCH TYPE	V_{INH}
HS-303RH/390RH/883S	5V
HS-307RH/883S	15V

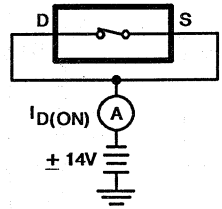




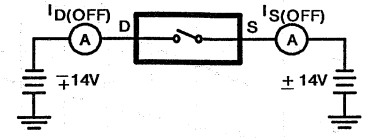
ON RESISTANCE TEST CIRCUIT (R_{ON})



ON LEAKAGE CURRENT TEST CIRCUIT ($I_{D_{ON}}$)

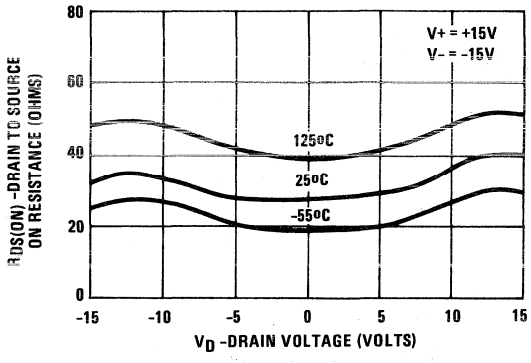


OFF LEAKAGE CURRENT TEST CIRCUIT ($I_{S_{OFF}}$, $I_{D_{OFF}}$)

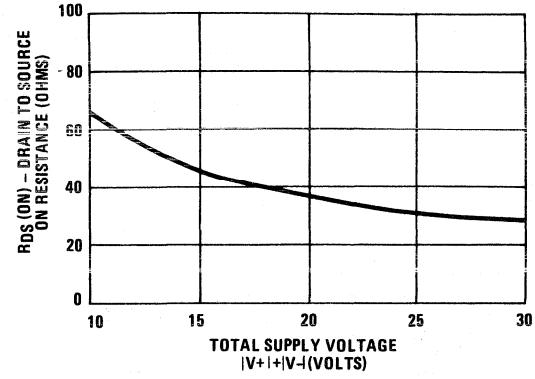


Performance Curves Typical Pre-Rad

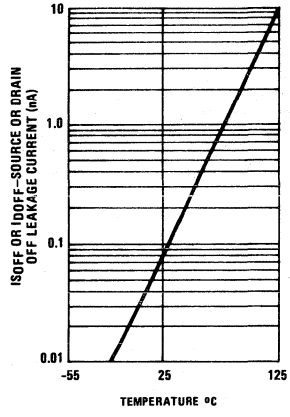
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



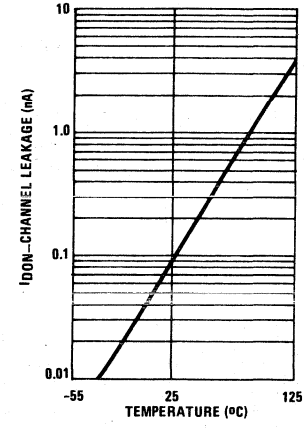
$R_{DS(ON)}$ vs. SUPPLY VOLTAGE



$I_{S(OFF)}$ OR $I_{D(OFF)}$ vs. TEMPERATURE

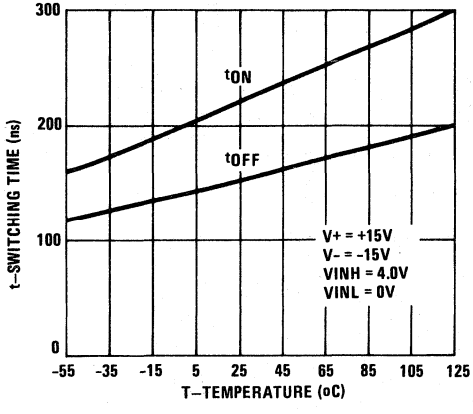


$I_{D(ON)}$ vs. TEMPERATURE *

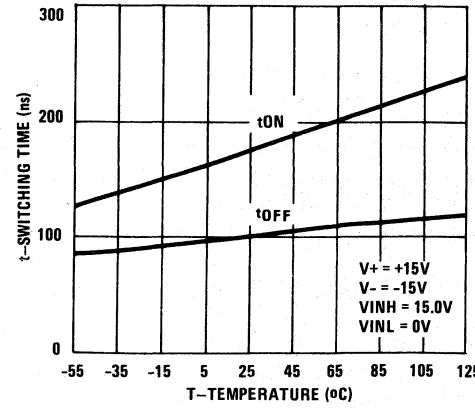


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

SWITCHING TIME vs. TEMPERATURE
HS-302RH/303RH/384RH/390RH/883S

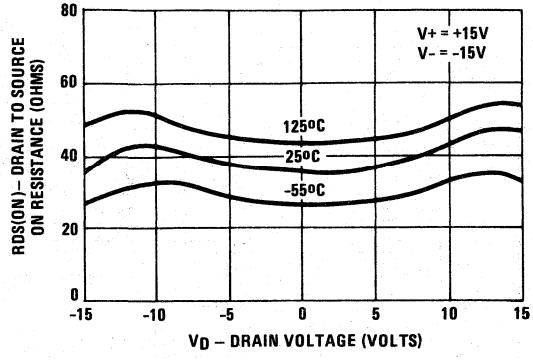


SWITCHING TIME vs. TEMPERATURE
HS-306RH/307RH/883S

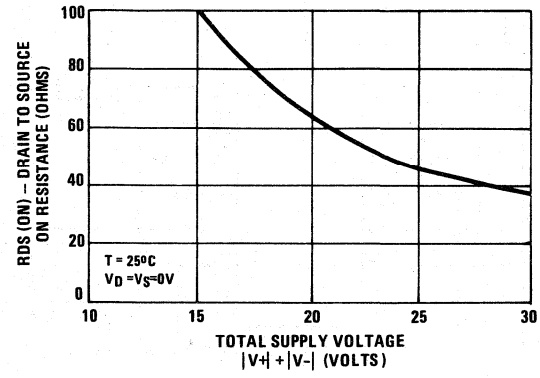


Performance Curves Typical Post Rad (100K Rad-Si)

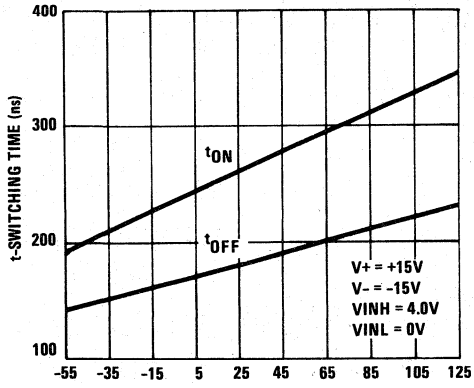
$R_{DS(ON)}$ vs. V_D AND TEMPERATURE



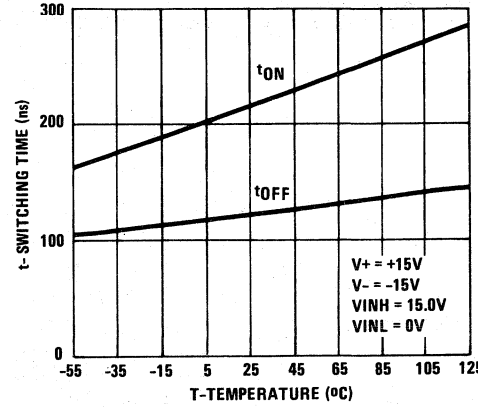
$R_{DS(ON)}$ vs. SUPPLY VOLTAGE



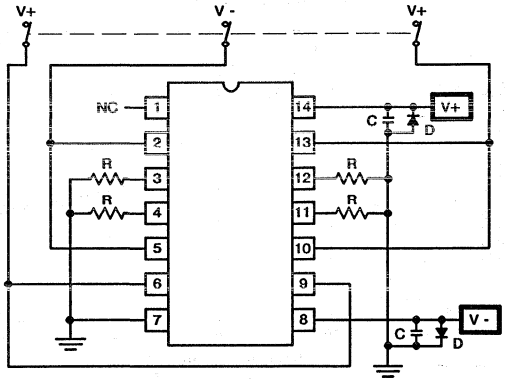
SWITCHING TIME vs. TEMPERATURE
HS-302RH/303RH/384RH/390RH/883S



SWITCHING TIME vs. TEMPERATURE
HS-306RH/307RH/883S

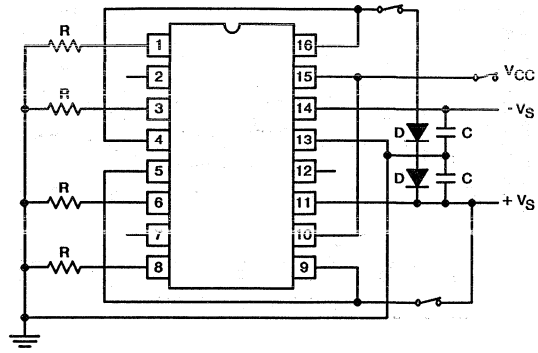


Burn-In Circuits



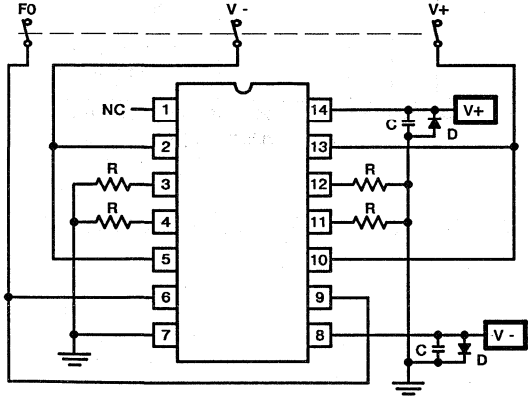
STATIC CONFIGURATION
HS-302RH/303RH/306RH/307RH/883S

R = 10KΩ ± 5%, 1/4W (4 per position)
C = 0.01μF minimum (per position) or 0.1μF minimum per row
D = IN4002 (or equivalent)
$+V_S$ = +15.5V ± 0.5V, $-V_S$ = −15.5V ± 0.5V



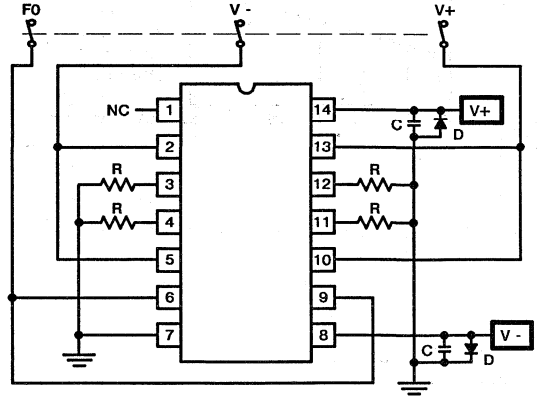
STATIC CONFIGURATION
HS-384RH/390RH/883S

R = 10KΩ ± 5%, 1/4W (4 per position)
C = 0.01μF minimum (per position) or 0.1μF minimum per row
D = IN4002 (or equivalent)
$+V_S$ = +15.5V ± 0.5V, $-V_S$ = −15.5V ± 0.5V
V_{CC} = +5.5V ± 0.5V



DYNAMIC CONFIGURATION
HS-302RH/303RH/883S

R = 10KΩ ± 5%, 1/4W (4 per position)
C = 0.01μF minimum (per position) or 0.1μF minimum per row
D = IN4002 (or equivalent)
F = 100kHz square wave, 50% duty cycle,
V_L = 0.8V (max), V_H = +13V to +15V
$+V_S$ = +15.5V ± 0.5V, $-V_S$ = −15.5V ± 0.5V



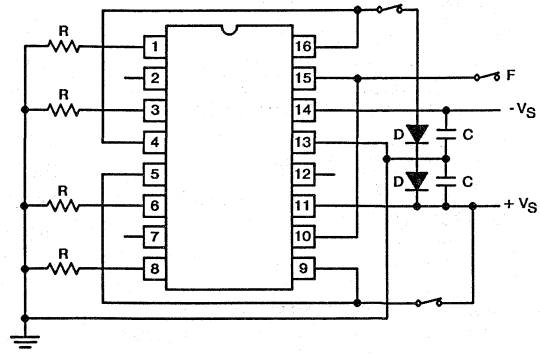
DYNAMIC CONFIGURATION
HS-306RH/307RH/883S

R = 10KΩ ± 5%, 1/4W (4 per position)
C = 0.01μF minimum (per position) or 0.1μF minimum per row
D = IN4002 (or equivalent)
F = 100kHz square wave, 50% duty cycle,
V_L = 0.8V (max), V_H = +13V to +15V
$+V_S$ = +15.5V ± 0.5V, $-V_S$ = −15.5V ± 0.5V

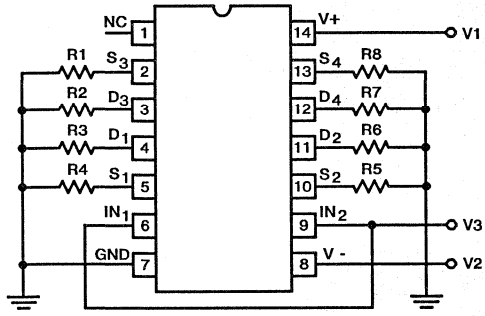
Burn-In Circuits (Continued)

DYNAMIC CONFIGURATION
HS-384RH/390RH/883S

R = 10KΩ ± 5%, 1/4W (4 per position)
C = 0.01µF minimum (per position) or 0.1µF minimum per row
D = IN4002 (or equivalent)
F = 100kHz square wave, 50% duty cycle,
V_L = 0.8V (max), V_H = +5.5V to +0.5V
$+V_S$ = +15.5V ± 0.5V, $-V_S$ = -15.5V ± 0.5V

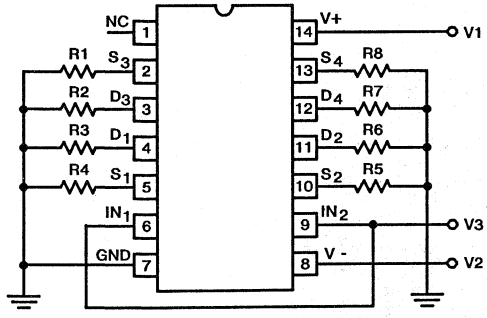


Irradiation Circuits



HS-302RH/303RH/883S

R1 - R8 = 10KΩ ± 5%, 1/4W
V1 = +15V ± 10%
V2 = -15V ± 10%
V3 = +5V ± 5%

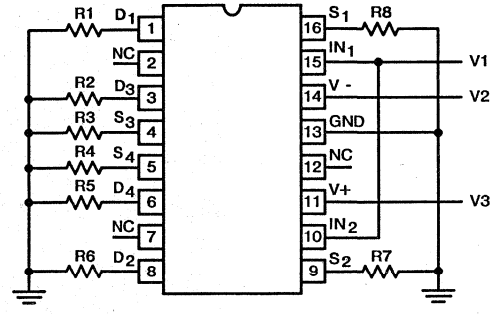


HS-306RH/307RH/883S

R1 - R8 = 10KΩ ± 5%, 1/4W
V1 = +15V ± 10%
V2 = -15V ± 10%
V3 = +12V ± 10%

Radiation Qualification Procedure

1. SAMPLE SELECTION:
   Die Samples shall be selected for total dose testing per Mil-Std-883, Method 5005, Group E, Subgroup 2 for steady-state, total dose irradiation.
2. IRRADIATION QUALIFICATION PROCEDURE:
   All irradiation qualification testing is performed per Mil-Std-883, Method 1019.
3. RADIATION BIAS CIRCUITS:
   Shown here are the radiation bias circuits used for this device qualification.



HS-384RH/390RH/883S

R1 - R8 = 10KΩ ± 5%, 1/4W
V1 = +15V ± 10%
V2 = -15V ± 10%
V3 = +5V ± 5%

Die Characteristics

DIE DIMENSIONS:
Die Size: 2130 x 1930µm
Die Thickness: 11 ± 1 mils
Pad Dimensions: 0.004" x 0.004"

METALLIZATION:
Front: Al, 12.5kÅ ± 2kÅ
Back: Gold

GLASSIVATION:
Type: Silox
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold
Temperature: Sidebrazed Ceramic DIP — 450°C ± 10°C (Max)
Cerpack — 450°C ± 10°C (Max)

WORST CASE CURRENT DENSITY: 1.732e05 A/cm^2

PROCESS: DI Linear Metal Gate CMOS

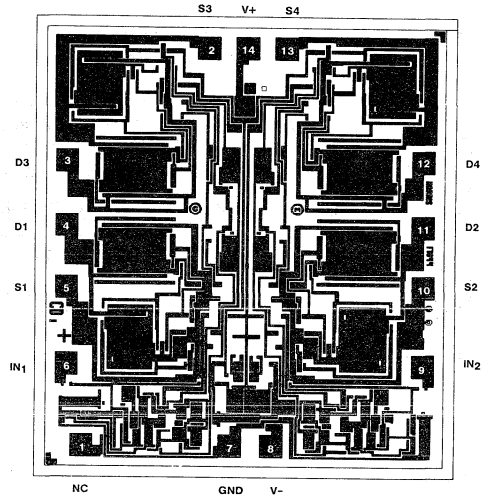
LEAD TEMPERATURE (10 Seconds Soldering): < 275°C

SUBSTRATE POTENTIAL: Unbiased

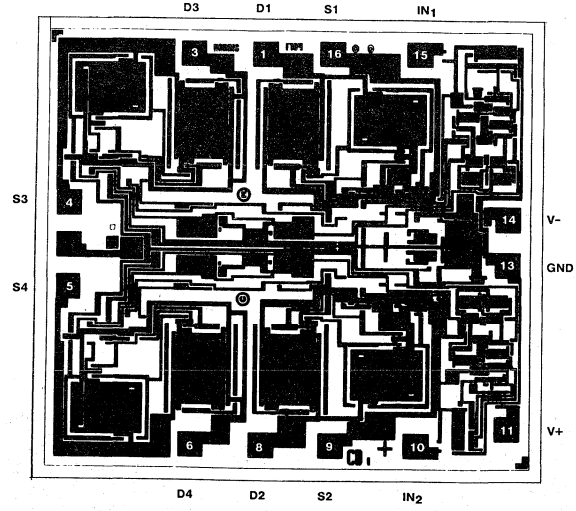
ESD RATING: <2000V

Metallization Mask Layout

HS-302RH/303RH/306RH/307RH/883S

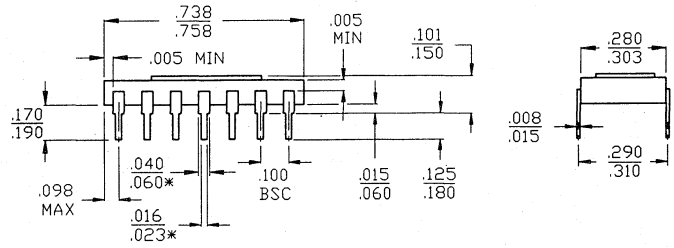


HS-384RH/390RH/883S



Packaging†

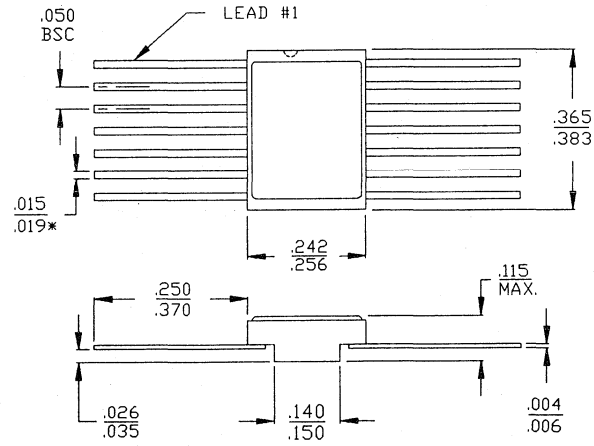
14 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

14 PIN CERAMIC FLATPACK



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

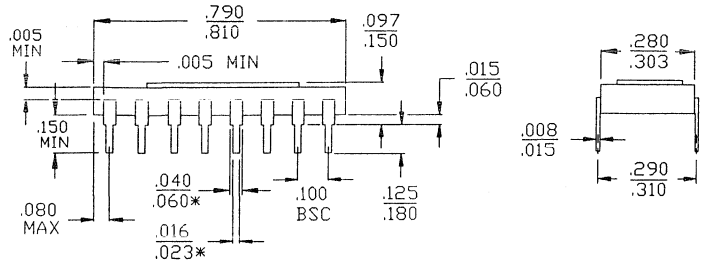
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 F-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

Packaging†

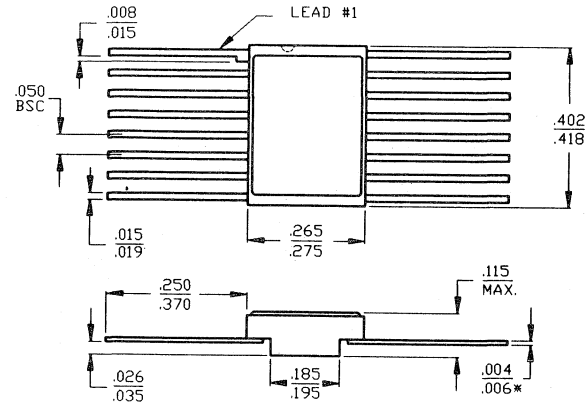
16 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

16 PIN CERAMIC FLATPACK



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 F-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

RAD-HARD 7

LINE Tx/Rx

HS-245RH
RADIATION HARDENED TRIPLE LINE TRANSMITTER

HS-246RH, HS-249RH
RADIATION HARDENED TRIPLE LINE RECEIVERS

HS-248RH
RADIATION HARDENED TRIPLE PARTY-LINE RECEIVER

July 1990

Features

- Radiation Hardened DI Processing
  - Total Dose (γ) 2 x 10^5 Rads (Si)
  - Transient Upset ($\dot{\gamma}$) Upset 1 x 10^9 Rads (Si)/s
  - Latchup Free
  - Neutron Fluence 5 x 10^{12} N/cm^2
- Replaces HD-245/246/248/249
- Current Mode Operation
- High Speed..... 15MHz with 50 Foot Cable
  2MHz with 1000 Foot Cable
- High Noise Immunity
- Low EMI Generation
- Low Power Dissipation
- High Common Mode Rejection
- Transmitter and Receiver Party Line Capability
- Tolerates -2.0V to +20.0V Ground Differential (Transmitter with Respect to Receiver)
- Transmitter Input/Receiver Output TTL/DTL Compatible

Description

The HS-245RH/246RH/248RH/249RH radiation hardened triple line transmitter and triple line receivers are fabricated using the Harris dielectric isolation process. These parts are identical in pinout and function to the original HD-245/246/248/249. They are also die size and bond pad placement compatible with the original parts for those customers who buy dice for hybrid assembly.

Each transmitter-receiver combination provides a digital interface between systems linked by 100Ω twisted pair, shielded cable. Each device contains three circuits fabricated within a single monolithic chip. Data rates greater than 15MHz are possible depending on transmission line loss characteristics and length.

The transmitter employs constant current switching which provides high noise immunity along with high speeds, low power dissipation, low EMI generation and the ability to drive high capacitance loads. In addition, the transmitters can be turned "off" allowing several transmitters to time-share a single line.

Receiver input/output differences are shown in the table:

	INPUT	OUTPUT
HS-246RH	100Ω	Open Collector
HS-248RH	Hi-Z	6K Pull-Up Resistors
HS-249RH	100Ω	6K Pull-Up Resistors

The internal 100Ω cable termination consists of 50Ω from each input to ground.

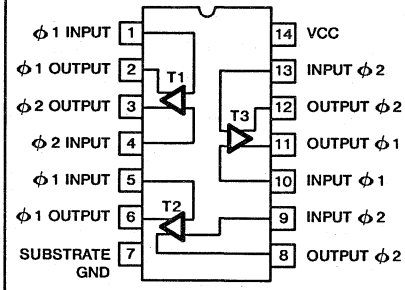
HS-248RH "party line" receivers have a Hi-Z input such that as many as ten of these receivers can be used on a single transmission line.

Each transmitter input and receiver output can be connected to TTL and DTL systems. When used with shielded transmission line, the transmitter-receiver system has very high immunity to capacitance and magnetic noise coupling from adjacent conductors. The system can tolerate ground differentials of -2.0V to +20.0V (transmitter with respect to receiver).

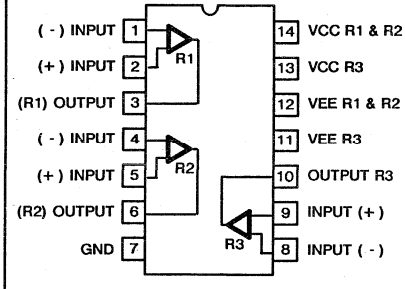
These parts are available in Class B or Class S processing. Contact your nearest Harris Sales Office for details.

Pinouts

HS9-245RH (FLATPACK)
HS1-245RH (CERAMIC DIP)
TOP VIEW



HS9-246RH/248RH/249RH
(FLATPACK)
HS1-246RH/248RH/249RH
(CERAMIC DIP)
TOP VIEW



7 LINE Tx/Rx

Absolute Maximum Ratings

Input Voltage ..... -0.5V to +10V
Output Voltage ..... -30V to +0.5V with Respect to VCC
Supply Voltage ..... -0.5V to +10V
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +275°C
Junction Temperature ..... +175°C
ESD Classification ..... Class 1

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Flatpack	75°C/W	13.0°C/W
Sidebraze DIP	67°C/W	16.0°C/W

Maximum Package Power Dissipation at +125°C
Flatpack 0.5W
Sidebraze DIP 0.5W
Transistor Count 6

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Voltage Range ..... 4.5V to 5.5V

TABLE 1. HS-245RH D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Low Current	IIL	VCC = 5.5V, Note 1	1, 2, 3	-55°C < TA < +125°C	-2.8	-	mA
On Output Current	IOUT "On"	VCC = 4.5V, 5.5V, Notes 1, 2	1, 2, 3	-55°C < TA < +125°C	-5.6	-1.0	mA
On Output Current Unbalance	ΔIOUT	VCC = 5.5V, Note 3	1, 2, 3	-55°C < TA < +125°C	-	380	µA
Off Output Current	IOUT "Off"	VCC = 4.5V, Note 1	1, 2, 3	-55°C < TA < +125°C	-100	-	µA
Output Breakdown	BVCER	VCC = 0.0V, Note 4	1	+25°C	-30	-	V
Power Supply Current	ICC	VCC = 5.5V, Notes 5, 6	1	+25°C	-	21	mA

NOTES:
1. One input at GND, one input open, each output at GND.
2. One input at 0.45V, one input open, each output at GND.
3. Difference between $\phi 1$ and $\phi 2$ "ON" output data current.
4. Each input at GND, one output at GND, ILIMIT > -100µA on output tested with -30V applied.
5. One input of each transmitter at GND and the other input open. All six output lines at GND.
6. All six input lines open, **all six** output lines at GND.

TABLE 2. HS-245RH A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH, TPHL	VCC = 4.5V, 5.5V	9, 10, 11	-55°C < TA < +125°C	-	14	ns

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings

Input Voltage ..... -1.0V to +1.0V
Output Voltage ..... -0.5V to +6.0V
Supply Voltage (VCC) ..... -0.5V to +8.0V
Supply Voltage (VEE) ..... -8.0 to +0.5V
Input Current ..... -25mA to +25mA
Output Current 50mA
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +275°C
Junction Temperature ..... +175°C
ESD Classification ..... Class 1

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Flatpack	75°C/W	13.0°C/W
Sidebraze DIP	67°C/W	16.0°C/W

Maximum Package Power Dissipation at +125°C
Flatpack 0.5W
Sidebraze DIP 0.5W
Transistor Count 9

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Voltage Range ..... 4.5V to 5.5V

TABLE 1. HS-246RH, HS-248RH, HS-249RH D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Resistance	RIN	VCC = 5.0V, VEE = -5.0V (HS-246RH & HS-249RH)	1, 2, 3	-55°C < TA < +125°C	39	90	Ω
Pullup Resistance	RPU	VCC = 5.0V, VEE = -5.0V (HS-248RH & HS-249RH)	1, 2, 3	-55°C < TA < +125°C	4.1	10.5	kΩ
Logical "1" Output Voltage	VOH	VCC = 4.5V, VEE = -4.5V IOH = -120µA, Note 1 (HS-248RH & HS-249RH)	1, 2, 3	-55°C < TA < +125°C	2.5	-	V
Logical "0" Output Voltage	VOL	VCC = 4.5V, VEE = -4.5V IOL = 9.6mA (HS-248RH & HS-249RH) Note 2	1, 2, 3	-55°C < TA < +125°C	-	0.45	V
		VCC = 4.5V, VEE = -4.5V IOL = 10.0mA (HS-246RH) Note 2	1, 2, 3	-55°C < TA < +125°C	-	0.45	V
Logical "0" Output Voltage, Input Short Circuit	VOLSC	VCC = 4.5V, VEE = -4.5V IOL = 3.2mA, Note 3	1	+25°C	-	0.45	V
Power Supply Current	ICC	VCC = 5.5V, VEE = -5.5V (HS-246RH) Notes 4, 5	1	+25°C	-	6.6	mA
		VCC = 5.5V, VEE = -5.5V (HS-248RH & HS-249RH) Notes 4, 5	1	+25°C		7.8	mA
Power Supply Current	IEE	VCC = 5.5V, VEE = -5.5V Note 4, 5	1	+25°C	-	6.0	mA

NOTES:
1. (+) I_{IN} = 1.5mA; (-) Input = Open (For HS-248RH Ext. 50Ω Res. or 0.75mV)
2. (+) Input = Open; (-) I_{IN} = 1.5mA. (For HS-248 Ext. 50Ω Res. or 0.75mV)
3. Both inputs shorted to GND; or both inputs open such that 50Ω termination resistors are in the circuit.
4. (+) Input = Open; (-) I_{IN} = 3mA
5. (+) I_{IN} = 3mA; (-) Input = Open

TABLE 2. HS-246RH, HS-248RH, HS-249RH A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH, TPHL	VCC = 4.5V, VEE = -4.5V	9, 10, 11	-55°C < TA < +125°C	-	30	ns

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

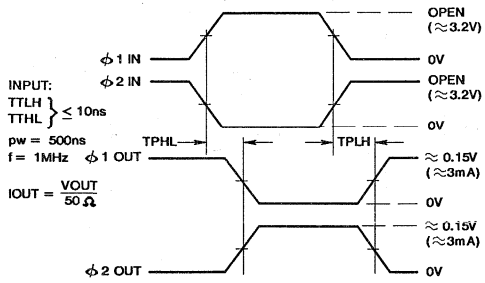
TABLE 4. APPLICABLE SUBGROUPS

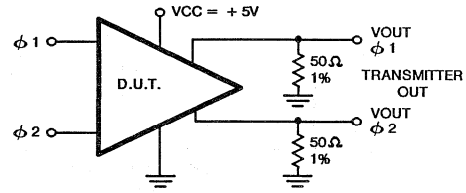
MIL-STD-883 TEST REQUIREMENTS	GROUP A SUBGROUPS PER METHOD 5005 (SEE TABLES 1 & 2)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Test Parameters (Method 5004)	1, 2, 3, 9, 10,11 (Note 1) 7, 8A, 8B (Functional Tests)
Group A Test Requirements (Method 5005)	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B5 End-Point Electrical Parameters (Method 5005) (Class S Only)	1, 2, 3
Group B6 End-Point Electrical Parameters (Method 5005) (Class S Only)	1
Group D End-Point Electrical Parameters (Method 5005)	1
Group E2 End-Point Electrical Parameters (Method 5005)	1, 7 (Note 3)

NOTES 1. PDA applies to subgroup 1 and delta limits.
2. Endpoints are datalogged pre- and post-irradiation testing.
3. Endpoints are datalogged pre- and post-irradiation testing.

Test Circuits and Applications

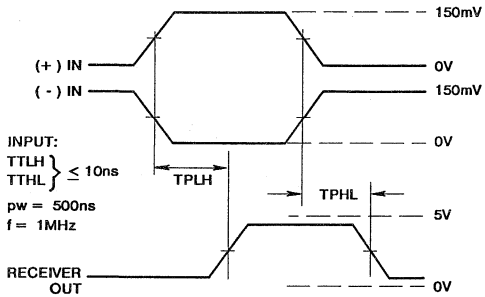
CIRCUIT #1 TRANSMITTER PROPAGATION DELAY



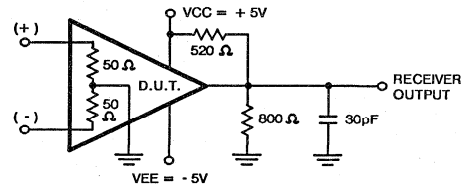


All timing measurements referenced to 50% V points.

CIRCUIT #2 RECEIVER PROPAGATION DELAY

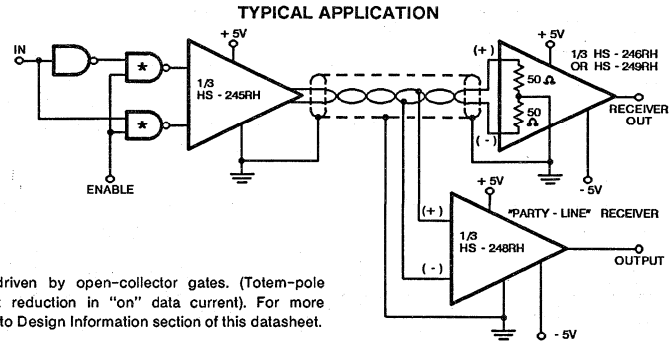


All timing measurements referenced to 50% V points.



NOTE: External 50Ω resistors needed for HS-248RH

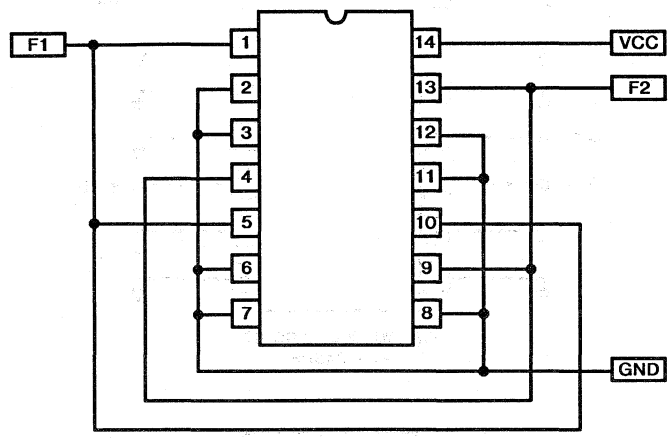
TYPICAL APPLICATION



* HS-245RH should be driven by open-collector gates. (Totem-pole output may cause slight reduction in "on" data current). For more detailed information, refer to Design Information section of this datasheet.

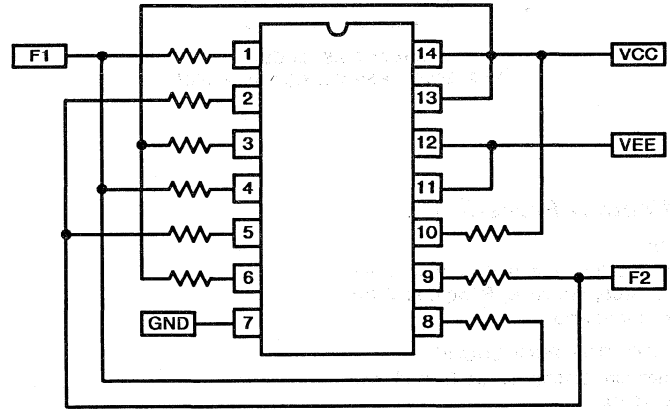
Burn-In Circuits

HS9-245RH (FLATPACK)
HS1-245RH (CERAMIC DIP)



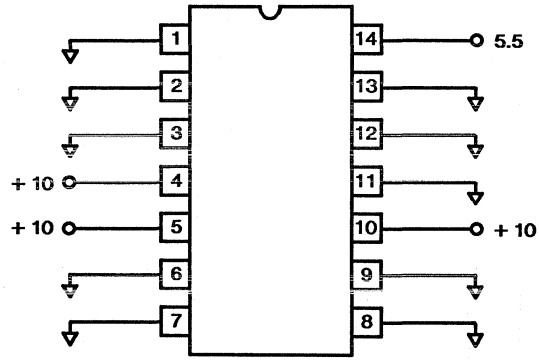
NOTES:
VCC = 5.0V + 10%
TA (Min) = +125°C

HS9-246RH, HS9-248RH, HS9-249RH (FLATPACK)
HS1-246RH, HS1-248RH, HS1-249RH (CERAMIC DIP)

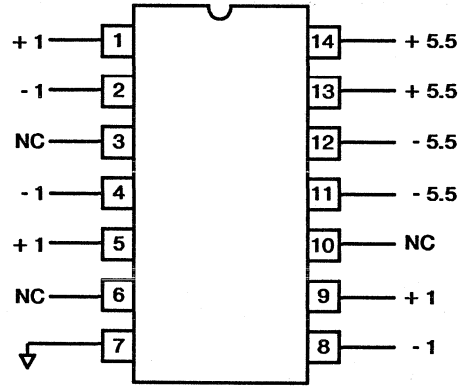


NOTES:
VCC = +5.0V ± 10%
VEE = -5.0V ± 10%
TA (Min) +125°C
All resistors 1.0kΩ ± 10%, 1/4W (Min)

Irradiation Circuits



GAMMA BIAS CIRCUIT
HS1-245RH



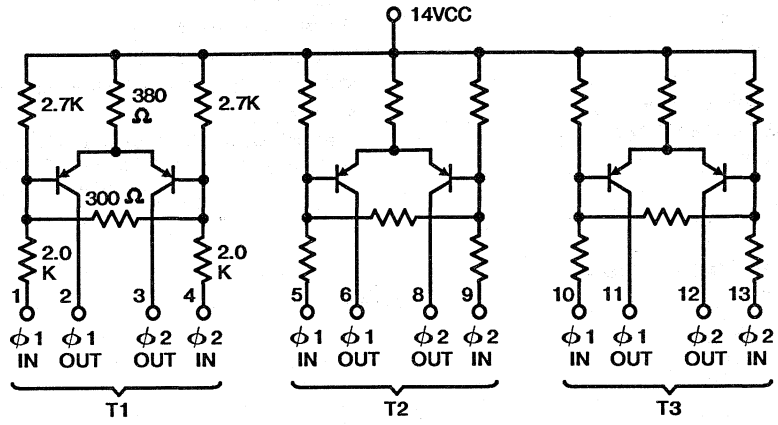
GAMMA BIAS CIRCUIT
HS9-246RH, HS9-248RH, HS9-249RH

Radiation Qualification Procedure

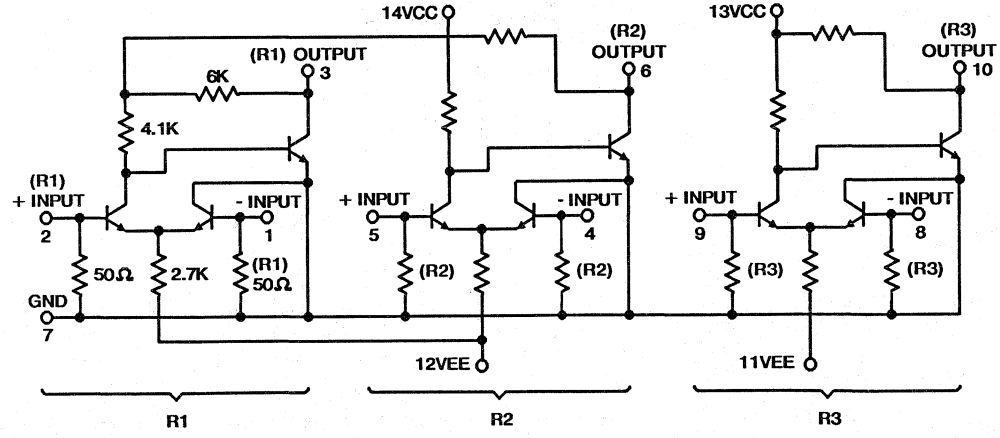
1. SAMPLE SELECTION:
   Die Samples shall be selected for total dose testing per Mil-Std-883, Method 5005, Group E, Subgroup 2 for steady-state, total dose irradiation.
2. IRRADIATION QUALIFICATION PROCEDURE:
   All irradiation qualification testing is performed per Mil-Std-883, Method 1019.
3. RADIATION BIAS CIRCUIT:
   Listed above are the radiation bias circuits used for these devices.

Schematics

HS-245RH



HS-246RH HS-248RH HS-249RH



NOTES:

1. HS-249RH is as shown
2. HS-246RH does not have 6K output pull-up resistors
3. HS-248RH does not have 50Ω input termination resistors

Die Characteristics

DIE DIMENSIONS:
45 x 45 x 11 mils
(1140 x 1140 x 280 µm)

METALLIZATION:
Type: Aluminum
Thickness: 12.5kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
7.8×10^4 A/cm^2

GLASSIVATION:
Type: Silox
Thickness: 8.0kÅ ± 1kÅ

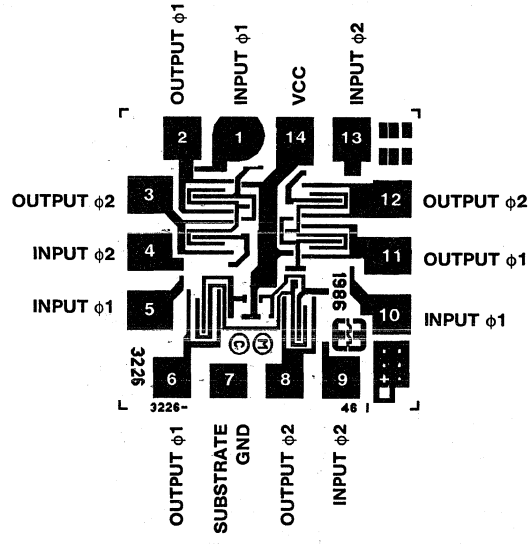
TRANSISTOR COUNT: 6

PROCESS: HFSB Bipolar/Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Flatpack — 460°C (Max)

Metallization Mask Layout

HS-245RH



Die Characteristics

DIE DIMENSIONS:
1140 x 1190 x 280 µm)
(45 x 47 x 11 mils)

METALLIZATION:
Type: T.W.
Thickness: 2.5kÅ ± 0.5kÅ
Type: Al
Thickness: 14kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
1.4×10^5 A/cm^2

GLASSIVATION:
Type: Silox
Thickness: 8.0kÅ ± 1.0kÅ

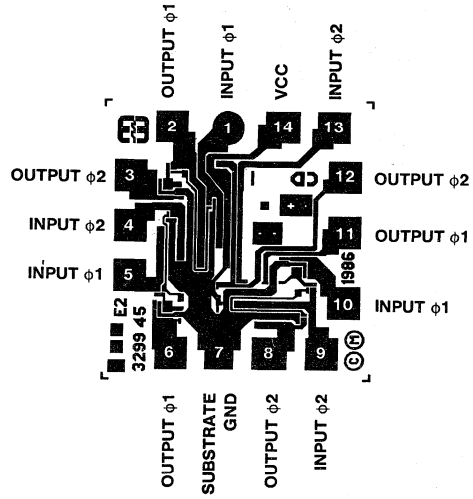
TRANSISTOR COUNT: 9

PROCESS: ALPS Bipolar/Dielectric Isolation

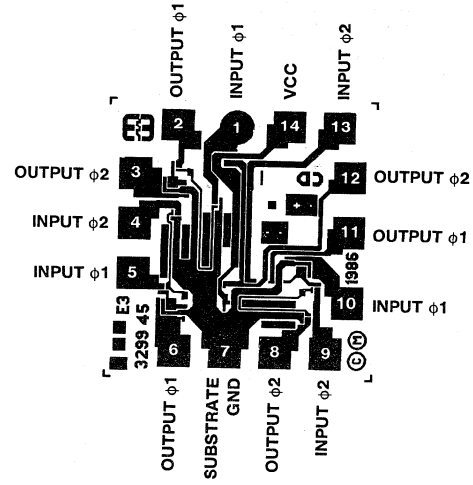
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Flatpack — 460°C (Max)

Metallization Mask Layout

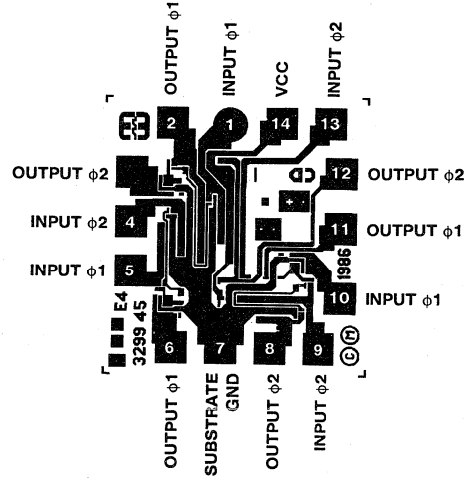
HS-246RH



HS-248RH

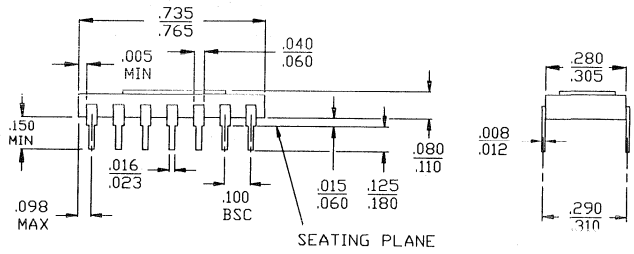


HS-249RH



Packaging†

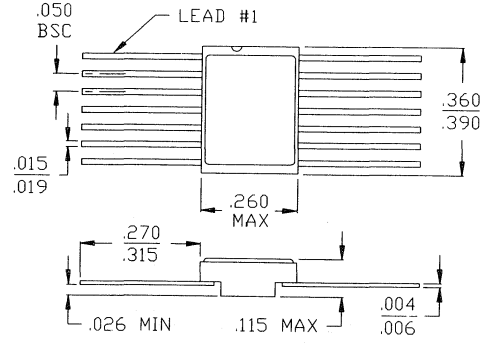
14 PIN CERAMIC SIDEBRAZE DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

14 PIN FLATPACK



LEAD MATERIAL: Type A or B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 F-2A

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Voltage Mode Transmission

Data rates of up to 10 million bits per second can be obtained with standard TTL logic; however, the transmission distance must be very short. For example, a typical 50 foot low capacitance cable will have a capacitance of approximately 750pF which requires a current of greater than 50mA to drive 5V into this cable at 10MHz; therefore, voltage mode transmitters are undesirable for long transmission lines at high data rates due to the large current required to charge the transmission line capacitance.

Current Mode Transmission

An alternate method of driving high data rates down long transmission lines is to use a current mode transmitter. Current mode logic changes the current in a low impedance transmission line and requires very little change in voltage. For example, a 2mA change in transmitter current will produce a 100mV change in receiver voltage independent of the series transmission line resistance. The rise time at the receiver for a typical 50 foot cable (750pF) is approximately 30ns for a 2mA pulse.

An emitter coupled logic gate is frequently used for a current mode transmitter. However, ECL gates are not compatible with TTL and DTL logic and they require considerable power. The Harris Semiconductor HS-245RH is a TTL/DTL compatible current mode transmitter designed for high data rates on long transmission lines. Data rates of 15 megabits per second can be obtained with 50 feet of transmission line when using the companion HS-246RH or HS-249RH receiver. Data rates of 2 megabits per second are easily obtained on transmission lines as long as 1,000 feet. The Harris transmitter and receivers feature very low power, typically 25mW for the transmitter and 15mW for the receiver.

Harris Transmitter/Receivers

The Harris transmitter/receiver family consists of a triple line transmitter, two triple line receivers with internal terminations and a triple party-line receiver. The general characteristics of the transmitter and receivers are outlined in Table A.

TABLE A. GENERAL TRANSMITTER/RECEIVER CHARACTERISTICS

TRIPLE LINE TRANSMITTER			
PARAMETER	**HS-245RH**	**UNITS**	**COMMENTS**
Operating Temperature Range	-55°C to +125°C	°C	
"ON" Output Current	1.0 Min	mA	Over Full Temperature Range
Power Supply Current	7.0 Max	mA	Per Transmitter Section
Standby Current	33 Max	µA	Per Transmitter Section
Propagation Delay	14 Max	ns	Over Full Temperature Range

TRIPLE LINE RECEIVER				
PARAMETER	**RECEIVER TYPE**	**LIMITS**	**UNITS**	**COMMENTS**
Operating Temperature Range	HS-246RH/248RH/249RH	-55°C to +125°C	°C	
Power Supply ICC (VCC = +5.0V)	HS-246RH/248RH/249RH	2.6	mA	Per Receiver Section
Propagation Delay	All Receivers	30	ns	Over Full Temp. Range
Input Impedance and Output Circuit		**INPUT**		**OUTPUT**
	HS-246RH	100	Ω	Open Collector
	HS-248RH	Hi-Z		6K Pull-Up Resistor
	HS-249RH	100	Ω	6K Pull-Up Resistor

DESIGN INFORMATION (Continued)

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Transmitter

The HS-245RH transmitters have two inputs per transmitter, either of which is low while the other is open during normal operation and both inputs are open during standby. For optimum transmitter performance, the "off" input should be open circuit rather than being pulled towards +5V, because this will reduce the "on" output data current. On the other hand, the "on" and "off" output data current will be increase if the "off" input is held below its open circuit voltage. Open collector gates such as the 7401 and 7403 or 7405 Hex-Inverter are suitable for driving the HS-245RH transmitter inputs. By using 2-input gates as shown in Figure 1, an enable line can be provided so that more than one transmitter may be connected to a line for time sharing. When the enable line is low the transmitter will be disabled and will present a high impedance to the transmission line as well as requiring very little power supply current.

Complementary input signals may be derived from high speed inverter gates as shown, or by using the complementary outputs of a flip-flop. When the transmitter is connected near the midpoint of a long transmission line or to a line with terminations at both ends, two transmitter sections should be paralleled with respective inputs and outputs connected together in order to drive the reduced impedance. This parallel transmitter technique can also be used to increase the data rate on long transmission lines.

Transmitter Operation

The transmitter alternately applies the current to each of the two conductors in the twisted pair line such that the total current in the twisted pair is constant and always in the same direction. This current flows through either of the two 50Ω terminating resistors at the receiver and returns to the transmitter as a steady DC current on the transmission line shield. The DC power supply return for the transmitter is through the receiver terminating resistors (the transmitter ground pin is only a substrate ground). Therefore, it is essential that the shield be connected to the power supply common at both the transmitter and receiver, preferably at the integrated circuit "ground" pin. More than fifteen twisted pair lines can share the same shield without crosstalk.

Receivers

The HS-248RH "party-line" receiver presents a high impedance load to the transmission line allowing as many as ten HS-248RH receivers to be distributed along a line without excessive loading. Figure 1 shows a typical system of a transmitter, a terminating receiver and a party-line receiver. The transmission line is terminated in its characteristics impedance by an HS-246RH, HS-249RH, or by a pair of 50Ω resistors connecting each line to the ground return shield.

Transmission Lines

The maximum frequency (or minumum pulse width) which can be carried by a certain length of a given transmission line is dependent on the loss characteristics of the particular line. At low frequencies, there will be virtually no loss in pulse amplitude, but there will be a degradation of rise and fall-time which is roughly proportional to the square of the line length. This is shown in Figure 2. If the pulse width is

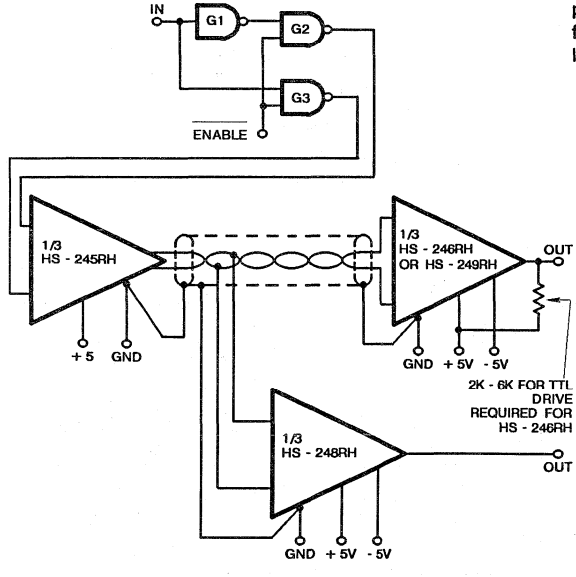
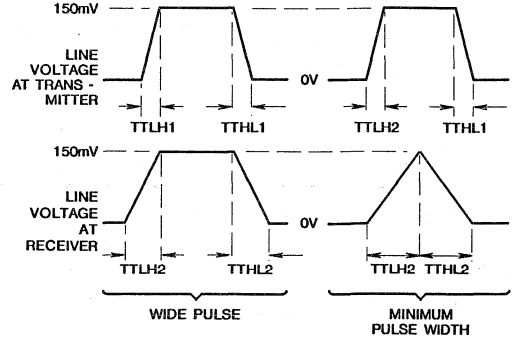


FIGURE 1. TYPICAL DATA TRANSMISSION SYSTEM



$T_{RLH_2} = T_{TLH_1} KL^2$

$T_{THL_2} = T_{THL_1} KL^2$

Where: L is Line Length
K is Determined by line loss characteristics.

FIGURE 2. TRANSMISSION LINE WAVE-SHAPING

DESIGN INFORMATION (Continued)

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less than the rise-time at the receiver end, the pulse amplitude will be diminished, approaching the point where it cannot be detected by the receiver.

The transmission line used with the Harris HS-245RH series transmitter and receivers can be any ordinary shielded, twisted pair line with a characteristic impedance of 100Ω. Twisted pair lines consisting of number 20 or 22 gauge wire will generally have this characteristic impedance. Special high quality transmission lines are not necessary and standard audio, shielded-twisted pair, cable is generally suitable.

Since the necessary characteristics for various twisted pair lines are not readily available, it may be necessary to take some measurements on a length of the proposed line. To do this, connect an HS-245RH transmitter to one end of the line (100 feet or more) and an HS-246RH or an HS-249RH receiver to the other end. The rise and fall-times can be measured on the line at both ends and the constant "K", for that line can be computed as shown in Figure 2 so that the minimum pulse width can be determined for any length of line.

Data rates of 2MHz have been obtained using 1,000 feet of standard shielded, twisted pair, audio cable. Data rates of 15MHz are possible on shorter lengths of transmission line (50 feet).

Electromagnetic Interference

Very little electromagnetic interference is generated by the Harris current mode system because the total current through the twisted pair is constant, while the current through the shield is also constant and in the opposite direction. This can be verified by observing, with a current probe, the total current through the twisted pair, through the shield and through the complete shielded, twisted pair cable. In each case a constant current will be observed with only small variations. Small pulses may be observed if the complementary inputs to the transmitter do not switch at the same time. The current will decrease during the time both inputs are high, and will increase during the time both inputs are low. These switching pulses may be observed when using the circuit shown in Figure 1. The amplitude and shape of these pulses will depend of the propagation delay of G1, and transition times G2 and G3. These pulses are generally of no concern because of their small amplitude and width, but they may be reduced by increasing the similarity of the waveforms and timing synchronization of the complementary signals applied to the transmitter.

In addition to generating very little noise, the system is also highly immune to outside noise since it is difficult to capacitively couple a differential signal into the low impedance twisted pair cable and it is even more difficult in induce a differential current into the line due to the very high impedance of the constant current transmitter. Therefore, differential mode interference is generally not a problem with the Harris current mode system. Large common mode voltages can also be tolerated because the output current of the transmitter is constant as long as the receiver termination ground is less than 2V positive with respect to the grounded input of the transmitter, and is less than 25V negative with respect to the transmitter VCC. The current mode system is totally unaffected by ground differential noise of +2V at frequencies as high as 1MHz.

Propagation Delay

The worst case propagation delay of a transmitter and receiver, connected as shown in Figure 1, can be determined by adding the maximum delay shown on the data sheet for the transmitter and receiver. These overall switching characteristics are shown in Table B. For the entire system, however, the propagation delay of the transmission line must also be considered. This delay, of course, depends on the length of the line and the characteristics of the line, but in general, delays of between 1.5ns and 3.0ns per foot can be expected.

TABLE B. OVERALL TRANSMITTER/RECEIVER SWITCHING CHARACTERISTICS

CHARACTERISTICS	-55°C to +125°C HS-245RH HS-246RH HS-248RH HS-249RH			UNITS
	MIN	TYP	MAX	
Progagation Delay TPLH	-	18	40	ns
Propagation Delay TPHL	-	18	40	ns
Duty Cycle Distortion TPLH - TPHL	-	2	15	ns

VCC = +5V, VEE = -5V

RAD-HARD 8

MICROPROCESSORS

HARRIS

HS-80C85RH

Radiation Hardened 8-Bit CMOS Microprocessor

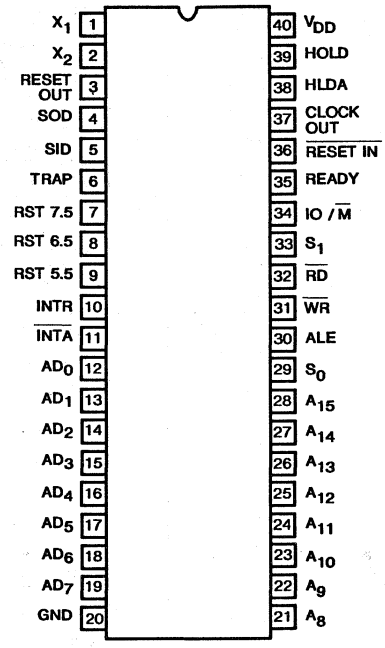
July 1990

Features

- Radiation Hardened EPI-CMOS
- Parametrics Guaranteed ..... 1×10^5 RAD(Si)
- Transient Upset..... $> 1 \times 10^8$ RAD(Si)/s
- Latch-up Free ..... $> 1 \times 10^{12}$ RAD(Si)/s
- Low Standby Current.....500μA Max
- Low Operating Current .....5.0mA/MHz (X_1 Input)
- Electrically Equivalent to Sandia SA 3000
- 100% Software Compatible with INTEL 8085
- Operation from DC to 2MHz, Post Radiation
- Single 5 Volt Power Supply
- On-Chip Clock Generator and System Controller
- Four Vectored Interrupt Inputs
- Completely Static Design
- Self Aligned Junction Isolated (SAJI) Process
- Military Temperature Range..... -55°C to +125°C

Pinout

TOP VIEW

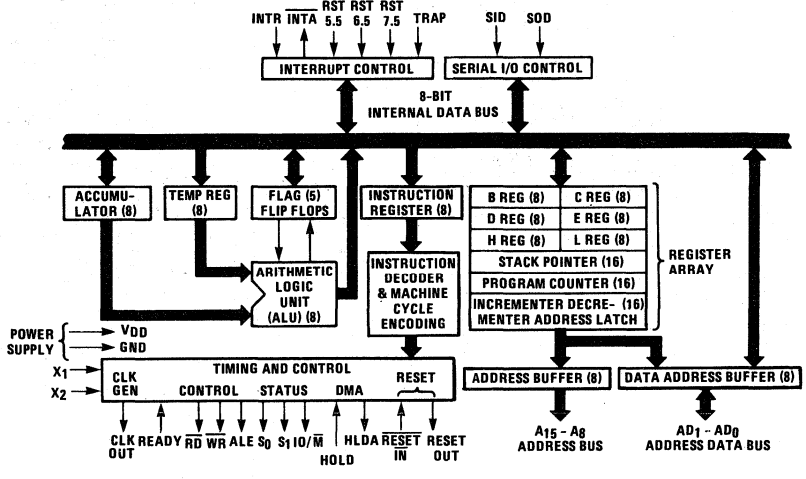


Description

The HS-80C85RH is an 8-bit CMOS microprocessor fabricated using the Harris radiation hardened self-aligned junction isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

The HS-80C85RH is a functional logic emulation of the HMOS 8085 and its instruction set is 100% software compatible with the HMOS device. The HS-80C85RH is designed for operation with a single 5 volt power supply. Its high level of integration allows the construction of a radiation hardened microcomputer system with as few as three ICs (HS-80C85RH CPU, HS-83C55RH ROM I/O, and the HS-81C55/56RH RAM I/O.

Functional Diagram



8 MICROPROCESSORS

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Table 1. Pin Description

Symbol	Type	Name and Function
A_8 - A_{15}	O	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7}	I/O	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE	O	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, and IO/$\overline{M}$	O	Machine Cycle Status: IO/$\overline{M}$ S_1 S_0 Status 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch i i i Opcode fetch 1 1 1 Interrupt Acknowledge • 0 0 Halt • X X Hold • X X Reset • = 3-state (high impedance) X = unspecified S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$	O	Read Control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$	O	Write Control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$, 3-stated during Hold and Halt modes and during RESET.

Symbol	Type	Name and Function
READY	I	Ready: If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD	I	Hold: Indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA	O	Hold Acknowledge: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR	I	Interrupt Request: Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{INTA}$	O	Interrupt Acknowledge: Is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate an 8259A Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5	I	Restart Interrupts: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.

Table 1. Pin Description (Continued)

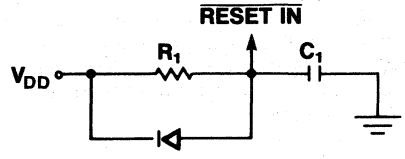
Symbol	Type	Name and Function
TRAP	I	Trap: Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 2.)
$\overline{\text{RESET IN}}$	I	Reset In: Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 1). Upon power-up, $\overline{\text{RESET IN}}$ must remain low for at least 10 "clock cycle" after minimum V_{DD} has been reached. For proper reset operation after the power-up duration, $\overline{\text{RESET IN}}$ should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.

Symbol	Type	Name and Function
RESET OUT	O	Reset Out: Reset Out indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1 X_2	I O	X_1 and X_2: Are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK	O	Clock: Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID	I	Serial Input Data Line: The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD	O	Serial Output Data Line: The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	I	Power: +5V supply.
GND	I	Ground: Reference.

Table 2. Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched.)
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:
1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.



TYPICAL POWER-ON RESET RC VALUES*
R_1 = 75 KΩ
C_1 = 1 μF
*VALUES MAY HAVE TO VARY DUE TO APPLIED POWER SUPPLY RAMP UP TIME.

Figure 1. Power-On Reset Circuit

Functional Description

The HS-80C85RH is a complete 8-bit parallel central processing unit implemented in a self aligned, silicon gate, CMOS technology. Its static design allows the device to be operated at any external clock frequency from a maximum of 4 MHz down to DC. The processor clock can be stopped in either the high or low state and held there indefinitely. This type of operation is especially useful for system debug or power critical applications. The device is designed to fit into a minimum system of three ICs: CPU (HS-80C85RH), RAM/IO (HS-81C55/56RH) and ROM/IO Chip (HS-83C55RH).

Since the HS-80C85RH is implemented in CMOS, all of the advantages of CMOS technology are inherent in the device. These advantages include low standby and operating power, high noise immunity, moderately high speed, wide operating temperature range, and designed-in radiation hardness. Thus the HS-80C85RH is ideal for weapons and space applications.

The HS-80C85RH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The HS-80C85RH register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The HS-80C85RH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The HS-80C85RH provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and $IO/\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The HS-80C85RH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the HS-80C85RH has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt, and a bus vectored interrupt, INTR.

INTERRUPT AND SERIAL I/O

The HS-80C85RH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is maskable (can be enabled or disabled by EI or DI software instructions), and causes the CPU to fetch in an RST instruction, externally placed on the data bus, which vectors a branch to any one of eight fixed memory locations (Restart addresses). The decimal addresses of these dedicated locations are: 0, 8, 16, 24, 32, 40, 48, and 56. Any of these addresses may be used to store the first instruction(s) of a routine designed to service the requirements of an interrupting device. Since the (RST) is a call, completion of the instruction also stores the old program counter contents on the STACK. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 2.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive.*

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request (a normally high level signal with a low going pulse is recommended for highest system noise immunity). The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the 80C85RH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP – highest priority, RST 7.5, RST 6.5, RST 5.5, INTR – lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive.* The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 2 illustrates the TRAP interrupt request circuitry within the HS-80C85RH. Note that the

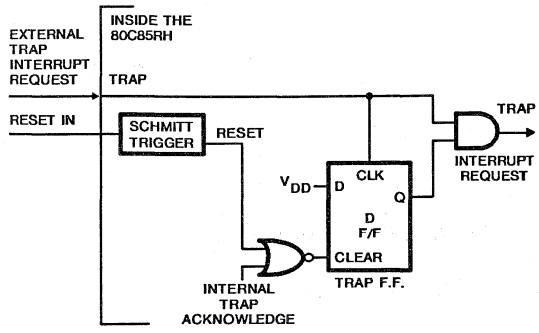


Figure 2. TRAP and RESET IN Circuit

servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that is disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5-7.5 will provide current interrupt enable status, revealing that interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

DRIVING THE X_1 AND X_2 INPUTS

You may drive the clock inputs of the HS-80C85RH with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving frequency may be any value from DC to 4MHz and must be twice the desired internal clock frequency.

The following guidelines should be observed when a crystal is used to drive the HS-80C85RH clock input:

1) A 20pF capacitor should be connected from X_2 to ground to assure oscillator start-up at the correct frequency.
2) A 10MΩ resistor is required between X_1 and X_2 for bias point stabilization.

In addition, the crystal should have the following characteristics:

1) Parallel resonance at twice the desired internal clock frequency
2) C_L (load capacitance) $\leq$ 30pF
3) C_S (shunt capacitance) $\leq$ 7pF
4) R_S (equivalent shunt resistance) $\leq$ 75Ω
5) Drive level: 10mW
6) Frequency tolerance: ±0.005% (suggested)

A parallel-resonant LC circuit may be used as the frequency-determining network for the HS-80C85RH, providing that its frequency tolerance of approximately ±10% is acceptable. The components are chosen from the formula:

$$f = \frac{1}{2\pi\sqrt{L(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int}, or 30pF. The use of an LC circuit is not recommended for frequencies higher than approximately 4MHz.

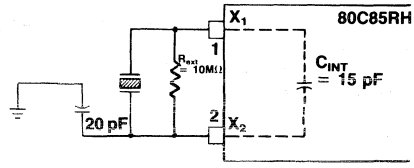
An RC cicruit may be used as the frequency-determining network for the HS-80C85RH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

Figure 3 shows the recommended clock driver circuits.

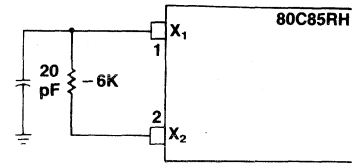
For driving frequencies up to and including 4MHz you may supply the driving signal to X1 and leave X2 open-circuited (Figure 3D).

HS-80C85RH CAVEATS

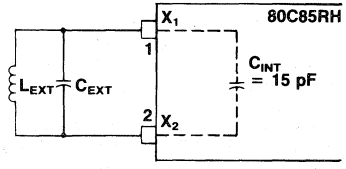
1. An important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule also applies to inputs connected to a tri-state bus. The need for external pull-up resistors during tri-state bus conditions is eliminated by the presence of regenerative latches on the following HS-80C85RH output pins: AD0-AD7, A8-A15, and IO/M. Figure 4 depicts an output and corresponding regenerative latch. When the output driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the tri-state condition. A transient drive current of approximately ± 1.0mA at 0.5 V_{DD} for 10nsec is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during tri-state conditions.



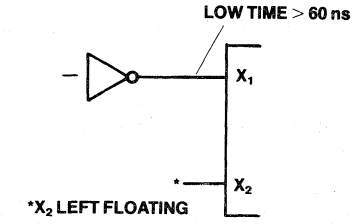
a. Quartz Crystal Clock Driver



c. RC Circuit Clock Driver



b. LC Tuned Circuit Clock Driver



d. 0-6 MHz Input Frequency External Clock Driver Circuit

Figure 3. Clock Driver Circuits

2. The $\overline{RD}$ and $\overline{WR}$ pins of the HS-80C85RH contain internal dynamic pull-up transistors to avoid spurious selection of memory devices when the $\overline{RD}$ and $\overline{WR}$ pins assume the high impedance state. This eliminates the need for external resistive pull-ups on these pins.

3. The $\overline{RESET\ IN}$ and X_1 inputs on the HS-80C85RH are schmit trigger inputs. This eliminates the possibility of internal oscillations in response to slow rise time input signals at these pins.

4. A high frequency bypass capacitor of approximately 0.1 µf should be connected between V_{DD} and GND to shunt power supply transients.

5. The HS-80C85RH is functional within 10 input clock cycles after application of power (assuming that reset has been asserted from power-on). Start up conditions in the crystal-controlled oscillator mode must also account for the characteristics of the oscillator.

GENERATING AN HS-80C85RH WAIT STATE

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 5 may be used to insert one WAIT state in each HS-80C85RH machine cycle.

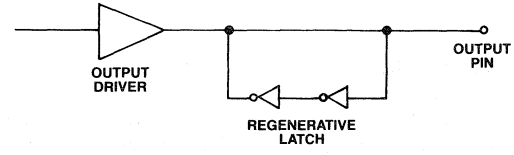
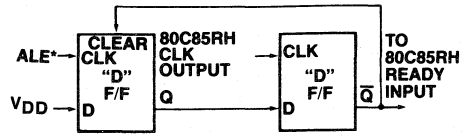


Figure 4. Output Driver and Latch for Pins AD0-AD7, A8-A15, and IO/$\overline{M}$.

The D flip-flops should be chosen so that
- CLK is rising edge-triggered
- CLEAR is low-level active.

The READY line is used to extend the read and write pulse lengths so that the 80C85RH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.



*ALE AND CLK (OUT) SHOULD BE BUFFERED IF CLK INPUT OF LATCH EXCEEDS 80C85RH IOL OR IOH.

Figure 5. Generation of a Wait State for HS-80C85RH CPU

SYSTEM INTERFACE

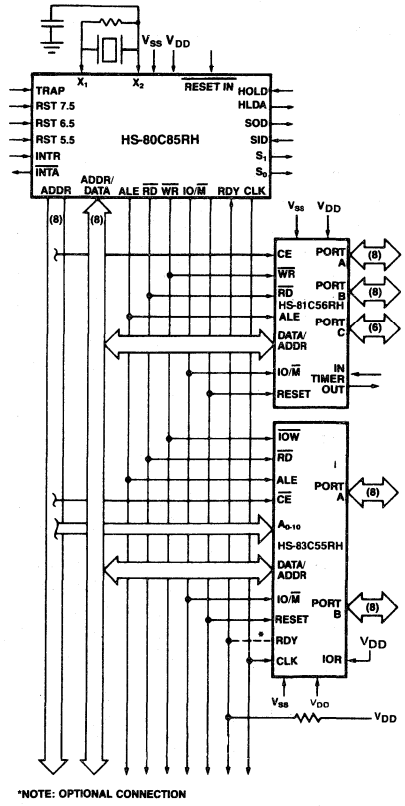
The HS-80C85RH family includes memory components, which are directly compatible to the HS-80C85RH CPU. For example, a system consisting of the three radiation-hardened chips, HS-80C85RH, HS-81C56RH, and HS-83C55RH will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 6.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 7 shows the system configuration of Memory Mapped I/O using HS-80C85RH.

The HS-80C85RH CPU can also interface with the standard radiation-hardened memory that does *not* have the multiplexed address/data bus. It will require use of the HS-82C12RH (8-bit latch) as shown in Figure 8.



*NOTE: OPTIONAL CONNECTION

Figure 6. HS-80C85RH Minimum System (Standard I/O Technique)

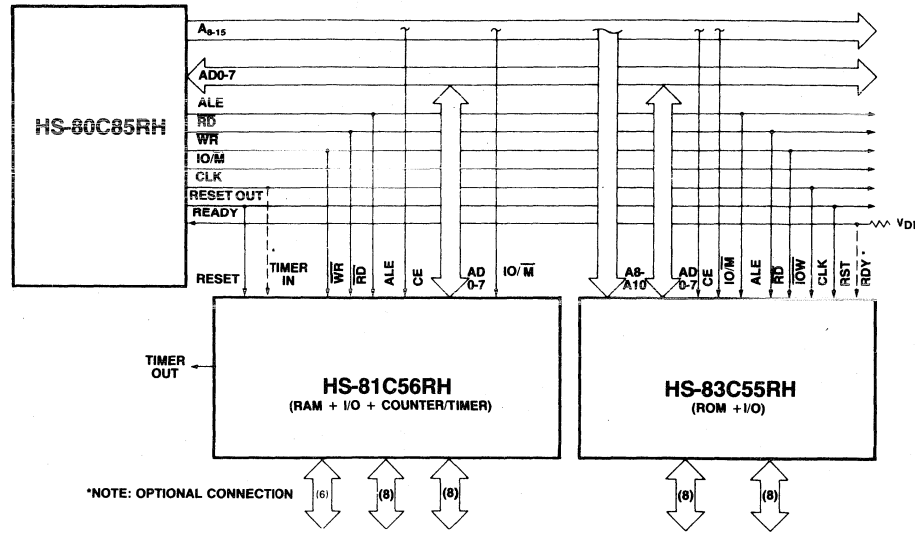


Figure 7. HS-80C85RH Minimum System (Memory Mapped I/O)

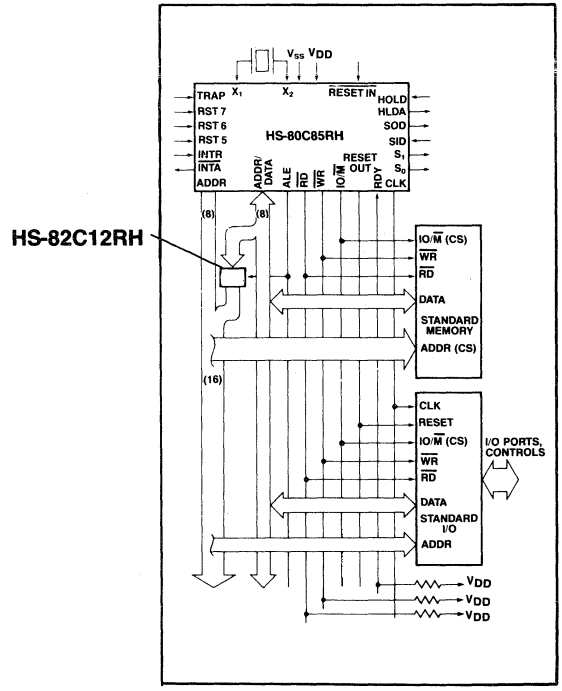


Figure 8. HS-80C85RH System (Using Standard Memories)

BASIC SYSTEM TIMING

The HS-80C85RH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 9 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/$\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 3.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ are used as command lines since they become active when the transfer of data is to take place.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 4.

Table 3. HS-80C85RH Machine Cycle Chart

MACHINE CYCLE			STATUS			CONTROL		
			IO/$\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)		0	1	1	0	1	1
MEMORY READ	(MR)		0	1	0	0	1	1
MEMORY WRITE	(MW)		0	0	1	1	0	1
I/O READ	(IOR)		1	1	0	0	1	1
I/O WRITE	(IOW)		1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)		1	1	1	1	1	0
BUS IDLE	(BI):	DAD	0	1	0	1	1	1
		ACK. OF RST, TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

Table 4. HS-80C85RH Machine State Chart

Machine State	Status & Buses				Control		
	S1,S0	IO/$\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}$,$\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
† IO/M = 1 during T_4-T_6 of INA machine cycle.

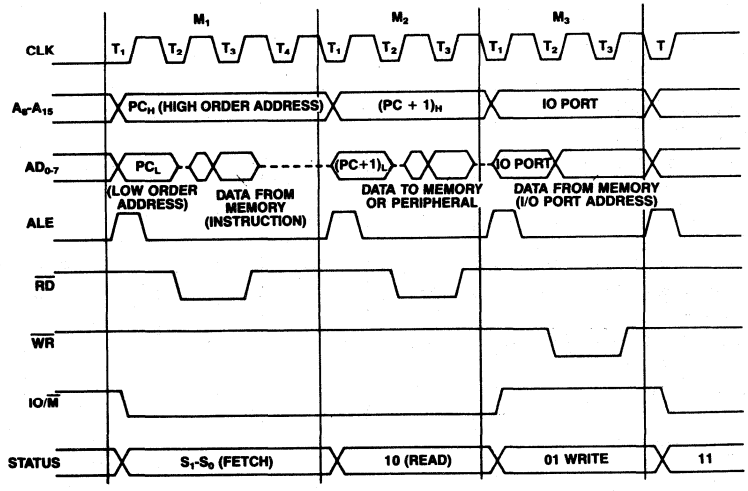


Figure 9. 80C85RH Basic System Timing

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND)..... +7.0V
Input or Output Voltage Applied..... (GND - 0.3V) to (V_{DD} + 0.3V)
Storage Temperature Range .....-65°C to +150°C

Operating Range

Operating Supply Range..... +4.75V to +5.25V
Operating Temperature Range.....-55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

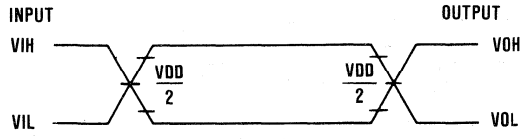
D.C. Electrical Specifications

			(Note 1, 6) RADIATION, TEMPERATURE AND V_{DD} = OP. RANGE			
	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
DC	V_{IL}	Input Low Voltage		+0.8	V	V_{DD} = 4.75V
	V_{IH}	Input High Voltage	V_{DD} -0.5		V	V_{DD} = 4.75V
	V_{OL}	Output Low Voltage		0.5	V	I_{OL} = 1mA, V_{DD} = 5.25V
	V_{OH}	Output High Voltage	V_{DD} -0.5		V	I_{OH} = -1mA, V_{DD} = 4.75V
	I_{DDSB}	Standby Current		500	μA	V_{DD} = 5.25 V
	I_{DDOP}	Operating Current Note 2		5.0	mA/MHz	V_{DD} = 5.25V
	I_I	Input Leakage		±1.0	μA	0 ≤ VIN ≤ VDD
AC	t_{CYC}	CLK Cycle Period	500		ns	Note 4
	t_1	CLK Low Time (Standard CLK Loading	40		ns	
	t_2	CLK High Time (Standard CLK Loading	100		ns	
	t_r, t_f	CLK Rise and Fall Time		100	ns	
	t_{XKR}	X_1 Rising to CLK Rising	30	250	ns	
	t_{XKF}	X_1, Rising to CLK Falling	50	275	ns	
	t_{AC}	A_{8-15} Valid to Leading Edge of Control Note 3	300		ns	
	t_{ACL}	A_{0-7} Valid to Leading Edge of Control	300		ns	
	t_{AD}	A_{0-15} Valid to Valid Data In		875	ns	Notes 4, 7
	t_{AFR}	Address Float After Leading Edge of READ (INTA)		25	ns	Note 4
	t_{AL}	A_{8-15} Valid Before Trailing Edge of ALE Note 3	75		ns	
	t_{ALL}	A_{0-7} Valid Before Trailing Edge of ALE	125		ns	
	t_{ARY}	READY Valid from Address Valid		250	ns	Notes 4, 8, 9
	t_{CA}	Address (A_{8-15}) Valid After Control	150		ns	Note 4
	t_{CC}	Width of Control Low (RD, WR, INTA) Edge of ALE	575		ns	
	t_{CL}	Trailing Edge of Control to Leading Edge of ALE	60		ns	
	t_{DW}	Data Valid to Trailing Edge of WRITE	575		ns	
	t_{HABE}	HLDA to Bus Enable		375	ns	
	t_{HABF}	Bus Float After HLDA		375	ns	

	SYMBOL	PARAMETER	(Notes 1, 6) RADIATION, TEMPERATURE AND V_{DD} = OP. RANGE MIN	MAX	UNITS	TEST CONDITIONS
	t_{HACK}	HLDA Valid to Trailing Edge of CLK	90		ns	Note 4
	t_{HDH}	HOLD Hold Time	0		ns	Notes 4, 8
	t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	300		ns	Notes 4, 8
	t_{INH}	INTR Hold Time	0		ns	Notes 4, 8
	t_{INS}	INTR, RST and TRAP Setup Time to Falling Edge of CLK	375		ns	Notes 4, 8
	t_{LA}	Address Hold Time After ALE	75		ns	Note 4
	t_{LC}	Trailing Edge of ALE to Leading Edge of Control	150		ns	Note 4
	t_{LCK}	ALE Low During CLK High	125		ns	Note 4
	t_{LDR}	ALE to Valid Data During Read		675	ns	Notes 4, 7
AC	t_{LDW}	ALE to Valid Data During Write		350	ns	Note 4
	t_{LL}	ALE Width	200		ns	Note 4
	t_{LRY}	ALE to READY Stable		175	ns	Note 4
	t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling the Address	120		ns	Note 4
	t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		375	ns	Notes 4, 7
	t_{RV}	Control Trailing Edge to Leading Edge of Next Control	550		ns	Note 4
	t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$	0		ns	Notes 4, 8
	t_{RYH}	READY Hold Time	0		ns	Notes 4, 8
	t_{RYS}	READY Setup Time to Leading Edge of CLK	250		ns	Notes 4, 8
	t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	150		ns	Note 4
	t_{WDL}	LEADING Edge of $\overline{WRITE}$ to Data Valid		50	ns	Note 4

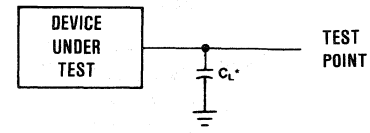
NOTES:
1. All devices guaranteed at worst case limits and over radiation.
2. Operating supply current (I_{DDOP}) is proportional to crystal frequency.
3. A_8-A_{15} address specifications also apply to IO/M, S_0, and S_1 except A_8-A_{15} are undefined during T_4-T_6 of OFF cycle whereas IO/M, S_0, and S_1 are stable.
4. Test Conditions: t_{CYC} = 500ns, C_L = 150pF.
5. Output timings are measured with purely capacitive load.
6. Devices screened to more rigorous electrical specifications are available. Contact your nearest Harris representative for details.
7. **The maximum delay time before valid data is guaranteed.**
8. **These set-up and hold times AC parameters are tested as maximums to guarantee system operation at the lowest minimum.**
9. **This parameter is a set-up time for the ready state.**

AC Testing Input, Output Waveform



AC Testing: All input signals must switch between VIL max and VIH min, tr and tf must be less thatn or equal to 15ns.

AC Testing Load Circuit



*CL includes stray and jig capacitance

TABLE 5. BUS TIMING SPECIFICATION AS A t_{CYC} DEPENDENT

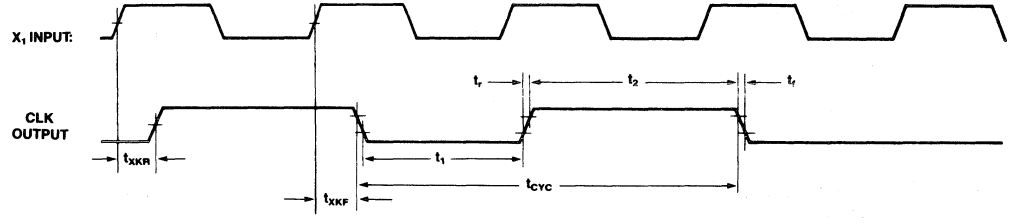
SYMBOL	HS-80C85RH	
t_{AL}	(1/2)T - 175	Minimum
t_{LA}	(1/2)T - 175	Minimum
t_{LL}	(1/2)T - 50	Minimum
t_{LCK}	(1/2)T - 125	Minimum
t_{LC}	(1/2)T - 100	Minimum
t_{AD}	(5/2 + N)T - 375	Maximum
t_{RD}	(3/2 + N)T - 375	Maximum
t_{RAE}	(1/2)T - 130	Minimum
t_{CA}	(1/2)T - 100	Minimum
t_{DW}	(3/2 + N)T - 175	Minimum
t_{WD}	(1/2)T - 100	Minimum

SYMBOL	HS-80C85RH	
t_{CC}	(3/2 + N)T - 175	Minimum
t_{CL}	(1/2)T - 190	Minimum
t_{ARY}	(3/2)T - 500	Maximum
t_{HACK}	(1/2)T - 160	Minimum
t_{HABF}	(1/2)T +125	Maximum
t_{HABE}	(1/2)T +125	Maximum
t_{AC}	(2/2)T - 200	Minimum
t_1	(1/2)T - 210	Minimum
t_2	(1/2)T - 150	Minimum
t_{RV}	(3/2)T - 200	Minimum
t_{LDR}	(4/2)T - 325	Maximum

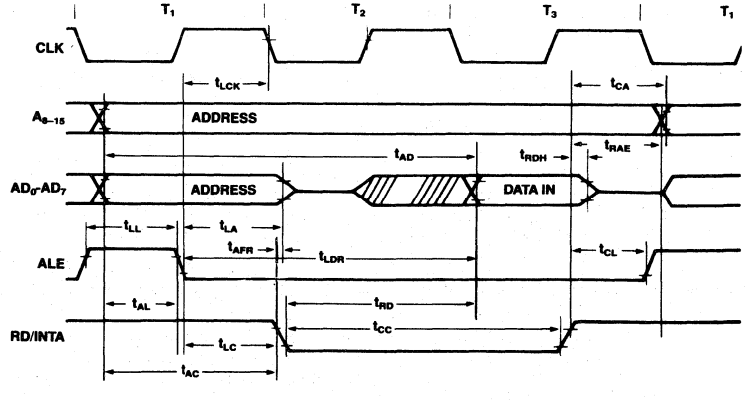
NOTE: N is equal to the total WAIT states. T = t_{CYC}.

Waveforms

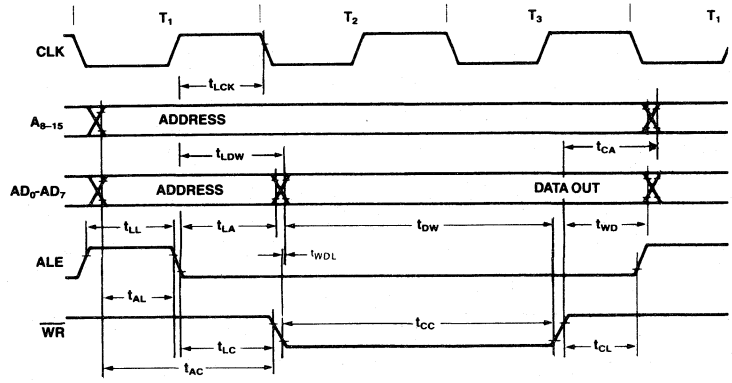
CLOCK



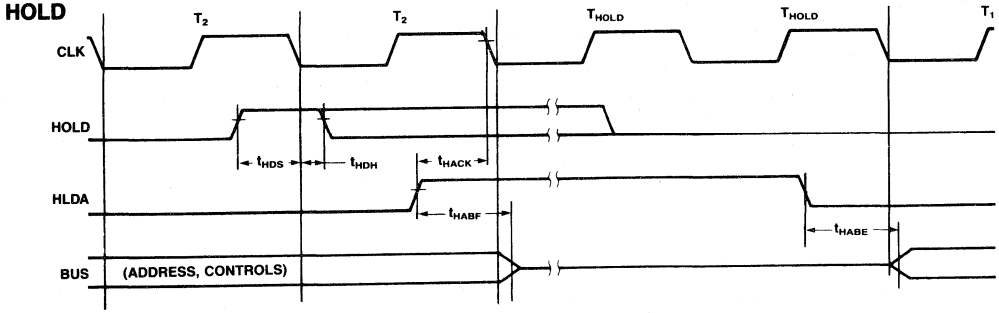
READ



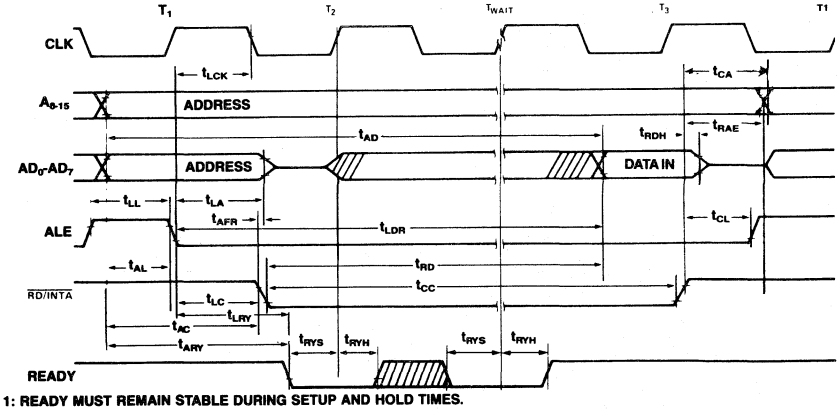
WRITE



HOLD



READ OPERATION WITH WAIT CYCLE (TYPICAL) — SAME READY TIMING APPLIES TO WRITE



NOTE 1: READY MUST REMAIN STABLE DURING SETUP AND HOLD TIMES.

INTERRUPT AND HOLD

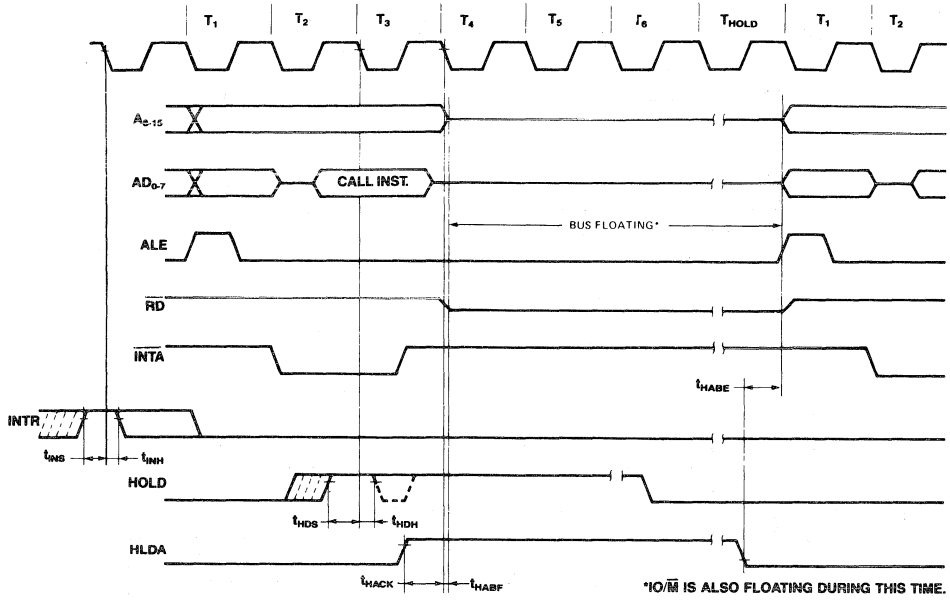


Table 6. Instruction Set Summary

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
MOVE, LOAD, AND STORE		
MOVr1, r2	0 1 D D D S S S	Move register to register
MOV M,r	0 1 1 1 0 S S S	Move register to memory
MOV r,M	0 1 D D D 1 1 0	Move memory to register
MVI r	0 0 D D D 1 1 0	Move immediate register
MVI M	0 0 1 1 0 1 1 0	Move immediate memory
LXI B	0 0 0 0 0 0 0 1	Load immediate register Pair B & C
LXI D	0 0 0 1 0 0 0 1	Load immediate register Pair D & E
LXI H	0 0 1 0 0 0 0 1	Load immediate register Pair H & L
STAX B	0 0 0 0 0 0 1 0	Store A indirect
STAX D	0 0 0 1 0 0 1 0	Store A indirect
LDAX B	0 0 0 0 1 0 1 0	Load A indirect
LDAX D	0 0 0 1 1 0 1 0	Load A indirect
STA	0 0 1 1 0 0 1 0	Store A direct
LDA	0 0 1 1 1 0 1 0	Load A direct
SHLD	0 0 1 0 0 0 1 0	Store H & L direct
LHLD	0 0 1 0 1 0 1 0	Load H & L direct
XCHG	1 1 1 0 1 0 1 1	Exchange D & E, H & L Registers
STACK OPS		
PUSH B	1 1 0 0 0 1 0 1	Push register Pair B & C on stack
PUSH D	1 1 0 1 0 1 0 1	Push register Pair D & E on stack
PUSH H	1 1 1 0 0 1 0 1	Push register Pair H & L on stack
PUSH PSW	1 1 1 1 0 1 0 1	Push A and Flags on stack

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
CZ	1 1 0 0 1 1 0 0	Call on zero
CNZ	1 1 0 0 0 1 0 0	Call on no zero
CP	1 1 1 1 0 1 0 0	Call on positive
CM	1 1 1 1 1 1 0 0	Call on minus
CPE	1 1 1 0 1 1 0 0	Call on parity even
CPO	1 1 1 0 0 1 0 0	Call on parity odd
RETURN		
RET	1 1 0 0 1 0 0 1	Return
RC	1 1 0 1 1 0 0 0	Return on carry
RNC	1 1 0 1 0 0 0 0	Return on no carry
RZ	1 1 0 0 1 0 0 0	Return on zero
RNZ	1 1 0 0 0 0 0 0	Return on no zero
RP	1 1 1 1 0 0 0 0	Return on positive
RM	1 1 1 1 1 0 0 0	Return on minus
RPE	1 1 1 0 1 0 0 0	Return on parity even
RPO	1 1 1 0 0 0 0 0	Return on parity odd
RESTART		
RST	1 1 A A A 1 1 1	Restart
INPUT/OUTPUT		
IN	1 1 0 1 1 0 1 1	Input
OUT	1 1 0 1 0 0 1 1	Output
INCREMENT AND DECREMENT		
INR r	0 0 D D D 1 0 0	Increment register
DCR r	0 0 D D D 1 0 1	Decrement register
INR M	0 0 1 1 0 1 0 0	Increment memory
DCR M	0 0 1 1 0 1 0 1	Decrement memory
INX B	0 0 0 0 0 0 1 1	Increment B & C registers
INX D	0 0 0 1 0 0 1 1	Increment D & E registers

Table 6. Instruction Set Summary (Continued)

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
POP B	1	1	0	0	0	0	0	1	Pop register Pair B & C off stack
POP D	1	1	0	1	0	0	0	1	Pop register Pair D & E off stack
POP H	1	1	1	0	0	0	0	1	Pop register Pair H & L off stack
POP PSW	1	1	1	1	0	0	0	1	Pop A and Flags off stack
XTHL	1	1	1	0	0	0	1	1	Exchange top of stack, H & L
SPHL	1	1	1	1	1	0	0	1	H & L to stack pointer
LXI SP	0	0	1	1	0	0	0	1	Load immediate stack pointer
INX SP	0	0	1	1	0	0	1	1	Increment stack pointer
DCX SP	0	0	1	1	1	0	1	1	Decrement stack pointer
JUMP									
JMP	1	1	0	0	0	0	1	1	Jump unconditional
JC	1	1	0	1	1	0	1	0	Jump on carry
JNC	1	1	0	1	0	0	1	0	Jump on no carry
JZ	1	1	0	0	1	0	1	0	Jump on zero
JNZ	1	1	0	0	0	0	1	0	Jump on no zero
JP	1	1	1	1	0	0	1	0	Jump on positive
JM	1	1	1	1	1	0	1	0	Jump on minus
JPE	1	1	1	0	1	0	1	0	Jump on parity even
JPO	1	1	1	0	0	0	1	0	Jump on parity odd
PCHL	1	1	1	0	1	0	0	1	H & L to program counter
CALL									
CALL	1	1	0	0	1	1	0	1	Call unconditional
CC	1	1	0	1	1	1	0	0	Call on carry
CNC	1	1	0	1	0	1	0	0	Call on no carry
LOGICAL									
ANA r	1	0	1	0	0	S	S	S	And register with A
XRA r	1	0	1	0	1	S	S	S	Exclusive OR register with A
ORA r	1	0	1	1	0	S	S	S	OR register with A
CMP r	1	0	1	1	1	S	S	S	Compare register with A
ANA M	1	0	1	0	0	1	1	0	And memory with A
XRA M	1	0	1	0	1	1	1	0	Exclusive OR memory with A
ORA M	1	0	1	1	0	1	1	0	OR memory with A
CMP M	1	0	1	1	1	1	1	0	Compare memory with A
ANI	1	1	1	0	0	1	1	0	And immediate with A
XRI	1	1	1	0	1	1	1	0	Exclusive OR immediate with A
ORI	1	1	1	1	0	1	1	0	OR immediate with A
CPI	1	1	1	1	1	1	1	0	Compare immediate with A
ROTATE									
RLC	0	0	0	0	0	1	1	1	Rotate A left
RRC	0	0	0	0	1	1	1	1	Rotate A right
RAL	0	0	0	1	0	1	1	1	Rotate A left through carry
RAR	0	0	0	1	1	1	1	1	Rotate A right through carry

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
INX H	0	0	1	0	0	0	1	1	Increment H & L registers
DCX B	0	0	0	0	1	0	1	1	Decrement B & C
DCX D	0	0	0	1	1	0	1	1	Decrement D & E
DCX H	0	0	1	0	1	0	1	1	Decrement H & L
ADD									
ADD r	1	0	0	0	0	S	S	S	Add register to A
ADC r	1	0	0	0	1	S	S	S	Add register to A with carry
ADD M	1	0	C	0	0	1	1	0	Add memory to A
ADC M	1	0	0	0	1	1	1	0	Add memory to A with carry
ADI	1	1	0	0	0	1	1	0	Add immediate to A
ACI	1	1	0	0	1	1	1	0	Add immediate to A with carry
DAD B	0	0	0	0	1	0	0	1	Add B & C to H & L
DAD D	0	0	0	1	1	0	0	1	Add D & E to H & L
DAD H	0	0	1	0	1	0	0	1	Add H & L to H & L
DAD SP	0	0	1	1	1	0	0	1	Add stack pointer to H & L
SUBTRACT									
SUB r	1	0	0	1	0	S	S	S	Subtract register from A
SBB r	1	0	0	1	1	S	S	S	Subtract register from A with borrow
SUB M	1	0	0	1	0	1	1	0	Subtract memory from A
SBB M	1	0	0	1	1	1	1	0	Subtract memory from A with borrow
SUI	1	1	0	1	0	1	1	0	Subtract immediate from A
SBI	1	1	0	1	1	1	1	0	Subtract immediate from A with borrow
SPECIALS									
CMA	0	0	1	0	1	1	1	1	Complement A
STC	0	0	1	1	0	1	1	1	Set carry
CMC	0	0	1	1	1	1	1	1	Complement carry
DAA	0	0	1	0	0	1	1	1	Decimal adjust A
CONTROL									
EI	1	1	1	1	1	0	1	1	Enable Interrupts
DI	1	1	1	1	0	0	1	1	Disable Interrupt
NOP	0	0	0	0	0	0	0	0	No-operation
HLT	0	1	1	1	0	1	1	0	Halt
RIM	0	0	1	0	0	0	0	0	Read Interrupt Mask
SIM	0	0	1	1	0	0	0	0	Set Interrupt Mask

NOTES:
1. DDS or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

Radiation Screening Procedure

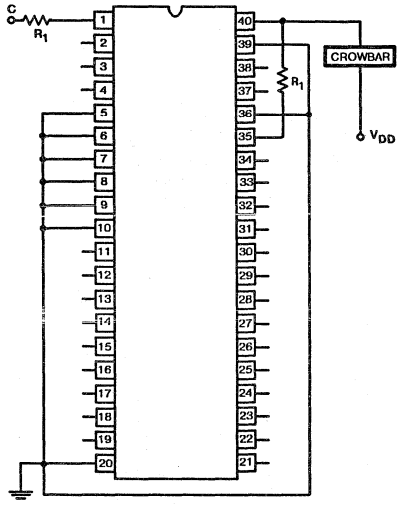
1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested to the customer's specification for proper operation.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad-Si (±10%) from a Gamma-cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The lot will be accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-80C85RH has been designed to survive in a radiation environment and to meet the electrical characteristcs. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1×10^5 Rad-Si. Transient radiation tests have shown the following results:

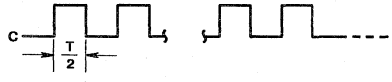
- Latch-up free to doses $\geq 1 \times 10^{12}$ rads/sec.
- Upset (loss of stored data) $\geq 1 \times 10^8$ rads/sec.

Burn-in Circuits

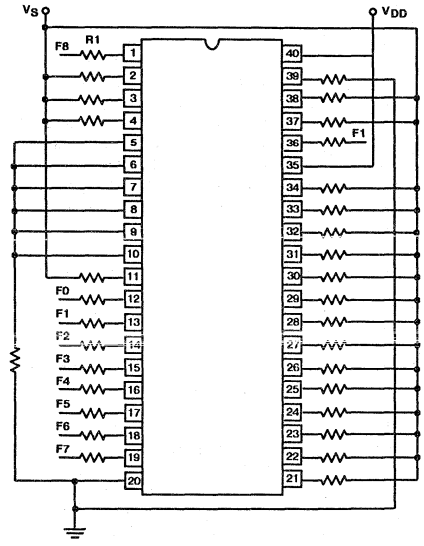


STATIC CONFIGURATION

Minimum Temperature = +125°C
V_{DD} = 10V ± 5% R1 = 1kΩ, 1/4W

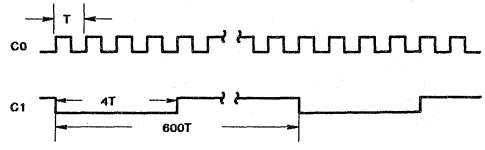


C Must Be Pulsed a Minimum of 10 Times.
C is Grounded After Initial Pulses. T > 200ns.



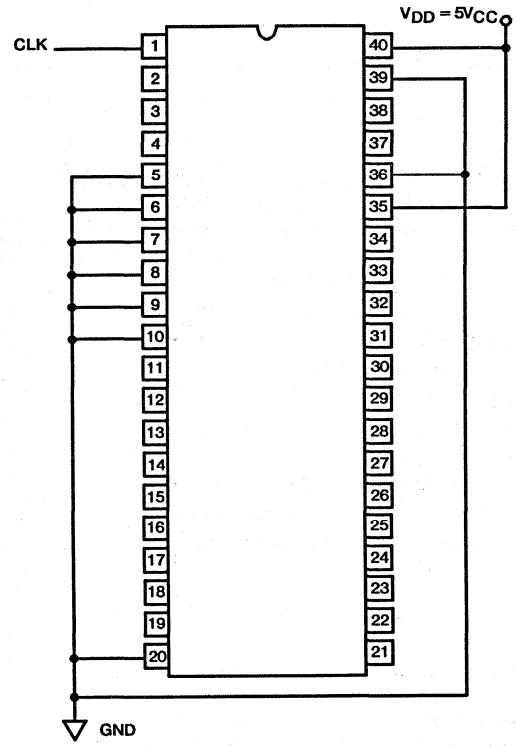
DYNAMIC CONFIGURATION

T = 5µs, F0 = 200kHz, 50% duty cycle, F1 used to periodically reset processor.
Minimum Temperature = +125°C, V_{DD} = 10V ± 5%.
All resistors 100kΩ



SIGNAL NAME	FREQUENCY	DUTY CYCLE
F0	50KHz	50%
F1	F0/2	50%
F2	F1/2	50%
F3	F2/2	50%
F4	F3/2	50%
F5	F4/2	50%
F6	F5/2	50%
F7	F6/2	50%

Irradiation Circuit



NOTE: Clk must be pulsed 10 cycles (0-5V, 50% Duty Cycle) for initial set-up. Pin 1 should be left at GND.

HARRIS

HS-80C86RH

Radiation Hardened CMOS 16-Bit Microprocessor

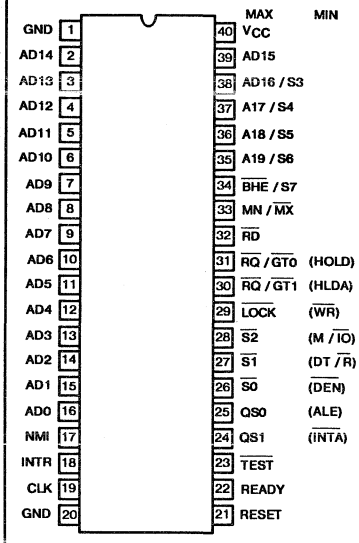
July 1990

Features

- Radiation Hardened
  - Latch Up Free EPI-CMOS
  - Total Dose ..... > 100K RAD(Si)
  - Transient Upset ..... > 10^8 RAD(Si)/sec
  - Functional after Total Dose ..... 1 x 10^6 RAD(Si)
- Low Power Operation
  - ICCSB = 500µA Maximum
  - ICCOP = 12mA/MHz Maximum
- Pin Compatible with NMOS 8086 and Harris 80C86
- Completely Static Design DC to 5MHz
- 1 Mbyte of Direct Memory Addressing Capability
- 24 Operand Addressing Modes
- Bit, Byte, Word, and Block Move Operations
- 8 and 16 Bit Signed/Unsigned Arithmetic
  - Binary or Decimal
  - Multiply and Divide
- Bus-hold Circuitry Eliminates Pull-up Resistors for CMOS Designs
- Hardened Field, Self Aligned, Junction Isolated CMOS Process
- Single 5V Power Supply
- Military Temperature Range..... -55°C to +125°C

Pinout

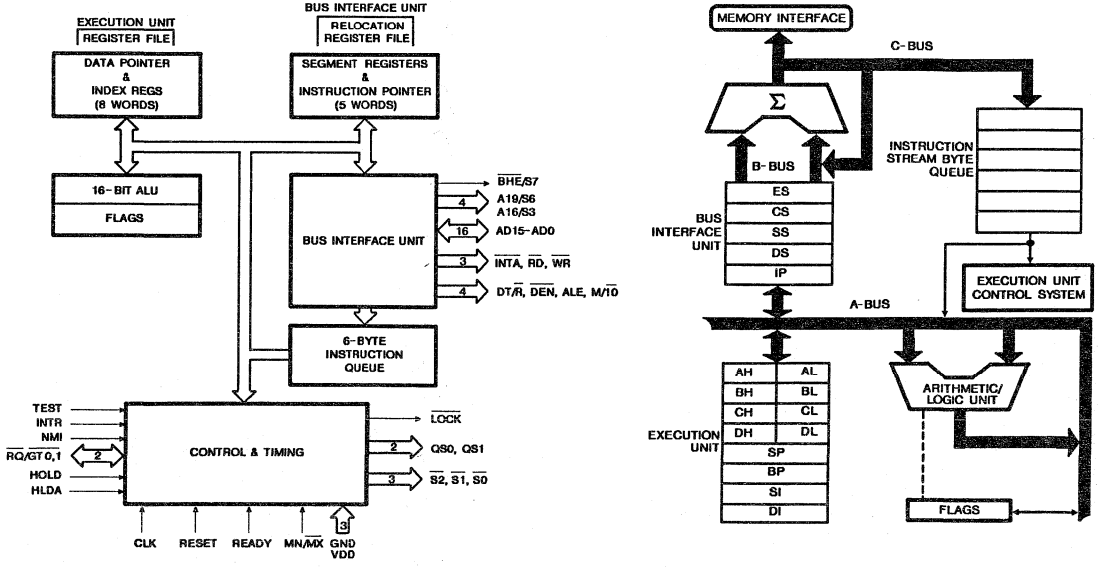
DIP
TOP VIEW



Description

The Harris HS-80C86RH high performance radiation hardened 16 bit CMOS CPU is manufactured using a hardened field, self-aligned silicon gate CMOS process. Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multi-processing, allow user configuration to achieve the highest performance level. Industry standard operation allows use of existing NMOS 8086 hardware and software designs.

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

The following pin function descriptions are for HS-80C86RH systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the HS-80C86RH (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
AD_{15}-AD_0	2-16, 39	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, T_W, T_4) bus. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7-D_0. It is LOW during T1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use AD_0 to condition chip select functions (See $\overline{BHE}$). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A_{19}/S_6 A_{18}/S_5 A_{17}/S_4 A_{16}/S_3	35-38	O	ADDRESS/STATUS: During T_1, these are the four most significant address lines for memory operations. During I/O operations these lines are low. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W, T_4. S_6 is always zero. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. S_4 and S_3 are encoded as shown in (Table 1). This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence".
$\overline{BHE}/S_7$	34	O	BUS HIGH ENABLE/STATUS: During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D_{15}-D_8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. BHE is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S_7 status information is available during T_2, T_3 and T_4. The signal is active LOW, and is held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence"; it is LOW during T_1 for the first interrupt acknowledge cycle. (See Table 2).
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the $M/\overline{IO}$ or $\overline{S_2}$ pin. This signal is used to read devices which reside on the HS-80C86RH local bus. $\overline{RD}$ is active LOW during T_2, T_3 and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the 80C86 local bus has floated. This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence".
READY	22	I	READY: is the acknowledgement from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the HS-82C85RH Clock Generator to form READY. This signal is active HIGH. The HS-80C86RH READY input is not synchronized. Correct operation is not guaranteed if the Setup and Hold Times are not met.
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. If so, an interrupt service routine is called via an interrupt vector lookup table located in system memory. INTR is internally synchronized and can be internally masked by software resetting the interrupt enable bit. This signal is active HIGH.
$\overline{TEST}$	23	I	TEST: input is examined by the "Wait" instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. An interrupt service routine is called via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must change from LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VDD	40		VDD: +5V power supply pin. A 0.1μF capacitor between pins 20 and 40 is recommended for decoupling.
GND	1, 20		GND: Ground. Note: both must be connected. A 0.1μF capacitor between pins 1 and 20 is recommended for decoupling.
MN/$\overline{MX}$	33	I	MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

Pin Description

The following pin function descriptions are for the HS-80C86RH system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described below.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	26-28	O	STATUS: is active during T_4, T_1 and T_2 and is returned to the passive state (1, 1, 1) during T_3 or during T_W when READY is HIGH. This status is used by the 82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$ or $\overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle. These status lines are encoded as shown in Table 3. These signals are held at a high impedance logic one state during "grant sequence".
$\overline{RQ}/\overline{GT_0}$ $\overline{RQ}/\overline{GT_1}$	31, 30	I/O	REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bi-directional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ}/\overline{GT}$ Sequence Timing) 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the HS-80C86RH (pulse 1). 2. During a T_4 or T_I clock cycle, a pulse 1 CLK wide from the HS-80C86RH to the requesting master (pulse 2) indicates that the HS-80C86RH has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse 1 CLK wide from the requesting master indicates to the HS-80C86RH (pulse 3) that the "hold" request is about to end and that the HS-80C86RH can reclaim the local bus at the next CLK. The CPU then enters T_4 (or T_I if no bus cycles pending). Each Master-Master exchange of the local bus is a sequence of 3 pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met: 1. Request occurs on or before T_2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next cycle. 2. A memory cycle will start within three clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	29	O	LOCK: output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a HIGH impedance logic one state during "grant sequence". In MAX mode, $\overline{LOCK}$ is automatically generated during T_2 of the first $\overline{INTA}$ cycle and removed during T_2 of the second $\overline{INTA}$ cycle.
QS_1, QS_0	24, 25	O	QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS_1 and QS_0 provide status to allow external tracking of the internal HS-80C86RH instruction queue. Note that QS_1, QS_0 never become high impedance. QS_1 QS_0 0 0 No Operation 0 1 First Byte of Op Code from Queue 1 0 Empty the Queue 1 1 Subsequent Byte from Queue

TABLE 1.

S_4	S_3	CHARACTERISTICS
0	0	Alternate Data
0	1	Stack
1	0	Code or None
1	1	Data

TABLE 2.

$\overline{BHE}$	A_0	CHARACTERISTICS
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

TABLE 3.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

Pin Description

The following pin function descriptions are for the HS-80C86RH in minimum mode (i.e. MN/$\overline{MX}$ = V_{DD}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described below.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
M/$\overline{IO}$	28	O	STATUS LINE: logically equivalent to $\overline{S_2}$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ is held to a high impedance logic zero during local bus "hold acknowledge".
$\overline{WR}$	29	O	WRITE: indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T_2, T_3 and TW of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTERRUPT ACKNOWLEDGE: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3 and TW of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82 latch. It is a HIGH pulse active during clock LOW of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in maximum mode, and its timing is the same as for M/$\overline{IO}$ (T = HIGH, R = LOW). DT/$\overline{R}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{DEN}$	26	O	DATA ENABLE: provided as an output enable for a bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of T_2 until the middle of T_4, while for a write cycle it is active from the beginning of T_2 until the middle of T_4. $\overline{DEN}$ is held to a high impedance logic one during local bus "hold acknowledge".
HOLD HLDA	31, 30	I O	HOLD: indicates that another master is requesting a local bus "hold". To be a acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T_4 or T_I clock cycle. Simultaneously with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

Functional Description

Static Operation

All HS-80C86RH circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS HS-80C86RH can operate from DC to 5MHz. The processor clock may be stopped in either state (HIGH/LOW) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The HS-80C86RH can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since HS-80C86RH power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the HS-80C86RH power requirement is the standby current, (500μA maximum).

Internal Architecture

The internal functions of the HS-80C86RH processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU functional diagram.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching

provided by this unit serves to increase processor performance through improved bus bandwidth utitization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead-time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20-bit address to memory, which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 1).

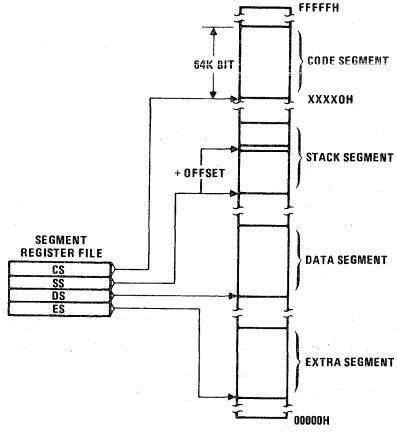


FIGURE 1. HS-80C86RH MEMORY ORGANIZATION

TABLE 4.

TYPE OF MEMORY REFERENCE	DEFAULT SEGMENT BASE	ALTERNATE SEGMENT BASE	OFFSET
Instruction Fetch	CS	None	IP
Stack Operation	SS	None	SP
Variable (except following)	DS	CS, ES, SS	Effective Address
String Source	DS	CS, ES, SS	SI
String Destination	ES	None	DI
BP Used As Base Register	SS	CS, DS, ES	Effective Address

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the specific rules of Table 4. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster and more structured. (See Table 4).

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. The performance penalty does not occur for instruction fetches; only word operands.

Physically, the memory is organized as a high bank (D15-D8) and a low bank (D7-D0) of 512K bytes addressed in parallel by the processor's address lines.

Byte data with even addresses is transferred on the D7-D0 bus lines while odd addressed byte data (A_0 HIGH) is transferred on the D15-D8 bus lines. The processor provides two enable signals, $\overline{BHE}$ and A_0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor at the byte level as necessary.

In referencing word data, the BIU requires one or two memory cycles depending on whether the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (See Figure 2). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed thru its own pair of 16-bit pointers - segment address pointer and offset address pointer. The first pointer, used as the offset address, is loaded into the IP and the second pointer, which designates the base address is loaded into the CS. At this point program control is transferred to the interrupt routine.

The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

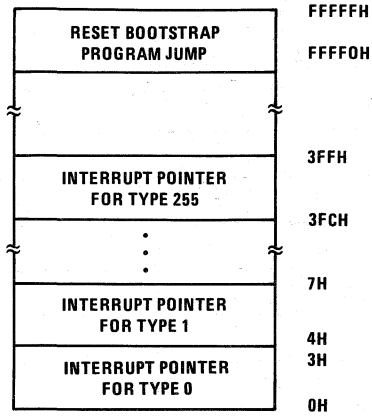


FIGURE 2. RESERVED MEMORY LOCATIONS

Minimum and Maximum Operation Modes

The requirements for supporting minimum and maximum HS-80C86RH systems are sufficiently different that they cannot be met efficiently using 40 uniquely defined pins. Consequently, the HS-80C86RH is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the HS-80C86RH defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to V_{DD}, the HS-80C86RH generates bus control signals itself on pins 24 through 31 and 34.

Bus Operation

The HS-80C86RH has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of 82C82 latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T_1, T_2, T_3 and T_4 (see Figure 3). The address is emitted from the processor during T_1 and data transfer occurs on the bus during T_3 and T_4. T_2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (TW) are inserted between T_3 and T_4. Each inserted wait state is the same duration as a CLK cycle. Idle periods occur between HS-80C86RH driven bus cycles whenever the processor performs internal processing.

During T_1 of any bus cycle, the ALE (Address Latch Enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$ and $\overline{S_2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to Table 5.

TABLE 5.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0	0	0	Interrupt
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

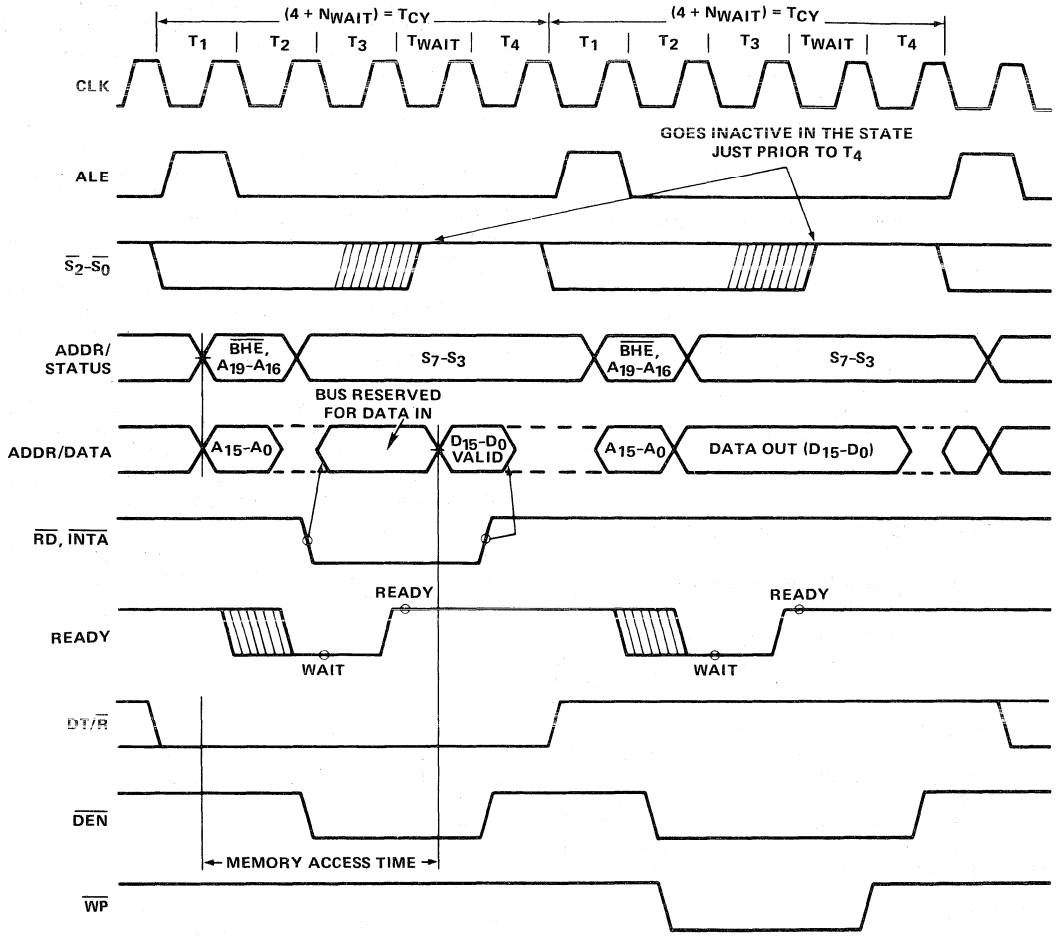


FIGURE 3. BASIC SYSTEM TIMING

Status bits S_3 through S_7 are time multiplexed with high order address bits and the $\overline{BHE}$ signal, and are therefore valid during T_2 through T_4. S_3 and S_4 indicate which segment register (see Instruction Set Description) was used for this bus cycle in forming the address, according to Table 6.

TABLE 6.

S_4	S_3	CHARACTERISTICS
0(LOW)	0	Alternate Data (extra segment)
0	1	Stack
1(HIGH)	0	Code or None
1	1	Data

S_5 is a reflection of the PSW interrupt enable bit. S_6 is always zero and S_7 is a spare status bit.

I/O Addressing

In the HS-80C86RH, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D7-D0 bus lines and odd addressed bytes on D15-D8. Care must be taken to ensure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

External Interface

Processor RESET and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The HS-80C86RH RESET is required to be HIGH for greater than 4 CLK cycles. The HS-80C86RH will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval, the HS-80C86RH operates normally beginning with the instruction in absolute location FFFF0H. (See Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH-to-LOW transition of RESET must occur no sooner than 50μs (or 4 CLK cycles, whichever is greater) after power-up, to allow complete initialization of the HS-80C86RH.

NMI will not be recognized prior to the second CLK cycle following the end of RESET. If NMI is asserted sooner than nine clock cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate need for pull-up/down resistors, "bus-hold" circuitry has been used on the HS-80C86RH pins 2-16, 26-32 and 34-39. (See Figure 4A and 4B). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set Description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service routine locations resides in absolute locations 0 through 3FFH, which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the interrupt service routine location. All flags and both the Code Segment and Instruction Pointer register are saved as part of the $\overline{INTA}$ sequence. These are restored upon execution of an Interrupt Return (IRET) instruction.

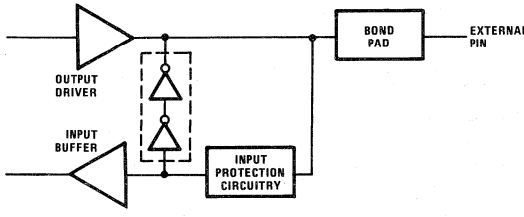


FIGURE 4A. BUS HOLD CIRCUITRY PIN 2-16, 34-39

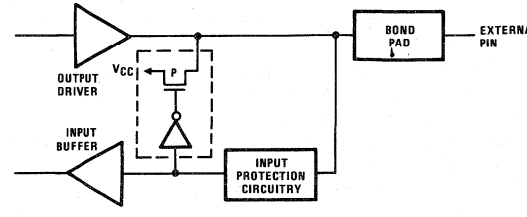


FIGURE 4B. BUS HOLD CIRCUITRY PIN 26-32

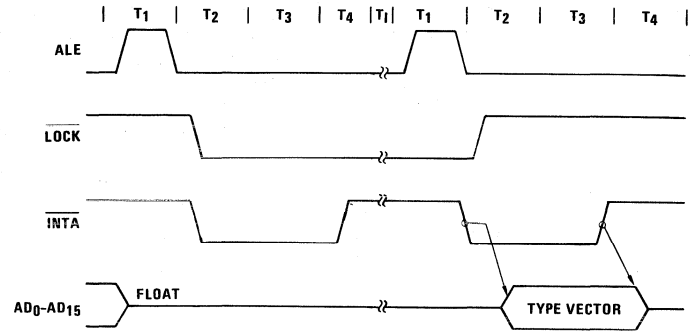


FIGURE 5. INTERRUPT ACKNOWLEDGE SEQUENCE

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any positive transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during or after the servicing of NMI. Another positive edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The HS-80C86RH provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable flag (IF) status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block- type instruction. INTR may be removed anytime after the falling edge of the first $\overline{INTA}$ signal. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 5) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The HS-80C86RH emits the $\overline{LOCK}$ signal (Max mode only) from T_2 of the first bus cycle until T_2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is supplied to the HS-80C86RH by the HS-82C59ARH Interrupt Controller, which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector look-up table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

Halt

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode the processor issues appropriate HALT status on $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ and the 82C88 bus controller issues one ALE. The HS-80C86RH will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator at the end of the local bus hold. An NMI or interrupt request (when interrupts enabled) or RESET will force the HS-80C86RH out of the "HALT" state.

Read/Modify/Write (Semaphore)

Operations Via Lock

The $\overline{LOCK}$ status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This gives the processor the

capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (forced LOW) in the clock cycle following decoding of the software "LOCK" prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While $\overline{LOCK}$ is active a request on a $\overline{RQ}/\overline{GT}$ pin will be recorded and then honored at the end of the $\overline{LOCK}$.

External Synchronization Via TEST

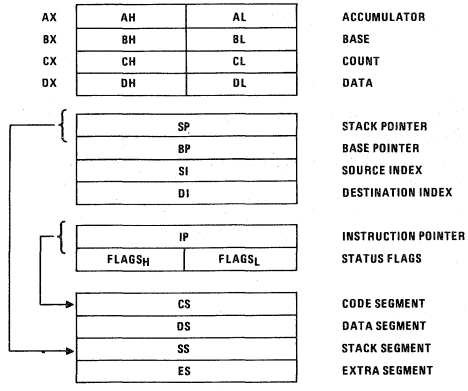
As an alternative to interrupts, the HS-80C86RH provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{TEST}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the HS-80C86RH three-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the HS-80C86RH will recognize interrupts and process them when it regains control of the bus. The WAIT instruction is then refetched, and reexecuted.

Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 6A and 6B, respectively. In minimum mode, the MN/$\overline{MX}$ pin is strapped to V_{DD} and the processor emits bus control signals (e.g. $\overline{RD}$, $\overline{WR}$, etc.) directly. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller used to generate MULTIBUS™ compatible bus control signals. Figure 3 shows the signal timing relationships.

TABLE 7. HS-80C86RH REGISTER MODEL



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System Timing - Minimum System

The read cycle begins in T_1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD_0-AD_{15}) at this time, into the 82C82 latches. The $\overline{BHE}$ and A_0 signals address the low, high or both bytes. From T_1 to T_4 the M/$\overline{IO}$ signal indicates a memory or I/O operation. At T_2, the address is removed from the address/data bus and the bus is held at the last valid logic state by internal bus hold devices. The read control signal is also asserted at T_2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will three-state its bus drivers. If a transceiver is required to buffer the HS-80C86RH local bus, signals DT/R and DEN are provided by the HS-80C86RH.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/$\overline{IO}$ signal is again asserted to indicate a memory or I/O write operation. In T_2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T_4. During T_2, T_3 and T_W, the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T_2 as opposed to the read which is delayed somewhat into T_2 to provide time for output drivers to become inactive.

The $\overline{BHE}$ and A_0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to Table 8.

TABLE 8.

$\overline{BHE}$	A_0	CHARACTERISTICS
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D7-D0 bus lines and odd address bytes on D15-D8.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is held at the last valid logic state by internal bus hold devices. (See Figure 4). In the second of two successive $\overline{INTA}$ cycles a byte of information is read from the data bus (D7-D0) as supplied by the interrupt system logic (i.e. HS-82C59ARH Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

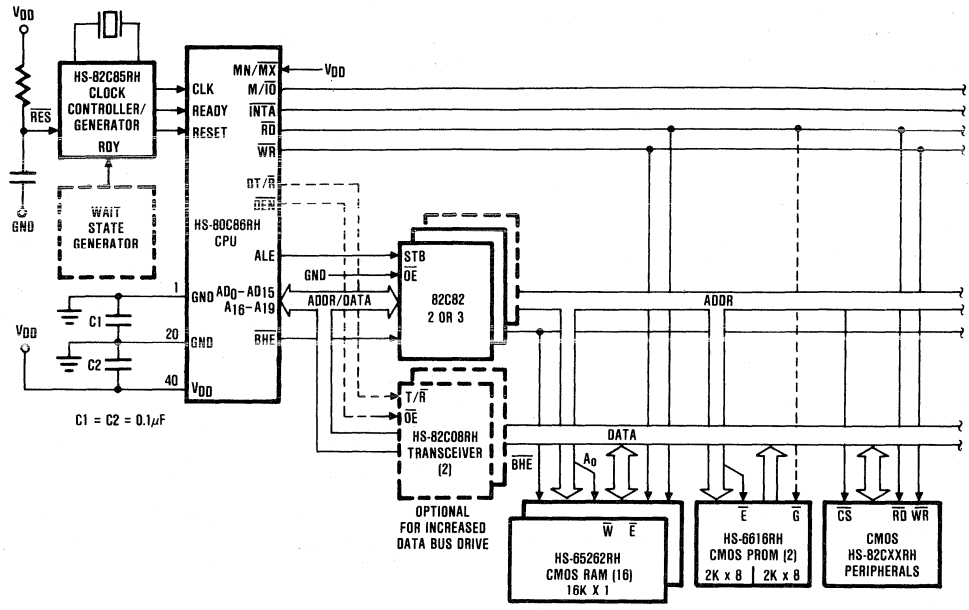


FIGURE 6A. MINIMUM MODE HS-80C86RH TYPICAL CONFIGURATION

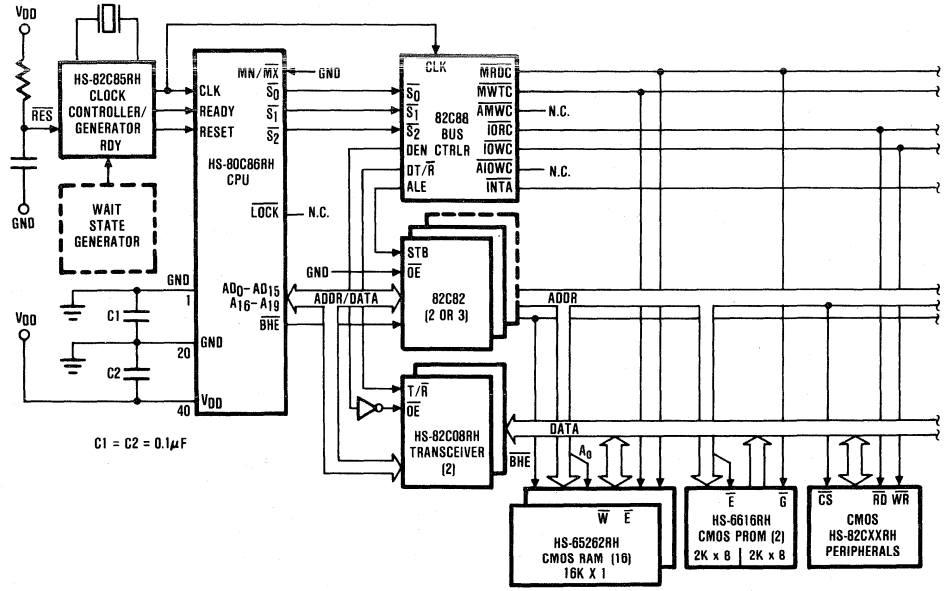


FIGURE 6B. MAXIMUM MODE HS-80C86RH TYPICAL CONFIGURATION

Bus Timing - Medium And Large Size Systems

For medium complexity systems the MN/$\overline{MX}$ pin is connected to GND and the 82C88 Bus Controller is added to the system as well as three 82C82 latches for latching the system address, and a transceiver to allow for bus loading greater than the HS-80C86RH is capable of handling. Bus control signals are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The HS-80C86RH status outputs ($\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$) provide type-of-cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The transceiver receives the usual T and OE inputs from the 82C88 DT/$\overline{R}$ and DEN signals.

For large multiple processor systems, the 82C89 bus arbiter must be added to the system to provide system bus management. In this case, the pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can be derived from an HS-82C59ARH located on either the local bus or the system bus. The processor's $\overline{INTA}$ output should drive the SYSB/$\overline{RESB}$ input of the 82C89 to the proper state when reading the interrupt vector number from the HS-82C59ARH during the interrupt acknowledge sequence and software "poll".

A Note on Radiation Hardened Product Availability

There are no immediate plans to develop the 82C88 Bus Controller or the 82C89 Arbiter as radiation hardened integrated circuits in packaged form. However, for systems requiring these circuits, they are available as soft coded LSI macros in the Harris HSC-RH radiation hardened Standard Cell.

Absolute Maximum Ratings

Supply Voltage .....+7.0 Volts
Input Voltage Applied.....GND -0.5V to V_{DD} +0.5V
Output Voltage Applied.....GND -0.5V to V_{DD} +0.5V
Storage Temperature Range .....-65°C to +150°C
Maximum Power Dissipation .....1 Watt

Operating Conditions

Operating Voltage Range.....+5 to ±10%
Operating Temperature Range.....-55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

D.C. Electrical Specifications

V_{DD} = 5.5V except VOL, VOH; VOL and VOH have V_{DD} = 4.5V; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	3.5		V	
VIL	Logical Zero Input Voltage		0.8	V	
VIHC	CLK Logical One Input Voltage	V_{DD} -0.8		V	
VILC	CLK Logical Zero Input Voltage		0.8	V	
VOH	Output High Voltage	3.0 V_{DD} -0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	1.0	μA	VIN = GND or V_{DD} Pins 17-19, 21-23, 33
IBHH	Input Current-Bus Hold High	-600	-40	μA	VIN = 3.0V (See Note 1)
IBHL	Input Current-Bus Hold Low	40	600	μA	VIN = 0.8V (See Note 2)
IO	Output Leakage Current	-10.0	10.0	μA	VOUT = GND or V_{DD} Pins 2-16, 26-29, 32, 34-39
IDDSB	Standby Power Supply Current		500	μA	V_{DD} = 5.5V VIN = V_{DD} or GND Outputs Unloaded (See Note 3)
IDDOP	Operating Power Supply Current		12	mA/MHz	V_{DD} = 5.5V

Capacitance

T_A = 25°C; V_{DD} = GND = 0V; VIN = +5V or GND.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CIN*	Input Capacitance		15	pF	FREQ = 1MHz. Unmeasured pins returned to GND
COUT*	Output Capacitance		15	pF	
CI/O*	I/O Capacitance		20	pF	

*Guaranteed and sampled, not 100% tested.

NOTES: 1. IBHH should be measured after raising VIN to V_{DD} and then lowering to 3.0V on the following pins: 2-16, 26-32, 34-39.
2. IBHL should be measured after lowering VIN to GND and then raising to 0.8V on the following pins: 2-16, 34-39.
3. IDDSB tested during clock high time after halt instruction executed. VIN = V_{DD} or GND, V_{DD} = 5.5V, Outputs unloaded.

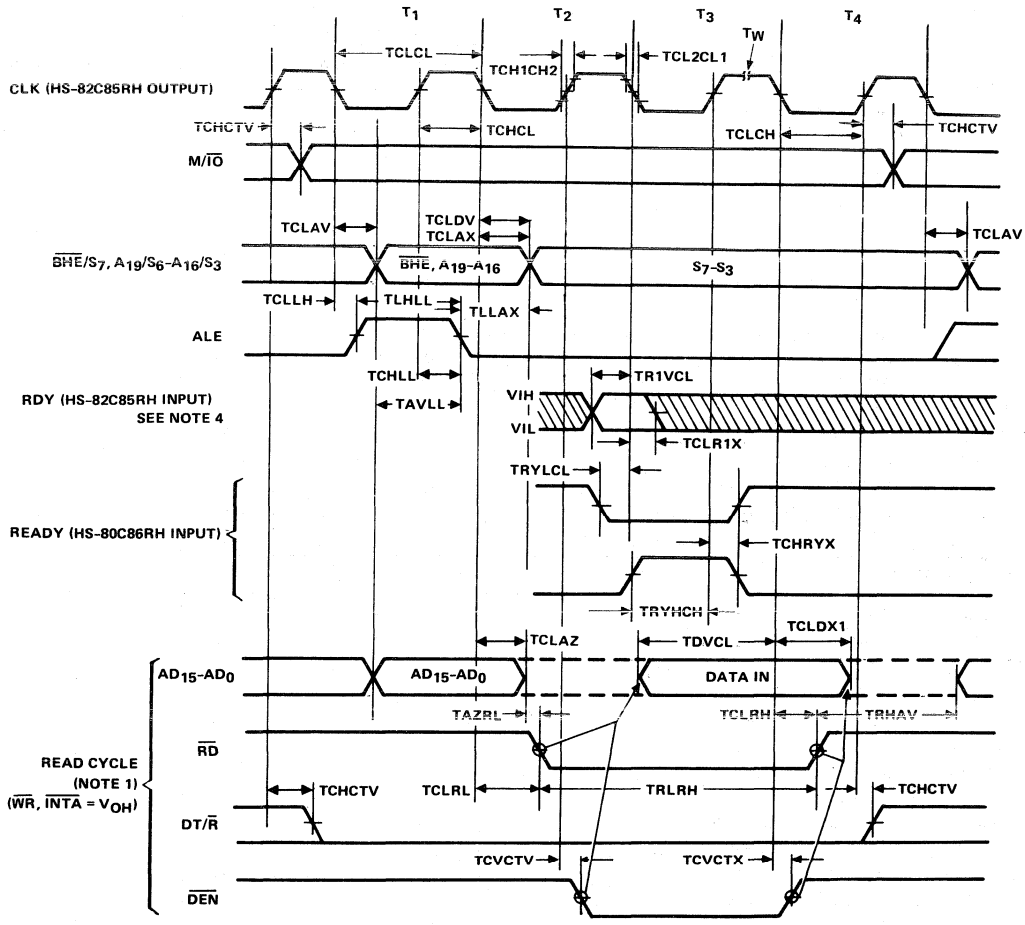
A.C. Electrical Specifications V_{DD} = 5.0V ± 10%; T_A = -55°C to +125°C

MINIMUM COMPLEXITY SYSTEM

SYMBOL	PARAMETER	HS-80C86RH MIN	HS-80C86RH MAX	UNITS	TEST CONDITIONS
TIMING REQUIREMENTS					
TCLCL	CLK Cycle Period	200		ns	
TCLCH	CLK Low Time	118		ns	
TCHCL	CLK High Time	69		ns	
TCH1CH2	CLK Rise Time **(Note 4)**		**15**	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time **(Note 4)**		**15**	ns	From 3.5V to 1.0V
TDVCL	Data In Setup Time	30		ns	
TCLDX1	Data In Hold Time	10		ns	
TR1VCL	RDY Setup Time into HS-82C85RH (Notes 1, 2)	35		ns	
TCLR1X	RDY Hold Time into HS-82C85RH (Notes 1, 2)	0		ns	
TRYHCH	READY Setup Time into HS-80C86RH	118		ns	
TCHRYX	READY Hold Time into HS-80C86RH	30		ns	
TRYLCL	READY Inactive to CLK (Note 3)	-8		ns	
THVCH	HOLD Setup Time	35		ns	
TINVCH	INTR, NMI, $\overline{TEST}$ Setup Time (Note 2)	30		ns	
TILIH	Input Rise Time (Except CLK) **(Note 4)**		**25**	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK) **(Note 4)**		**25**	ns	From 2.0V to 0.8V
TIMING RESPONSES					
TCLAV	Address Valid Delay	10	110	ns	CL = 100pF
TCLAX	Address Hold Time **(Note 4)**	10		ns	
TCLAZ	Address Float Delay **(Note 4, 5)**	TCLAX	80	ns	
TLHLL	ALE Width	TCLCH-20		ns	
TCLLH	ALE Active Delay		80	ns	
TCHLL	ALE Inactive Delay		85	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10		ns	
TCLDV	Data Valid Delay **(Note 4)**	10	110	ns	
TCLDX2	Data Hold Time **(Note 4)**	10		ns	
TWHDX	Data Hold Time After $\overline{WR}$ **(Note 4)**	TCLCL-30		ns	
TCVCTV	Control Active Delay 1	10	110	ns	
TCHCTV	Control Active Delay 2	10	110	ns	
TCVCTX	Control Inactive Delay	10	110	ns	
TAZRL	Address Float to READ Active **(Note 4, 5)**	0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-45		ns	
TCLHAV	HLDA Valid Delay	10	160	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL-75		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL-60		ns	
TAVLL	Address Valid to ALE Low	TCLCH-60		ns	
TOLOH	Output Rise Time		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		20	ns	From 2.0V to 0.8V

NOTES: 1. Signal at HS-82C85RH shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T_2 state (8ns into T_3).
4. Guaranteed but not tested.
5. Output drivers disabled. Bus hold circuitry still active.

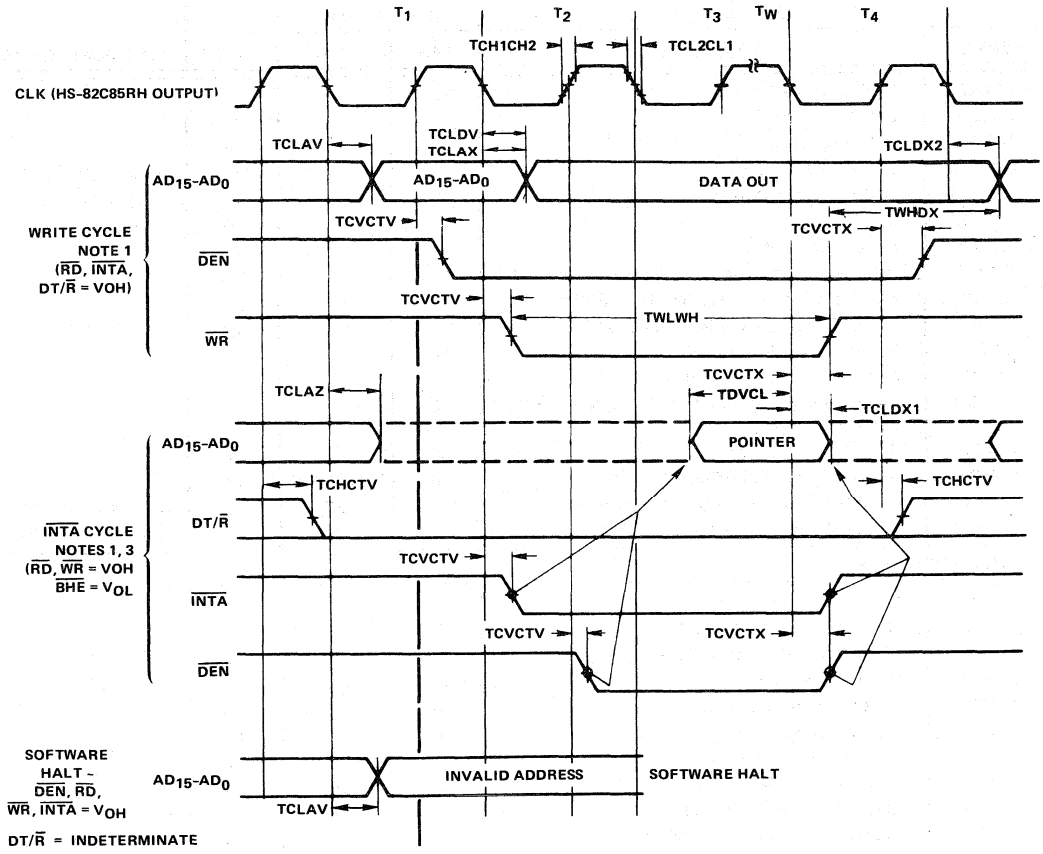
Waveforms



NOTES:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Two $\overline{INTA}$ cycles run back-to-back. The HS-80C86RH local ADDR/DATA bus is floating during both $\overline{INTA}$ cycles. Control signals are shown for the second $\overline{INTA}$ cycle.
4. Signals at HS-82C85RH are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

BUS TIMING - MINIMUM MODE SYSTEM

Waveforms



NOTES:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Two $\overline{INTA}$ cycles run back-to-back. The HS-80C86RH local ADDR/DATA bus is floating during both $\overline{INTA}$ cycles. Control signals are shown for the second $\overline{INTA}$ cycle.
4. Signals at HS-82C85RH are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

BUS TIMING - MINIMUM MODE SYSTEM

A.C. Electrical Specifications V_{DD} = 5.0V ± 10%; T_A = -55°C to +125°C

MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)

TIMING REQUIREMENTS		HS-80C86RH			
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TCLCL	CLK Cycle Period	200		ns	
TCLCH	CLK Low Time	118		ns	
TCHCL	CLK High Time	69		ns	
TCH1CH2	CLK Rise Time **(Note 6)**		15	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time **(Note 6)**		15	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		ns	
TCLDX1	Data In Hold Time	10		ns	
TR1VCL	RDY Setup Time into HS-82C85RH (Notes 1, 2)	35		ns	
TCLR1X	RDY Hold Time into HS-82C85RH (Notes 1, 2)	0		ns	
TRYHCH	READY Setup Time into HS-82C86RH	118		ns	
TCHRYX	READY Hold Time into HS-82C86RH	30		ns	
TRYLCL	READY Inactive to CLK (Note 3)	-8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) (Note 2)	30		ns	
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time	30		ns	
TCHGX	$\overline{RQ}$ Hold Time into HS-80C86RH (Note 4)	40	TCHCL + 10	ns	
TILIH	Input Rise Time (Except CLK) **(Note 6)**		25	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK) **(Note 6)**		25	ns	From 2.0V to 0.8V
TIMING RESPONSES					
TCLML	Command Active Delay (Note 1)	5	35	ns	
TCLMH	Command Inactive (Note 1)	5	35	ns	
TRYHSH	READY Active to Status Passive (Notes 3, 5)		110	ns	
TCHSV	Status Active Delay	10	110	ns	
TCLSH	Status Inactive Delay (Note 5)	10	130	ns	
TCLAV	Address Valid Delay	10	110	ns	
TCLAX	Address Hold Time **(Note 6)**	10		ns	
TCLAZ	Address Float Delay **(Note 6, 7)**	TCLAX	80	ns	CL = 100pF
TCHSZ	Status Float Delay **(Note 6, 7)**		80	ns	for all HS-80C86RH
TSVLH	Status Valid to ALE High (Note 1)		20	ns	Outputs (In addition
TSVMCH	Status Valid to MCE High (Note 1)		30	ns	to HS-80C86RH
TCLLH	CLK low to ALE Valid (Note 1)		20	ns	self-load
TCLMCH	CLK low to MCE High (Note 1)		25	ns	
TCHLL	ALE Inactive Delay (Note 1)	4	18	ns	
TCLMCL	MCE Inactive Delay (Note 1)		15	ns	
TCLDV	Data Valid Delay	10	110	ns	
TCLDX2	Data Hold Time **(Note 6)**	10		ns	
TCVNV	Control Active Delay (Note 1)	5	45	ns	
TCVNX	Control Inactive Delay (Note 1)	10	45	ns	
TAZRL	Address Float to Read Active **(Note 6, 7)**	0		ns	

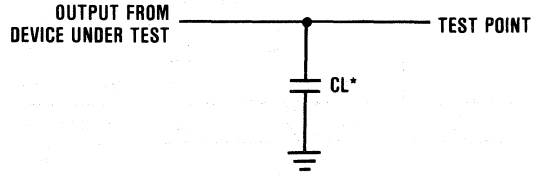
NOTES:
1. Signal at HS-82C85RH or 82C88 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T_2 state (8 nanoseconds into T_3).
4. The HS-80C86RH actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
5. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.
6. **Guaranteed but not tested.**
7. **Output drivers disabled. Bus hold circuitry still active.**

A.C. Electrical Specifications V_{DD} = 5.0V ± 10%; T_A = -55°C to +125°C

TIMING REQUIREMENTS (Continued)		HS-80C86RH			
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TCLRL	$\overline{RD}$ Active Delay	10	165	ns	CL = 100pF
TCLRH	$\overline{RD}$ Inactive Delay	10	150	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-45		ns	
TCHDTL	Direction Control Active Delay (Note 1)		50	ns	
TCHDTH	Direction Control Inactive Delay (Note 1)		30	ns	
TCLGL	$\overline{GT}$ Active Delay	0	85	ns	
TCLGH	$\overline{GT}$ Inactive Delay	0	85	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL-75		ns	
TOLOH	Output Rise Time		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15	ns	From 2.0V to 0.8V

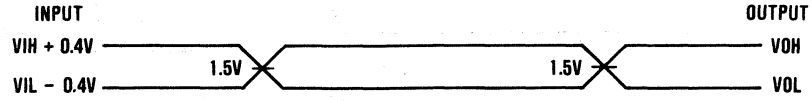
NOTES:
1. Signal at HS-82C85RH or 82C88 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T_2 state (8 nanoseconds into T_3).
4. The HS-80C86RH actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
5. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

A. C. Test Circuits



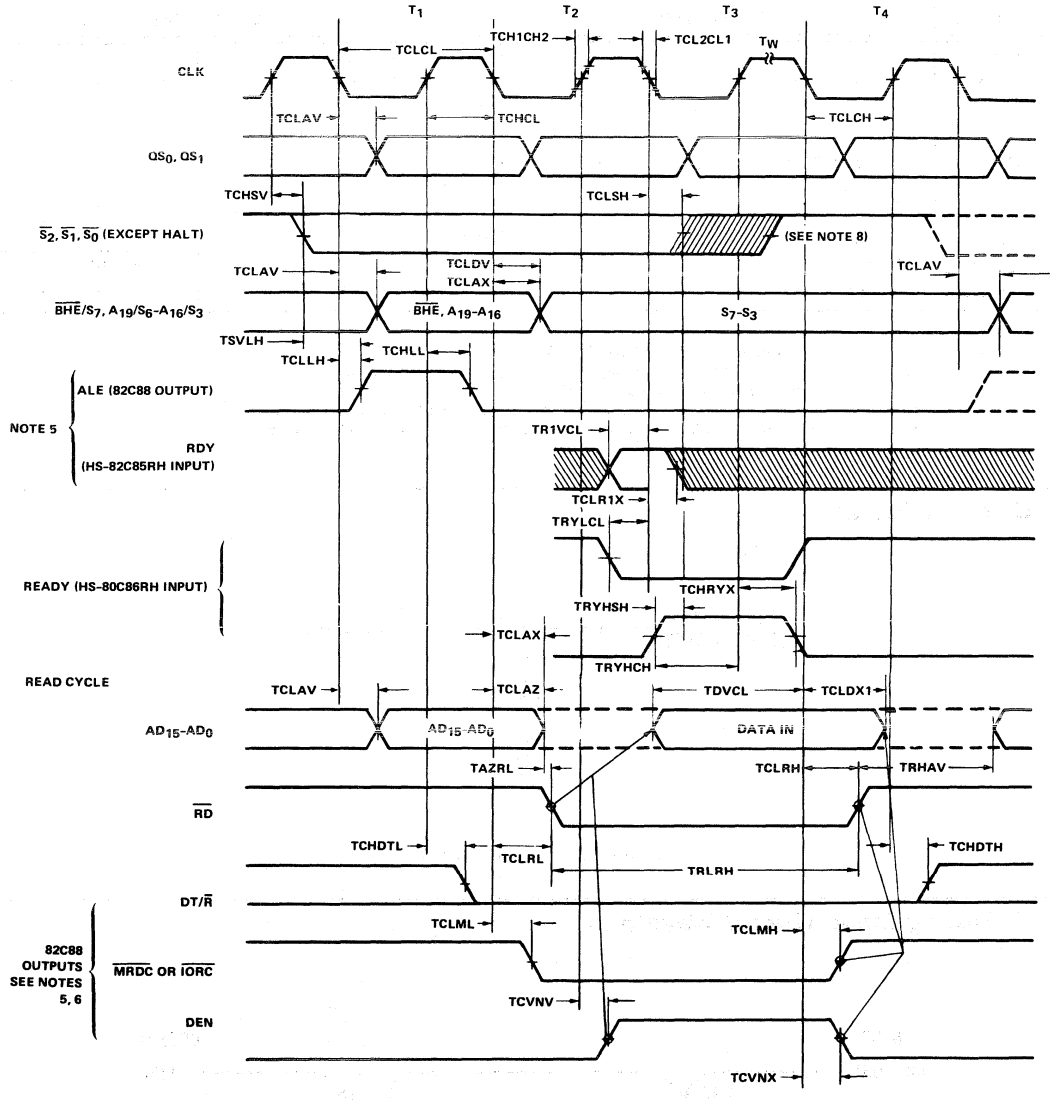
*Includes stray and jig capacitance.

A. C. Testing Input, Output Waveform



A. C. Testing: All inputs signals (other than CLK) must switch between VIL_{max} -0.4V and VIH_{min} +0.4V. CLK must switch between 0.4V and 3.9V. T_R and T_F must be less than or equal to 15ns. CLK T_R and T_F must be less than or equal to 10ns.

Waveforms

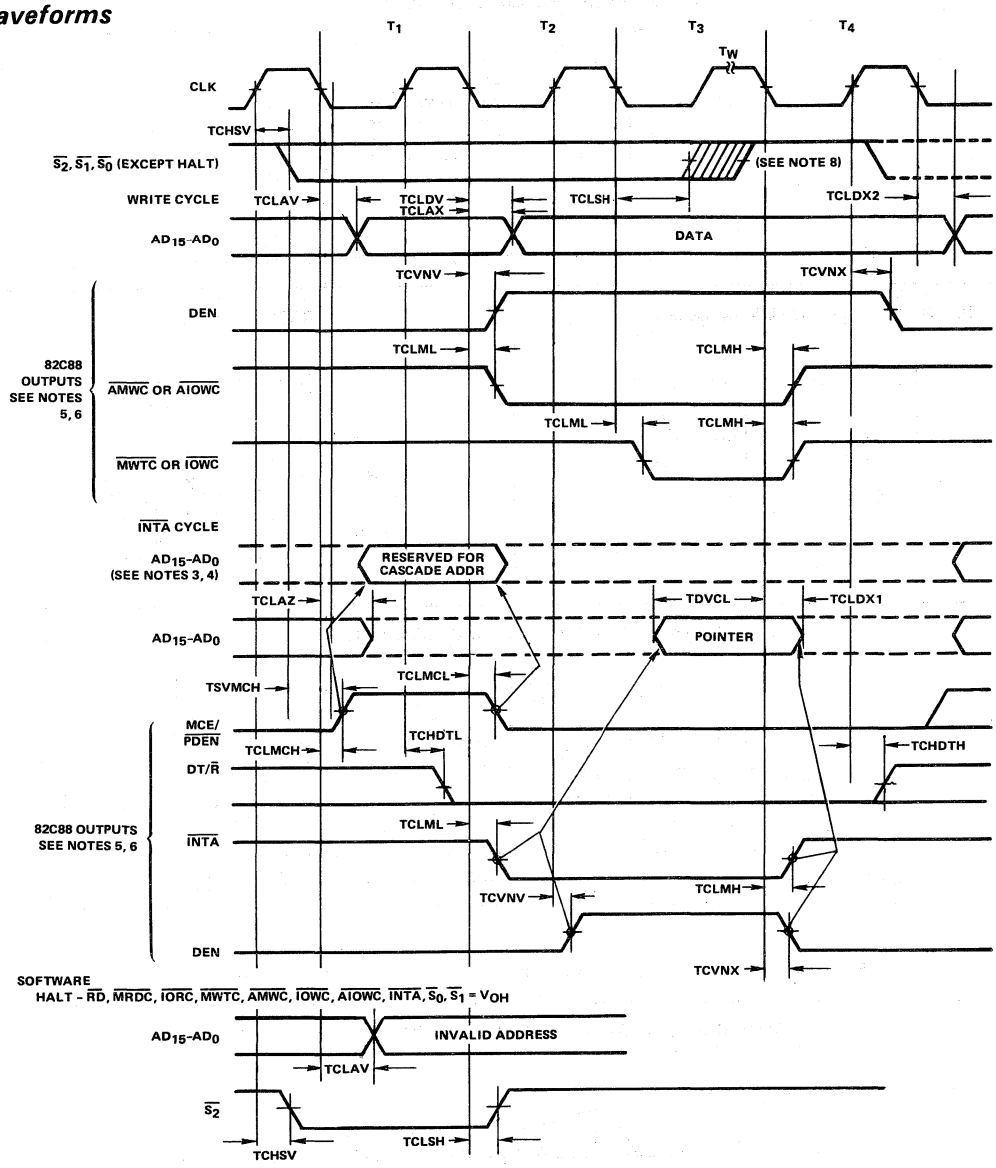


BUS TIMING - MAXIMUM MODE SYSTEM

NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second $\overline{INTA}$ cycle.
4. Two $\overline{INTA}$ cycles run back-to-back. The HS-80C86RH LOCAL ADDR/DATA BUS is floating during both $\overline{INTA}$ cycles. Control for pointer address is shown for second $\overline{INTA}$ cycle.
5. Signals at HS-82C85RH or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and DEN) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T_4.

Waveforms



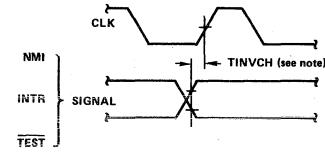
BUS TIMING-MAXIMUM MODE SYSTEM (USING 82C88)

NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second $\overline{INTA}$ cycle.
4. Two $\overline{INTA}$ cycles run back-to-back. The HS-80C86RH LOCAL ADDR/DATA BUS is floating during both $\overline{INTA}$ cycles. Control for pointer address is shown for second $\overline{INTA}$ cycle.
5. Signals at HS-82C85RH or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and DEN) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T_4.

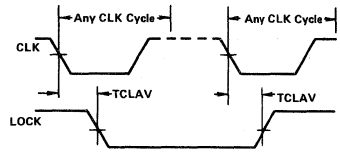
Waveforms

ASYNCHRONOUS SIGNAL RECOGNITION

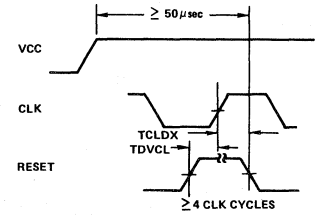


NOTE: Setup Requirements for asynchronous signals only to guarantee recognition at next CLK.

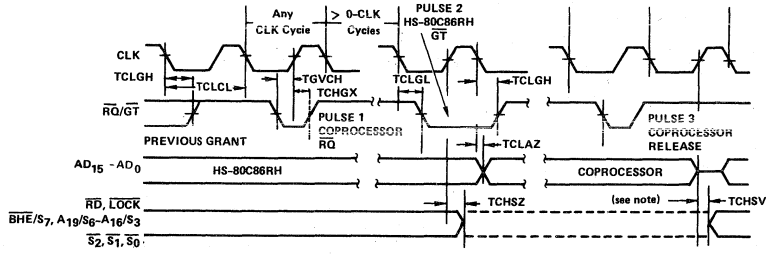
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



RESET TIMING

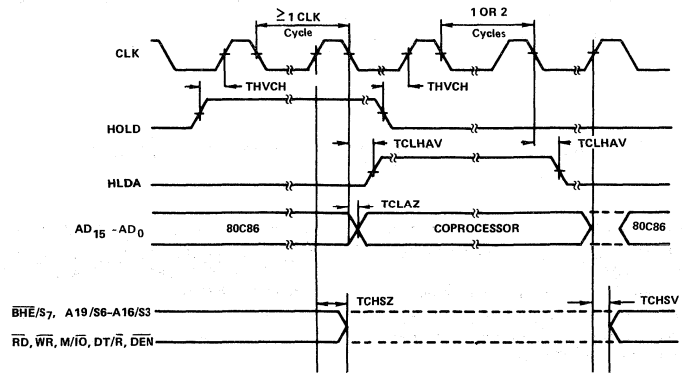


REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



NOTE: The coprocessor may not drive the busses outside the region shown without risking contention.

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



Instruction Set Summary

DATA TRANSFER

MOV = Move:	76543210	76543210	76543210	76543210
Register/memory to/from register	100010dw	mod reg r/m		
Immediate to register/memory	1100011w	mod000 r/m	data	data if w 1
Immediate to register	1011w reg	data	data if w 1	
Memory to accumulator	1010000w	addr low	addr-high	
Accumulator to memory	1010001w	addr-low	addr-high	
Register/memory to segment register	10001110	mod0reg r/m		
Segment register to register/memory	10001100	mod0reg r/m		

PUSH = Push:		
Register/memory	11111111	mod110 r/m
Register	01010 reg	
Segment register	000reg110	

POP = Pop:		
Register/memory	10001111	mod000 r/m
Register	01011 reg	
Segment register	000reg111	

XCHG = Exchange:		
Register/memory with register	1000011w	mod reg r/m
Register with accumulator	10010 reg	

IN=Input from:		
Fixed port	1110010w	port
Variable port	1110110w	

OUT = Output to:		
Fixed port	1110011w	port
Variable port	1110111w	
XLAT=Translate byte to AL	11010111	
LEA=Load EA to register	10001101	mod reg r/m
LDS=Load pointer to DS	11000101	mod reg r/m
LES=Load pointer to ES	11000100	mod reg r/m
LAHF=Load AH with flags	10011111	
SAHF=Store AH into flags	10011110	
PUSHF=Push flags	10011100	
POPF=Pop flags	10011101	

ARITHMETIC

ADD = Add:			
Reg./memory with register to either	000000dw	mod reg r/m	
Immediate to register/memory	100000sw	mod000 r/m	data	data if sw 01
Immediate to accumulator	0000010w	data	data if w 1	

ADC = Add with carry:			
Reg./memory with register to either	000100dw	mod reg r/m	
Immediate to register/memory	100000sw	mod010 r/m	data	data if sw 01
Immediate to accumulator	0001010w	data	data if w 1	

INC = Increment:		
Register/memory	1111111w	mod000 r/m
Register	01000 reg	
AAA=ASCII adjust for add	00110111	
DAA=Decimal adjust for add	00100111	

SUB = Subtract:			
Reg./memory and register to either	001010dw	mod reg r/m	
Immediate from register/memory	100000sw	mod101 r/m	data	data if sw 01
Immediate from accumulator	0010110w	data	data if w 1	

SBB = Subtract with borrow			
Reg./memory and register to either	000110dw	mod reg r/m	
Immediate from register/memory	100000sw	mod011 r/m	data	data if sw 01
Immediate from accumulator	0001110w	data	data if w 1	

DEC Decrement:	76543210	76543210	76543210	76543210
Register/memory	1111111w	mod001 r/m		
Register	01001 reg			
NEG Change sign	1111011w	mod011 r/m		

CMP Compare:				
Register/memory and register	001110dw	mod reg r/m		
Immediate with register/memory	100000sw	mod111 r/m	data	data if sw 01
Immediate with accumulator	0011110w	data	data if w 1	
AAS ASCII adjust for subtract	00111111			
DAS Decimal adjust for subtract	00101111			
MUL Multiply (unsigned)	1111011w	mod100 r/m		
IMUL Integer multiply (signed)	1111011w	mod101 r/m		
AAM ASCII adjust for multiply	11010100	00001010		
DIV Divide (unsigned)	1111011w	mod110 r/m		
IDIV Integer divide (signed)	1111011w	mod111 r/m		
AAD ASCII adjust for divide	11010101	00001010		
CBW Convert byte to word	10011000			
CWD Convert word to double word	10011001			

LOGIC

NOT Invert	1111011w	mod010 r/m
SHL/SAL Shift logical-arithmetic left	110100vw	mod100 r/m
SHR Shift logical right	110100vw	mod101 r/m
SAR Shift arithmetic right	110100vw	mod111 r/m
ROL Rotate left	110100vw	mod000 r/m
ROR Rotate right	110100vw	mod001 r/m
RCL Rotate through carry flag left	110100vw	mod010 r/m
RCR Rotate through carry right	110100vw	mod011 r/m

AND And:				
Reg./memory and register to either	001000dw	mod reg r/m		
Immediate to register/memory	1000000w	mod100 r/m	data	data if w 1
Immediate to accumulator	0010010w	data	data if w 1	

TEST And function to flags, no result:				
Register/memory and register	1000010w	mod reg r/m		
Immediate data and register/memory	1111011w	mod000 r/m	data	data if w 1
Immediate data and accumulator	1010100w	data	data if w 1	

OR Or:				
Reg./memory and register to either	000010dw	mod reg r/m		
Immediate to register/memory	1000000w	mod001 r/m	data	data if w 1
Immediate to accumulator	0000110w	data	data if w 1	

XOR Exclusive or:				
Reg./memory and register to either	001100dw	mod reg r/m		
Immediate to register/memory	1000000w	mod110 r/m	data	data if w 1
Immediate to accumulator	0011010w	data	data if w 1	

STRING MANIPULATION

REP=Repeat	1111001z
MOVS=Move byte/word	1010010w
CMPS=Compare byte/word	1010011w
SCAS=Scan byte/word	1010111w
LODS=Load byte/wd to AL/AX	1010110w
STOS=Stor byte/wd from AL/A	1010101w

Mnemonics ©Intel, 1978

Instruction Set Summary

CONTROL TRANSFER

CALL = Call:	76543210	76543210	76543210
Direct within segment	11101000	disp-low	disp-high
Indirect within segment	11111111	mod 010 r/m	
Direct intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 011 r/m	

JMP = Unconditional Jump:			
Direct within segment	11101001	disp-low	disp-high
Direct within segment-short	11101011	disp	
Indirect within segment	11111111	mod 100 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 101 r/m	

RET = Return from CALL:			
Within segment	11000011		
Within seg adding immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment adding immediate to SP	11001010	data-low	data-high

	76543210	
JE/JZ=Jump on equal/zero	01110100	disp
JL/JNGE=Jump on less/not greater or equal	01111100	disp
JLE/JNG=Jump on less or equal/not greater	01111110	disp
JB/JNAE=Jump on below/not above or equal	01110010	disp
JBE/JNA=Jump on below or equal/not above	01110110	disp
JP/JPE=Jump on parity/parity even	01111010	disp
JO=Jump on overflow	01110000	disp
JS=Jump on sign	01111000	disp
JNE/JNZ=Jump on not equal/not zero	01110101	disp
JNL/JGE=Jump on not less/greater or equal	01111101	disp
JNLE/JG=Jump on not less or equal/greater	01111111	disp

	76543210	
JNB/JAE Jump on not below/above or equal	01110011	disp
JNBE/JA Jump on not below or equal/above	01110111	disp
JNP/JPO=Jump on not par/par odd	01111011	disp
JNO Jump on not overflow	01110001	disp
JNS Jump on not sign	01111001	disp
LOOP Loop CX times	11100010	disp
LOOPZ/LOOPE Loop while zero/equal	11100001	disp
LOOPNZ/LOOPNE Loop while not zero/equal	11100000	disp
JCXZ Jump on CX zero	11100011	disp

INT Interrupt		
Type specified	11001101	type
Type 3	11001100	
INTO Interrupt on overflow	11001110	
IRET Interrupt return	11001111	

PROCESSOR CONTROL

CLC Clear carry	11111000	
CMC Complement carry	11110101	
STC Set carry	11111001	
CLD Clear direction	11111100	
STD Set direction	11111101	
CLI Clear interrupt	11111010	
STI Set interrupt	11111011	
HLT Halt	11110100	
WAIT Wait	10011011	
ESC Escape (to external device)	11011xxx	mod x x x r/m
LOCK Bus lock prefix	11110000	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL).
x = don't care
z is used for string primitives for comparison with Z-F FLAG.

SEGMENT OVERRIDE PREFIX

001 reg 110

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = +5V. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The sample devices shall be tested within one hour after irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.

Radiation Effects

1. TOTAL DOSE:

   No degradation of any parameter will be seen at 1 x 10^5 Rad(Si). Minimal (10%) increases in static supply current due to leakages will begin to appear between 1 x 10^5 Rad(Si) and 5 x 10^5 Rad(Si), increasing to 50% after exposure to 1 x 10^6 Rad(Si), although the device will remain functional within specifications.

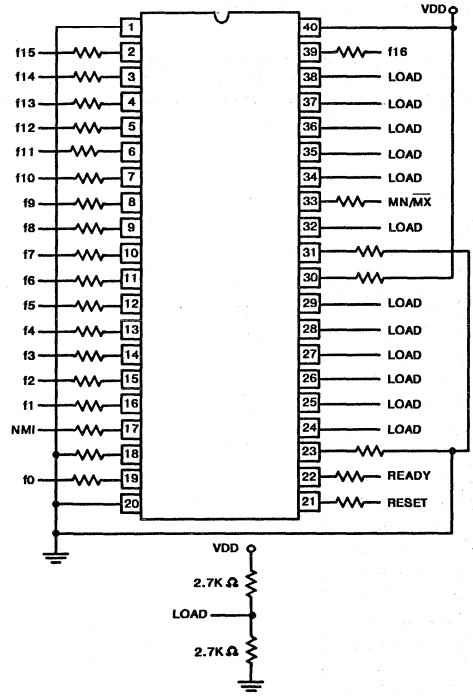
2. DOSE RATE:

   The HS-80C86RH is manufactured on EPI material and is consequently latch-up free. Transient upset can be expected at dose rates higher than 1 x 10^8 Rad(Si)/sec.

3. SINGLE EVENT UPSET:

   The HS-80C86RH is manufactured on EPI material and is consequently latch-up free. LET threshold has not yet been determined.

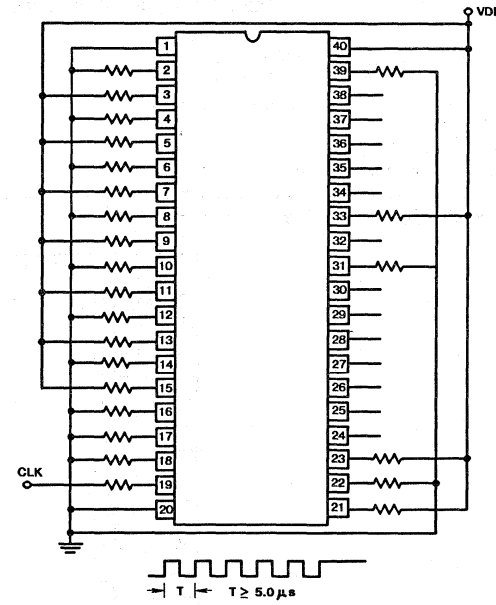
Burn-In Circuits



DYNAMIC CONFIGURATION

VDD = 6.0V ± 5% (Burn-In)
VDD = 5.5V ± 5% (Life Test)
TA = 125°C
Package: 40 Pin DIP
Part is Static Sensitive
Voltage Must Be Ramped

Resistors:
10kΩ (Pins 17, 18, 21, 22, 23, 33)
3.3kΩ (Pins 2-16, 19, 30, 31, 39)
2.7kΩ Loads As Indicated
All Resistors Are At Least 1/8W, ± 10%
F0 = 100kHz, F1 = F0/2, F2 = F1/2 . . .
RESET, NMI low after initialization.
READY pulsed low every 320µs
MN/$\overline{MX}$ changes state every 5.24 sec.



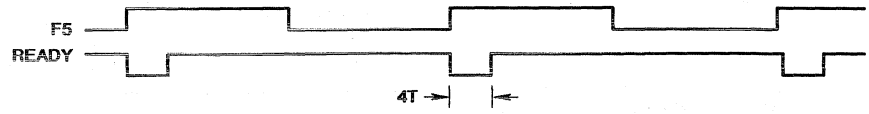
STATIC CONFIGURATION

VDD = +6.0V ± 10%
TA = 125°C Minimum
Part is Static Sensitive
Voltages Must Be Ramped
Package: 40 Pin DIP

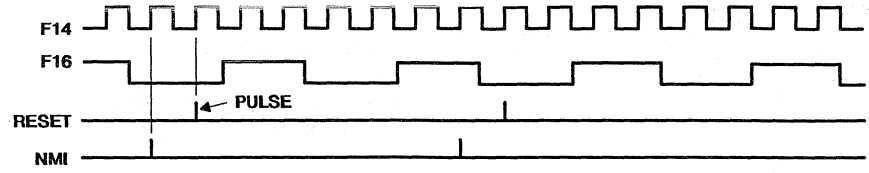
Resistors:
10kΩ ± 10%
(Pins 17, 18, 21-23, 31, 33)
2.7kΩ ± 5% (Pins 2-16, 39)
1.0kΩ ± 5% 1/10W Min (Pin 19)
Minimum of 5 CLK Pulses
After Initial Pulses, CLK is Left High
Pulses are 50% duty cycle square wave

Burn-In Circuits (Continued)

TIMING DIAGRAMS



READY TIMING AS COMPARED TO F5



RESET, NMI, AND MN/MX TIMING AS COMPARED TO F14 AND F16

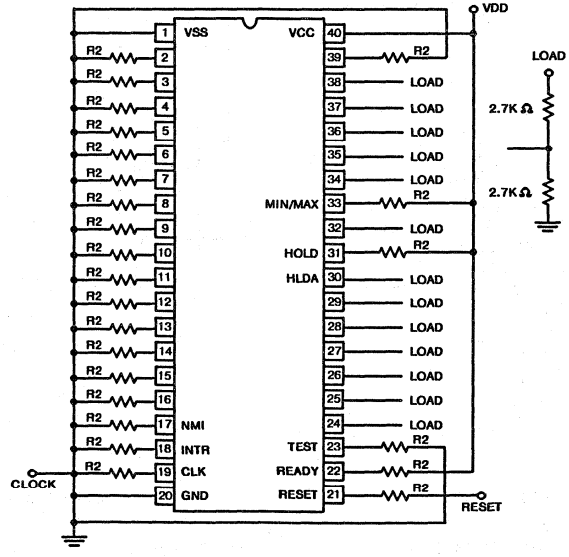
F0 = 100kHz, 50% duty cycle square wave.
F1 = F0/2, F2 = F1/2 . . . F16 = F15/2.

READY, RESET, and NMI timing are as shown below:
T = 10μsec.

All signals have rise/fall time limits:
100ns < t-rise, t-fall < 500ns

- RESET has a pulse width = 8T and occurs every two cycles of F16.
- NMI has a pulse width = 4T and occurs every two cycles of F16.
- MN/MX is a 50% duty cycle square wave and changes every eight cycles of F16.

Irradiation Circuit



R2 = 3.3kΩ, R3 = 47kΩ
Pins Tied to Gnd: 1-18, 20, 23, 39
Pins Tied to VCC: 22, 31, 33, 40
Pins With Loads: 24-29, 30, 32, 34-38
Pins Brought Out: 19 (Clock), 21 (Reset)

Clock and reset should be brought out separately so they can be toggled before irradiation.

RAD-HARD 9

MICROPROCESSOR PERIPHERALS

HARRIS

HS-3374RH

Radiation Hardened 8-Bit Bidirectional CMOS/TTL Level Converter

July 1990

Features

- Radiation Hardened EPI-CMOS
  - Total Dose ..... 1×10^5 RAD(Si)
  - Latch-Up Immune ..... $> 1 \times 10^{12}$ RAD(Si)/s*
- Low Propagation Delay Time
  - Typical CMOS to TTL Pre-Rad 30ns
  - Typical CMOS to TTL Post 100K RADs 30ns
  - Typical TTL to CMOS Pre-Rad 35ns
  - Typical TTL to CMOS Post 100K RADs 35ns
- Low Standby Power
- +10V CMOS and +5V TTL Power Supply Inputs
- Eight Non-inverting Three-State Input/Output Channels
- No External TTL Input Pull-Up Resistors Required
- High TTL Sink Current
- Equivalent to Sandia SA2996
- Military Temperature Range..... -55°C to +125°C

Description

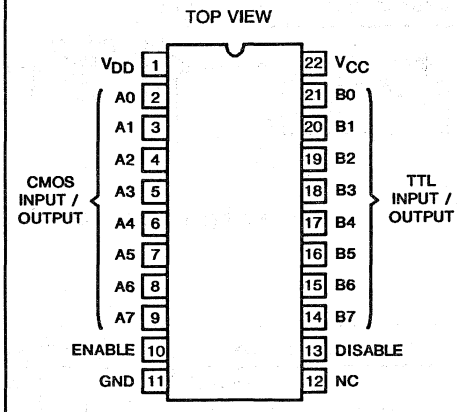
The Harris HS-3374RH is a radiation hardened 8-bit bidirectional level converter designed to interface CMOS logic levels with TTL logic levels in radiation hardened bus oriented systems. The HS-3374RH is fabricated using a radiation hardened EPI-CMOS process and features eight parallel bidirectional buffer/level converters.

Two control inputs, ENABLE and DISABLE, are used to determine the direction of data flow, and to set both the in puts and outputs in the high impedance state. The control inputs may be driven by either TTL or CMOS logic drivers capable of sinking one standard TTL load.

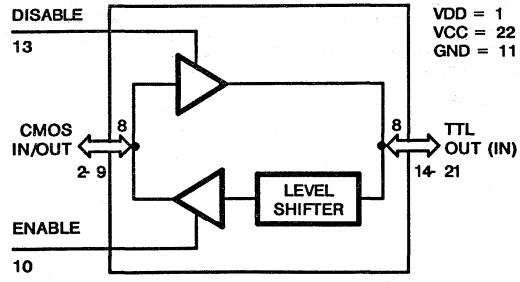
The HS-3374RH is a non-inverting version of the industry standard CD40116. The non-inverting outputs of the HS-3374RH reduce PC board chip count by eliminating the need to restore data back to a non-inverted format.

Pinout

TOP VIEW



Functional Diagram

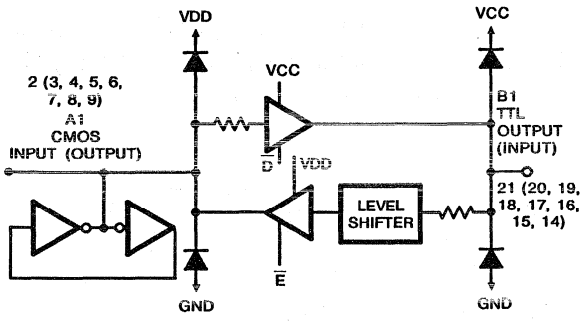


* For operation at 10 volts and transient levels above 1×10^{10} Rad(Si)/sec, please refer to Application Note 401.

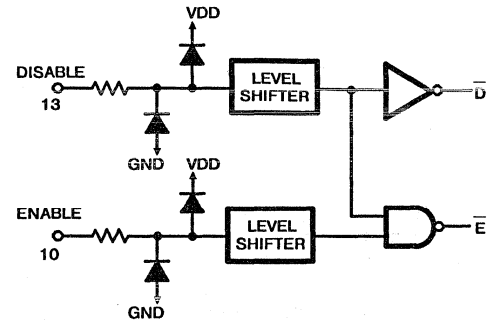
CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

9 MICROPROCESSOR PERIPHERALS

Functional Block Diagram



1 OF 8 IDENTICAL CIRCUITS



Enable and Disable are TTL Type Inputs

D and E Outputs are Common to All 8 Channels

INPUT (OUTPUT)		OUTPUT (INPUT)	
DATA	TERMINAL NUMBER	DATA	TERMINAL NUMBER
A0	2	B0	21
A1	3	B1	20
A2	4	B2	19
A3	5	B3	18
A4	6	B4	17
A5	7	B5	16
A6	8	B6	15
A7	9	B7	14

TRUTH TABLE

ENABLE	DISABLE	FUNCTION
X	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z)

0 = Low Level 1 = High Level X = Don't Care

Z = High Impedance on Both CMOS and TTL sides.

NOTE:

An important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule applies to inputs connected to a three-state bus. The need for external pull-up resistors during three-state bus conditions is eliminated by the presence of regenerative latches on the following HS-3374RH pins: A0-7. The functional block diagram depicts one of these pins with the regenerative latch. When the CMOS driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the three-state condition. A transient drive current of ±1.5mA at $V_{DD}/2$ ±0.5V for 10ns is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during three-state conditions.

WARNING: Do not activate the Disable input by hardwiring to any TTL input pins. This is an incorrect mode of operation.

Absolute Maximum Ratings

Supply Voltage (VDD to GND)..... +11.0V

Input or Output Voltage Applied..... (GND - 0.3V) to (VDD + 0.3V)

Storage Temperature.....-65°C to +150°C

Operating Range

Operating Supply Voltage VDD.....9.5V to 10.5V
VCC.....4.75V to 5.25V

Input Voltage Range
- Data Inputs, CMOS.....(GND - 0.3) to (V_{DD} + 0.3)
- Data Inputs, TTL.....(GND - 0.3) to (V_{CC} + 0.3)
- Enable, Disable Inputs.....(GND - 0.3) to (V_{DD} + 0.3)

Operating Temperature Range.....-55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications Notes (1), (2)

			TEMP & V_{DD} = OP. RANGE ±5%		TEMP = 25°C (3) V_{DD} = 10V, V_{CC} = 5V TYPICAL			
	SYMBOL	PARAMETER	MIN	MAX	PRE-RAD	POST-RAD	UNITS	TEST CONDITIONS (3)
DC	SIDD	Leakage Current		300	5	50	µA	Enable = 2.8V, Disable = 2.8V, Outputs Floating
				100	1	2	µA	Enable = 0.0V, Disable = 2.8V, Outputs Floating
	SICC	Leakage Current		5	1	1	µA	Enable = 0.0V, Disable = 2.8V, Outputs Floating
	ENABLE AND DISABLE INPUTS							
	IIH	Input Current High (CMOS)		1	0.1	0.1	µA	Floating Outputs
	TTL INPUTS TO CMOS OUTPUTS							
	IIL	Input Current Low	-1		-0.01	-0.01	µA	**VIL = 0.8V, Outputs Floating**
	IIH	Input Current High		1	0.01	0.01	µA	**VIH = 2.8V, Outputs Floating**
	VOL	Output Voltage Low		0.5	0.3	0.3	V	VIL = 0.8V, VIH = 2.8V, I_{SINK} = 2.0mA
	VOH	Output Voltage High	9.0		9.3	9.2	V	VIL = 0.8V, VIH = 2.8V, I_{SOURCE} = -2.0mA
	VIL	Input Voltage Low		0.8		0.8	V	
	VIH	Input Voltage High	2.8		2.8		V	
	CMOS INPUTS TO TTL OUTPUTS							
	VOL	Output Voltage Low		0.4	0.18	0.18	V	VIL = 1.0V, VIH = 10V, I_{SINK} = 11mA
	VOH	Output Voltage High	3.0		3.5	3.6	V	VIL = 1.0V, VIH = 10V, I_{SOURCE} = -2mA
	IOZ	High Z Leakage Current		±10	±1	±1	µA	VO = 0V or 2.8V, Enable = 0V, Disable = 2.8V
	VIL	Input Voltage Low		1.0		1.0	V	
	VIH	Input Voltage High	V_{DD} -1.0		V_{DD} -1.0		V	

	SYMBOL	PARAMETER	INPUT	OUTPUT	MAX	PRE-RAD TYPICAL	POST-RAD TYPICAL	UNITS	VDD	VCC	TEST CONDITIONS
AC	TPHLCT	Propagation Delay Times	CMOS	TTL	40	15	14	ns	9.5V	4.25V	V_{IL} = 1.0V, V_{IH} = 8.5V, C_L = 100pF
	TPLHCT	Data-In to Data-Out	"	"	50	20	17	ns	"	"	"
	TPHLTC	"	TTL	CMOS	85	45	35	ns	"	"	"
	TPLHTC	"	"	"	85	30	22	ns	"	"	"
	TPHZTC	Enable to CMOS Out	TTL	CMOS	90	65	56	ns	"	"	"
	TPZHTC	"	"	"	90	50	35	ns	"	"	"
	TPLZTC	"	"	"	90	65	60	ns	"	"	"
	TPZLTC	"	"	"	90	35	25	ns	"	"	"
	TPHZCT	Disable to TTL Out	CMOS	TTL	70	30	32	ns	"	"	"
	TPZHCT	"	"	"	130	55	40	ns	"	"	"
	TPLZCT	"	"	"	120	50	48	ns	"	"	"
	TPZLCT	"	"	"	125	55	40	ns	"	"	"
	TTHLCT	Transition Time	CMOS	TTL	20	10	10	ns	"	"	"
	TTLHCT	"	"	"	70	25	25	ns	"	"	"
	TTHLTC	"	TTL	CMOS	50	15	15	ns	"	"	"
	TTLHTC	"	"	"	50	10	10	ns	"	"	"

NOTES:
1. Pre-irradiation and Post-irradiation limits.
2. All devices guaranteed at worst case limits. Room temperature typical data provided for information and not guaranteed. Post radiation data at Total Dose = 1 x 10^5 Rad(Si).
3. V_{DD} = 10.5, V_{CC} = 5.25V.

Radiation Screening Procedure

1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad(Si) ±10% from a Gammacell 220 cobalt 60 source or equivalent. The samples shall be biased at V_{DD} and V_{CC} with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The lot will be accepted only if the sample, exclusive of non-radiation failures, meet the specified limits.

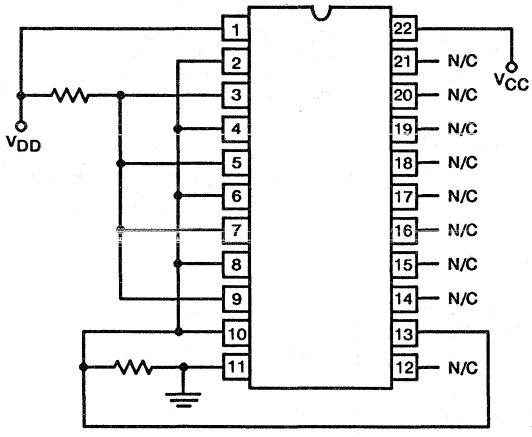
Radiation Effects

The HS-3374RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1×10^5 Rad(Si). Transient radiation tests have shown the following results:

- Latch-up free to doses $\geq 1 \times 10^{12}$ rads/sec*

*For operation at 10 volts and transient levels above 1×10^{10} Rad-Si/sec, please refer to Application Note 401.

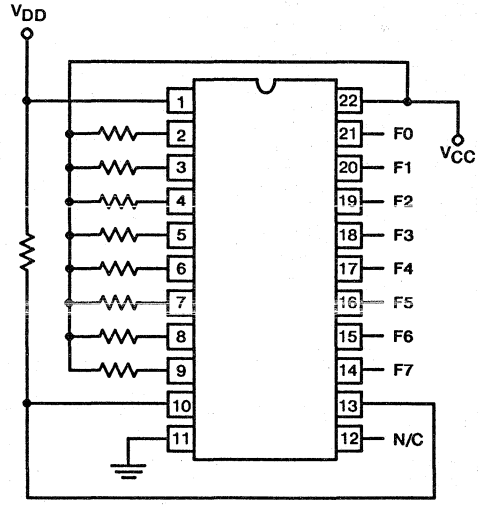
Burn-In Circuits



STATIC CONFIGURATION

Minimum Temperature +125°C
V_{CC} = 5.0V ±10%
V_{DD} = 10.0V ± 10%
All Resistors R1 = 10K 1/4 watt
Static Sensitive: All Voltages Must be Ramped
Crowbar Circuit: Yes

I_{CC} = 100µA
I_{DD} = 1mA

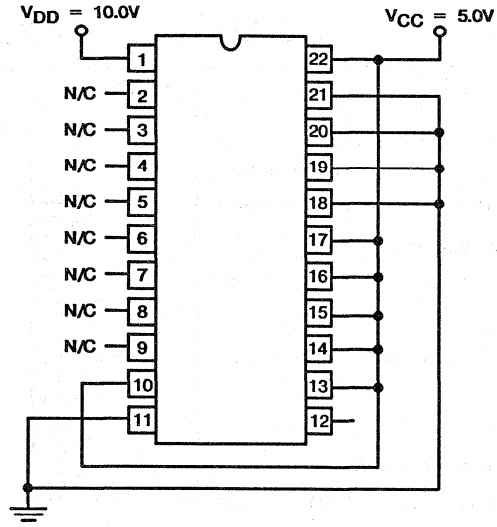


DYNAMIC CONFIGURATION

F0 = 1MHz, 50% Duty Cycle
F1 = F0/2, 50% Duty Cycle
F2 = F1/2, 50% Duty Cycle
F3 = F2/2, 50% Duty Cycle
F4 = F3/2, 50% Duty Cycle
F5 = F4/2, 50% Duty Cycle
F6 = F5/2, 50% Duty Cycle
F7 = F6/2, 50% Duty Cycle

V_{CC} = 5.0V ± 10%
V_{DD} = 10.0V ± 10%
Voltage Input High Max V_{DD}, Min V_{CC} - 1V
Voltage Input Low Max 1V, Min 0
Current Inputs: Sink 250µA
Source 250µA

Irradiation Circuit



HARRIS

HS-54C138RH

July 1990

Radiation Hardened 3-Line to 8-Line Decoder/Demultiplexer

Features

- Radiation Hardened
  - Total Dose ..... 1×10^5 RAD (Si)
  - Latch-up Immune EPI-CMOS ..... $>1 \times 10^{12}$ RAD(Si)
- Multiple Input Enable for Easy Expansion
- Single Power Supply ..... +5V
- Outputs Active Low
- Low Standby Power ..... (0.5mW Max @+5V)
- High Noise Immunity
- Equivalent to Sandia SA2995
- Bus Compatible with Harris Rad-Hard 80C85RH
- Full Military Temperature Range..... -55°C to +125°C

Description

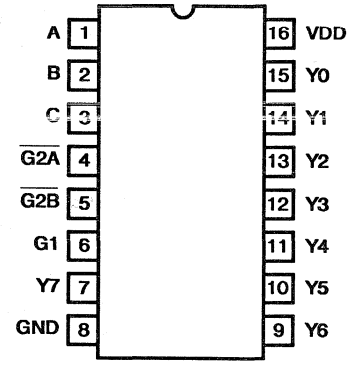
The Harris HS-54C138RH is a radiation hardened 3 to 8 decoder fabricated using a radiation hardened EPI-CMOS process. It features low power consumption, high noise immunity, and high speed. Also featured are pin and function compatibility with the 54LS138 industry standard part. The HS-54C138RH is ideally suited for high speed memory chip select address decoding. It is intended for use with the Harris HS-80C85RH radiation hardened microprocessor, but it can also be utilized as a demultiplexer in any low power rad-hard application.

The HS-54C138RH contains a one of eight binary decoder. A three bit binary input is used to select and activate each of the eight outputs, provided the three chip enable inputs are also present (see truth table).

The HS-54C138RH has an on-chip enable gate. The active high (G1) and both active low ($\overline{G2A}$, $\overline{G2B}$) inputs are Anded together to provide a single enable input to the device. See logic diagram on page 1. The use of both active high and active low inputs minimizes the need for external gates when expanding a system.

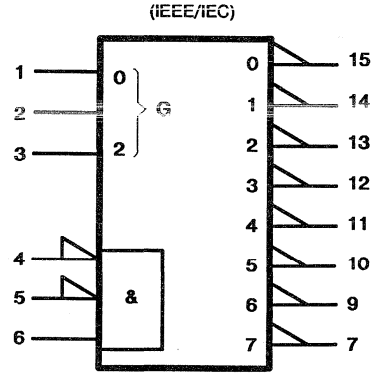
Pinout

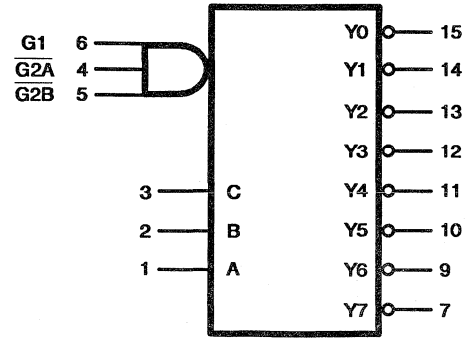
TOP VIEW



Logic Symbol

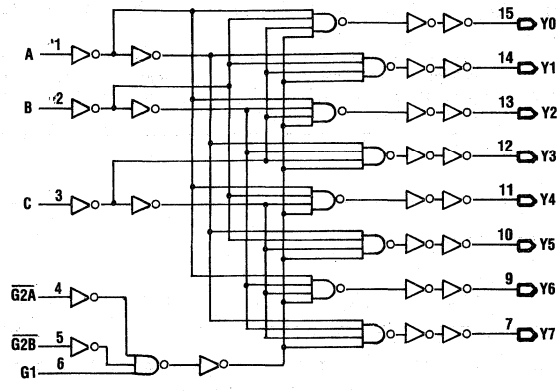
(IEEE/IEC)





CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Logic Diagram



Truth Table

SELECT			ENABLE			DATA OUTPUTS							
			G 2	G 2	G 1								
C	B	A	A	B		Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
H	H	L	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

H = High level
L = Low level
X = Don't care

Capacitance

SYMBOL	PARAMETER	MAX	UNITS
CIN*	Input Capacitance Select Input Pin Enable Input Pin	 6 6	 pF pF
COUT*	Output Capacitance Output Pin	 30	 pF

* Guaranteed but not tested.

Absolute Maximum Ratings

Supply Voltage (VDD to GND).....+7.0 Volts
Input or Output Voltage Applied ... (GND-0.3V)to(VDD+0.3V)
Storage Temperature Range .....-65°C to +150°C

Operating Range

Operating Supply Voltage..... +4.75V to +5.25V
Operating Temperature Range.....-55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications ②③

			Radiation,① Temp. & VDD = Operating Range 5V ± 5%		Temp = 25°C VDD = 5.0V Typical			
	SYMBOL	PARAMETER	MIN	MAX	PRE-RAD	POST RAD	UNITS	TEST CONDITIONS
D.C.	SIDD	Supply Current		100	1.0	1.0	uA	VDD = 5.25V, Vin = VDD or GND.
	VIH	Input High Voltage	VDD – 1.0				V	
	VIL	Input Low Voltage		1.0			V	
	VOH	Output High Voltage	4.25		4.5	4.5	V	VDD = 4.75V, Isource = –2mA, VIH = 3.75V, VIL = 1.0V
	VOL	Output Low Voltage		500	240	270	mV	VDD = 5.25V, Isink = 2mA, VIH = 4.25V, VIL = 1.0V
	IIH	Input Leakage Current		1	.003	.003	uA	VDD = 5.25V, Pin Under Test = VDD, Else VIN = 0V
	IIL	Input Leakage Current	–1		–.002	–.005	uA	VDD = 5.25V, Pin Under Test = 0V, Else VIN = VDD
A.C.		**SELECT TO OUTPUT PROPAGATION DELAY TIME**						
	TpLH(11)	Low to High Level Input Low to High Level Output		65	30	30	ns	VDD = 4.75V, VIL = 1.0V, VIH = 3.75V, CL = 100pF
	TpHL(11)	Low to High Level Input High to Low Level Output		90	50	50	ns	
	TpLH(12)	High to Low Level Input Low to High Level Output		75	35	50	ns	
	TpHL(12)	High to Low Level Input High to Low Level Output		90	50	55	ns	
		ENABLE TO OUTPUT PROPAGATION DELAY TIME						
	TpLH(21)	Low to High Level Input Low to High Level Output		70	35	45	ns	
	TpHL(21)	Low to High Level Input High to Low Level Output		105	55	50	ns	
	TpLH(22)	High to Low Level Input Low to High Level Output		70	35	45	ns	
	TpHL(22)	High to Low Level Input High to Low Level Output		105	55	50	ns	

NOTES ① All devices guaranteed at worst case limits. Room temperature typical data provided for information and not guaranteed. Post radiation data at Total Dose = 1×10^5 Rad(Si).
② Pre-irradiation and Post-irradiation limits.
③ Devices screened to more rigorous electrical specifications are available. Contact factory for details.

Radiation Screening Procedure

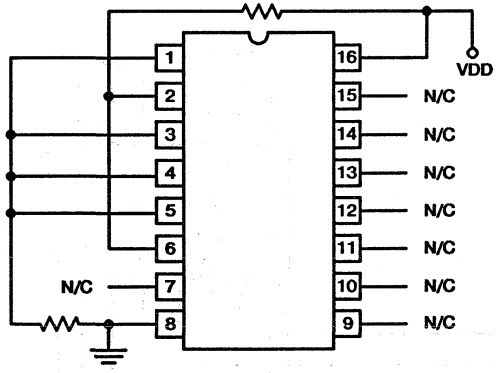
1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested to the customer's specification for proper operation.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad-Si (±10%) from a Gamma-cell 220 Cobalt 60 source or equivalent. The samples shall be biased at V_{DD} with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The lot will be accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact the factory for details.

Radiation Effects

The HS-54C138RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

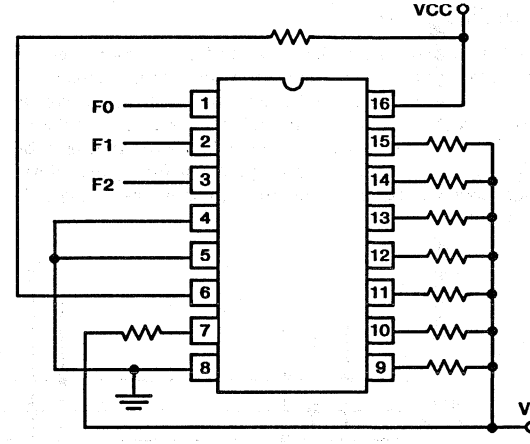
- Latch-up free to doses $\geq$ 1 x 10^{12} rads/sec.

Burn-In Circuits



STATIC CONFIGURATION

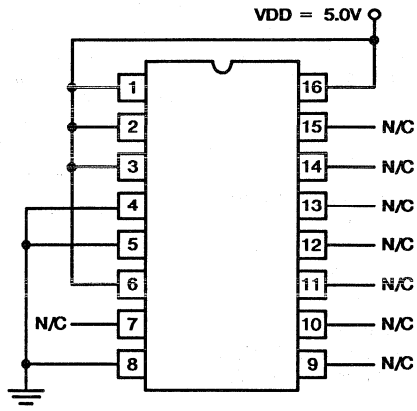
Minimum Temperature = +125°C, VDD = 10V ± 5%
All Resistors 10KΩ, 1/4 Watt



DYNAMIC CONFIGURATION

VCC = 5V ± 10%; VDD = 10V ± 5%, VS = 5V ± 10%
TA Min = +125°C; All Resistors Are 10kΩ ± 10%, 1/4 Watt,
F0 = 1MHz, 50% Duty Cycle,
F1 = F0/2
F2 = F1/2
Package: 16 Pin DIP; Package Code: SW. Part is Static Sensitive.
Voltages Must Be Ramped.

Irradiation Circuit



Applications

Typical applications include systems which require multiple input/output ports and memories. When the HS-54C138RH is enabled one of the eight outputs will go low. This output can be used to select a particular device or a group of devices. The HS-54C138RH can also be cascaded to provide an enabling scheme for larger systems and allow one decoder to control eight other decoders as in Figure 1.

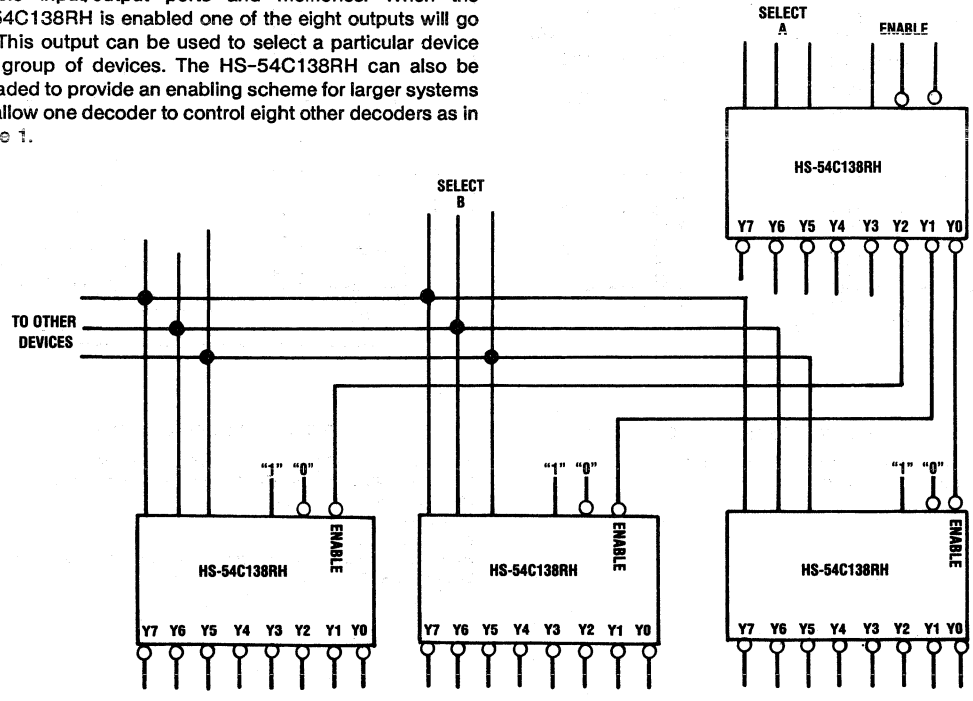


FIGURE 1

Applications (Continued)

Figure 2 shows a configuration that can be used to enable multiple I/O ports or memory devices. Up to 24 memory devices or I/O ports can be controlled using this circuit.

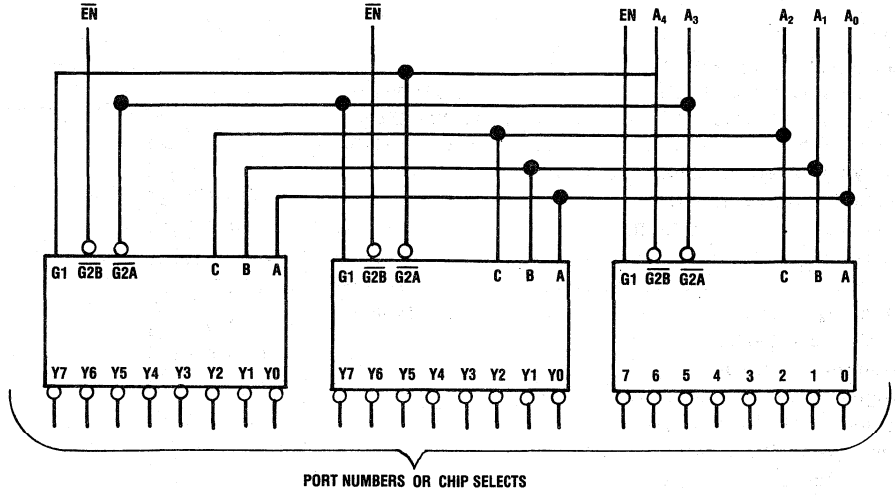


FIGURE 2

For demultiplexer operation, one of the three enable inputs is used as the data input while the other two inputs are enabled. The transmitted data is distributed to the proper output as determined by the 3-line select inputs. See Figure 3.

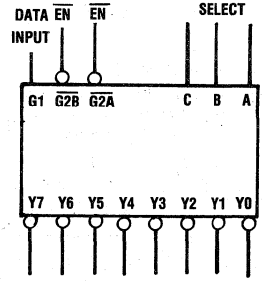


FIGURE 3

HARRIS HS-81C55/56RH

July 1990

Radiation Hardened 256 x 8 CMOS RAM

Features

- Radiation Hardened EPI-CMOS
  - Parametrics Guaranteed ..... 1 x 10^5 RAD(Si)
  - Transient Upset ..... > 1 x 10^8 RAD(Si)/s
  - Latch-Up Free ..... > 1 x 10^{12} RAD(Si)/s
- Electrically Equivalent to Sandia SA 3001
- Pin Compatible with Intel 8155/56
- Bus Compatible with HS-80C85RH
- Single 5 Volt Power Supply
- Low Standby Current ..... 100µA Max
- Low Operating Current 2mA/MHz
- Completely Static Design
- Internal Address Latches
- Two Programmable 8-Bit I/O Ports
- One Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Multiplexed Address and Data Bus
- Self Aligned Junction Isolated (SAJI) Process
- Military Temperature Range ..... -55°C to +125°C

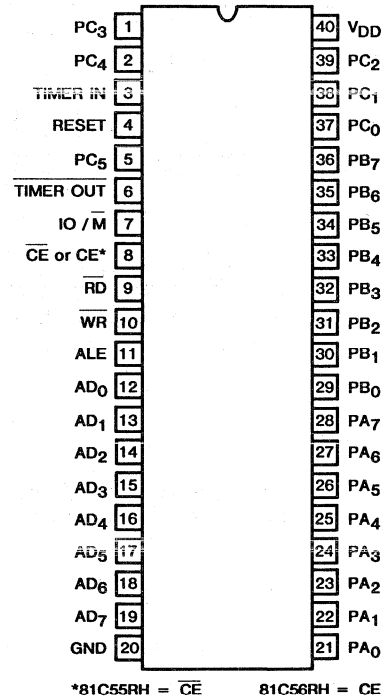
Description

The HS-81C55/56RH are radiation hardened RAM and I/O chips fabricated using the Harris radiation hardened Self-Aligned Junction Isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

The HS-81C55/56RH is intended for use with the HS80C85RH radiation hardened microprocessor system. The RAM portion is designed as 2048 static cells organized as 256 x 8. A maximum post irradiation access time of 500ns allows the HS-81C55/56RH to be used with the HS-80C85RH CPU without any wait states. The HS-81C55RH requires an active low chip enable while the HS-81C56RH requires an active high chip enable. These chips are designed for operation utilizing a single 5 volt power supply.

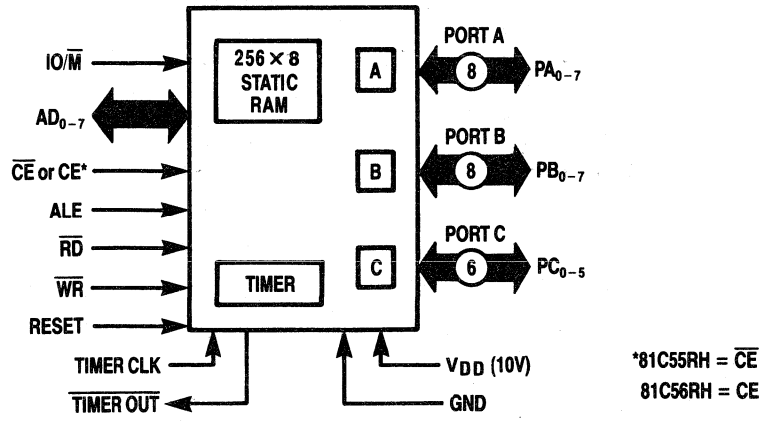
Pinout

TOP VIEW



*81C55RH = $\overline{CE}$ 81C56RH = CE

Block Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Table 1. Pin Description

Symbol	Type	Name and Function
RESET	I	**Reset:** Pulse provided by the HS-80C85RH to initialize the system (connect to HS-80C85RH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two HS-80C85RH clock cycle times.
AD_{0-7}	I/O	**Address/Data:** 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the HS-81C55/56RH on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$	I	**Chip Enable:** On the HS-81C55RH, this pin is $\overline{CE}$ and is ACTIVE LOW. On the HS-81C56RH, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$	I	**Read Control:** Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$	I	**Write Control:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{M}$.
ALE	I	**Address Latch Enable:** This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$	I	**I/O Memory:** Selects memory if low and I/O and command/status registers if high.
PA_{0-7}(8)	I/O	**Port A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7}(8)	I/O	**Port B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5}(6)	I/O	**Port C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — $\overline{ABF}$ (Port A Buffer Full) PC_2 — $\overline{A\ STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — $\overline{B\ BF}$ (Port B Buffer Full) PC_5 — $\overline{B\ STB}$ (Port B Strobe)
TIMER IN	I	**Timer Input:** Input to the counter-timer.
$\overline{TIMER\ OUT}$	O	**Timer Output:** This output can be either a square wave or a pulse, depending on the timer mode.
V_{DD}	I	**Voltage:** +5 volt
GND	I	**Ground:** Ground reference.

FUNCTIONAL DESCRIPTION

The HS-81C55RH/81C56RH contains the following:
- 2K Bit Static RAM organized as 256 × 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA_{0-7}, PB_{0-7}, PC_{0-5}) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{CE}$ and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

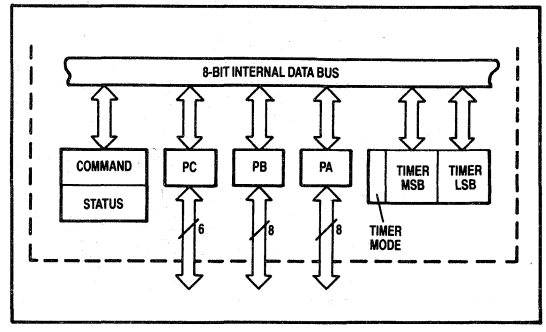


Figure 1. HS-81C55RH/81C56RH Internal Registers

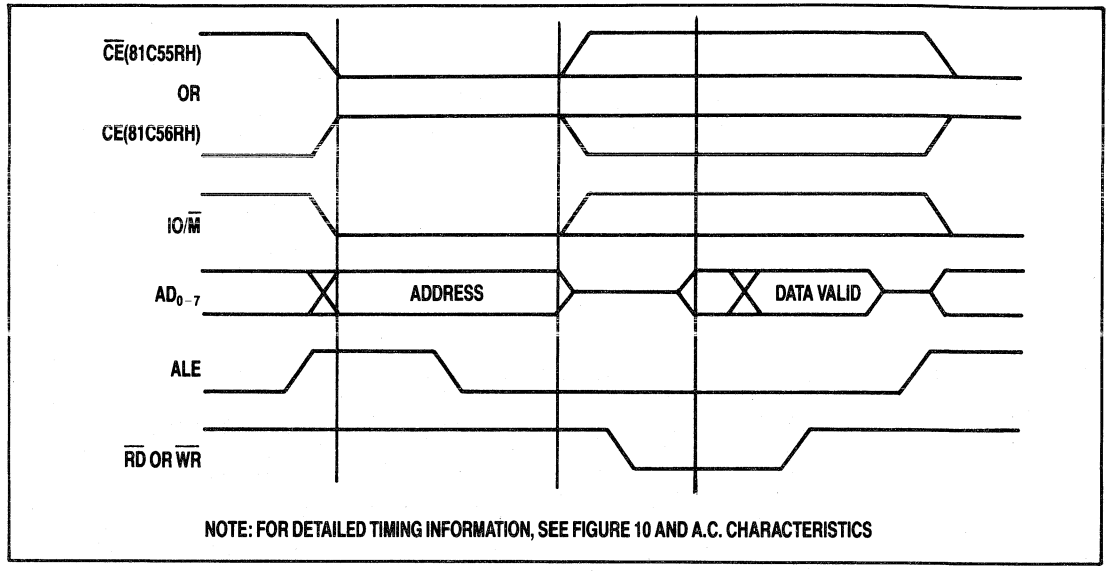


Figure 2. HS-81C55RH/81C56RH On-Board Memory Read/Write Cycle

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 3. The contents of the command register may never be read.

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 4. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

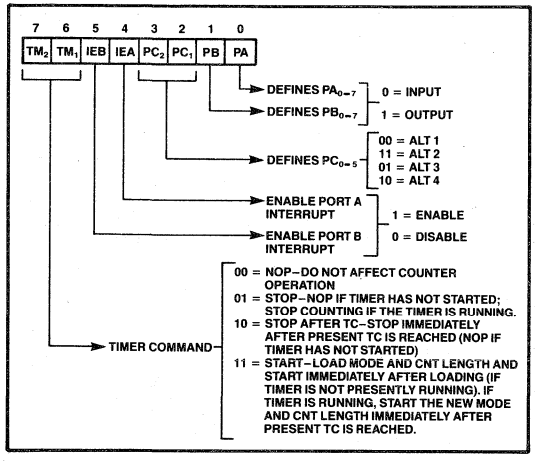


Figure 3. Command Register Bit Assignment

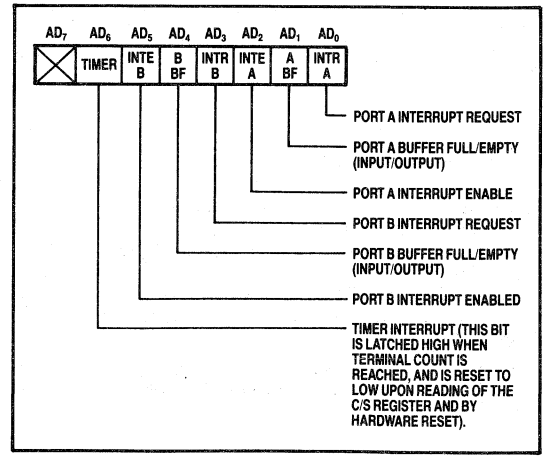


Figure 4. Status Register Bit Assignment

INPUT/OUTPUT SECTION

The I/O section of the HS-81C55/56RH consists of five registers: (See Figure 5)

- **Command/Status Register (C/S)** – Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD_{0-7} lines.

- **PA Register** – This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

- **PB Register** – This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.

- **PC Register** – This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

  When PC_{0-5} is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an Interrupt that the HS-81C55/56RH sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 2.)

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS †								
A7	A6	A5	A4	A3	A2	A1	A0	SELECTION
X	X	X	X	X	0	0	0	Interval Command/Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	Port C–General Purpose I/O or Control
X	X	X	X	X	1	0	0	Low-Order 8 bits of Timer Count
X	X	X	X	X	1	0	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X: Don't Care

†: I/O Address must be qualified by CE = 1(81C56RH) or $\overline{CE}$ = 0(81C55RH) and I/O $\overline{M}$ = 1 in order to select the appropriate register.

Figure 5. I/O Port and Timer Addressing Scheme

Figure 6 shows how I/O PORTS A and B are structured within the HS-81C55/56RH:

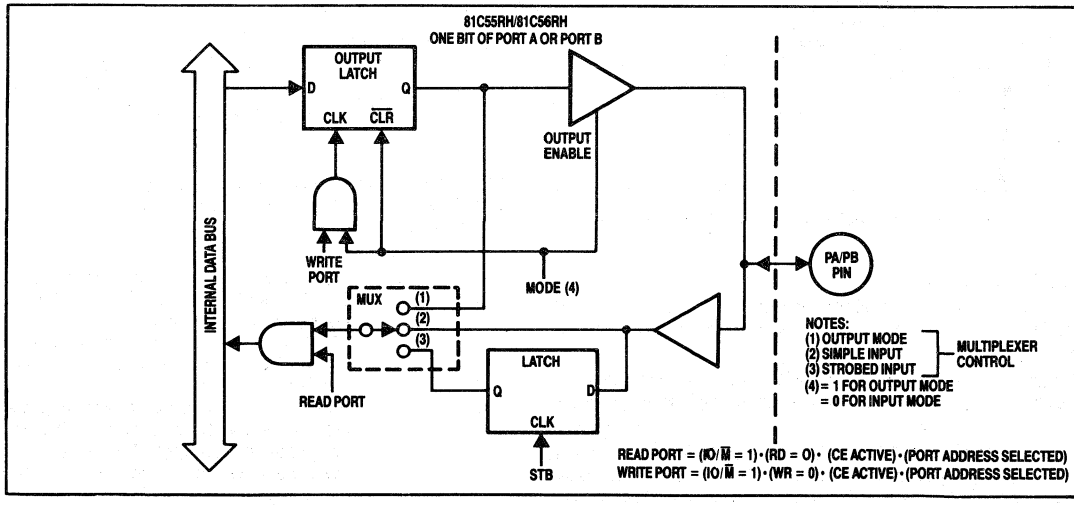


Figure 6. HS-81C55RH/81C56RH Port Functions

Table 2. Port Control Assignment

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A STB (Port A Strobe)	A STB (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B STB (Port B Strobe)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the HS-81C55/56RH are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the HS-81C55/56RH is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 7 shows how the HS-81C55/56RH I/O ports might be configured in a typical system.

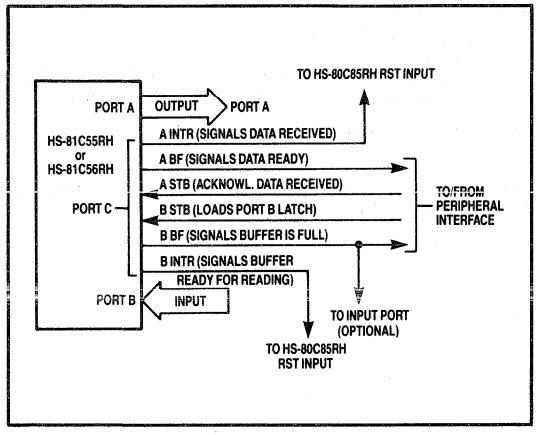


Figure 7. Example: Command Register = 00111001

TIMER SECTION

The timer is a 14-bit down counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 5).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 8). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0-13.

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 9.

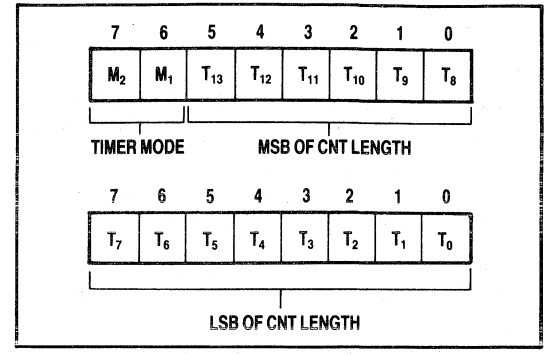


Figure 8. Timer Format

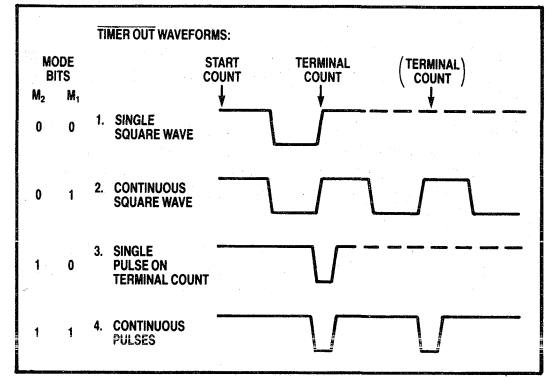


Figure 9. Timer Modes

Bits 6-7 (TM_2 and TM_1) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM_2	TM_1	
0	0	NOP – Do not affect counter operation.
0	1	STOP – NOP-if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC – Stop immediately after present TC is reached (NOP if timer has not started).
1	1	START – Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you *must* issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 10.

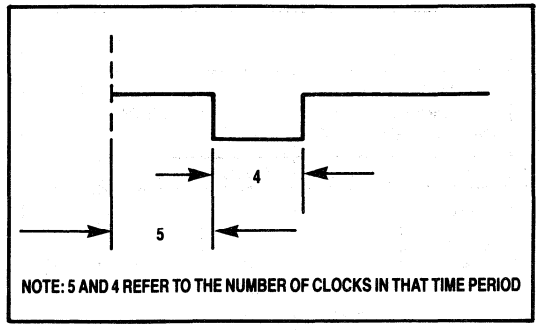


Figure 10. Asymmetrical Square-Wave Output Resulting from Count of 9

The counter in the HS-81C55/56RH is not initialized to any particular mode or count when hardware RESET occurs, but RESET does *stop* the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the HS-81C55/56RH chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the HS-80C85RH be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count −1 if full count is odd).

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the HS-81C55/56RH always counts out the right number of pulses in generating the TIMER OUT waveforms.

Absolute Maximum Ratings

Supply Voltage (VDD to GND) ..... +7.0V
Input or Output Voltage Applied ..... (GND - 0.3) to (V_{DD} + 0.3V)
Storage Temperature Range ..... -65°C to +150°C

Operating Range

Operating Supply Range ..... 4.75V to 5.25V
Operating Temperature Range ..... -55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications

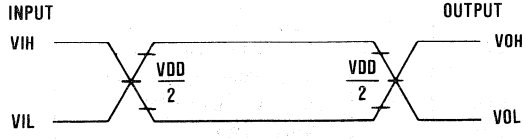
			(Notes 1, 4) RADIATION, TEMPERATURE AND V_{DD} = OP. RANGE			
	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
DC	V_{IL}	Input Low Voltage		0.5	V	V_{DD} = 4.75V
	V_{IH}	Input High Voltage	4.25		V	V_{DD} = 4.75V
	V_{OL}	Output Low Voltage		0.5	V	I_{OL} = 2mA, V_{DD} = 5.25V
	V_{OH}	Output High Voltage	4.25		V	I_{OH} = -2mA, V_{DD} = 4.75V
	I_I	Input Leakage		± 1.0	μA	V_{IN} = 0, V_{DD} = 5.25V
	I_{DDSB}	Standby Current		200	μA	V_{DD} = 5.25V
	I_{DDOP}	Operating Current Note 2		2	mA/MHz	V_{DD} = 5.25, f = 1MHz

Electrical Specifications

			RADIATION TEMPERATURE AND V_{DD} = OP. RANGE			NOTES
	SYMBOL	PARAMETER	MIN	MAX	UNITS	1,4
AC	t_{AL}	Address to Latch Setup Time	60		ns	
	t_{LA}	Address Hold Time After Latch	60		ns	
	t_{LC}	Latch to READ/WRITE Control	200		ns	
	t_{RD}	Valid Data Out Delay from READ Control		140	ns	
	t_{AD}	Address Stable to Data Out Valid		500	ns	
	t_{LL}	Latch Enable Width	160		ns	
	t_{RDF}	Data Bus Float After READ	0	80	ns	5
	t_{CL}	READ/WRITE Control to Latch Enable	10		ns	
	t_{CC}	READ/WRITE Control Width	200		ns	
	t_{DW}	Data In to WRITE Setup Time	200		ns	
	t_{WD}	Data In Hold Time After WRITE	25		ns	
	t_{RV}	Recovery Time Between Controls	220		ns	5
	t_{WP}	WRITE to Port Output		300	ns	
	t_{PR}	Port Input Setup Time	50		ns	
	t_{RP}	Port Input Hold Time	0		ns	
	t_{SBF}	Strobe to Buffer Full		300	ns	
	t_{SS}	Strobe Width	150		ns	
	t_{RBE}	READ to Buffer Empty		300	ns	
	t_{SI}	Strobe to INTR On		300	ns	
	t_{RDI}	READ to INTR Off		300	ns	
	t_{PSS}	Port Setup Time to Strobe	100		ns	6
	t_{PHS}	Port Hold Time After Strobe	100		ns	
	t_{SBE}	Strobe to Buffer Empty		300	ns	
	t_{WBF}	WRITE to Buffer Full		300	ns	
	t_{WI}	WRITE to INTR Off		300	ns	
	t_{TL}	TIMER-IN to TIMER-OUT Low		300	ns	
	t_{TH}	TIMER-IN to TIMER-OUT High		300	ns	
	t_{RDE}	Data Bus Enable from READ Control	120		ns	
	t_1	TIMER-IN Low Time	40		ns	
	t_2	TIMER-IN High Time	75		ns	

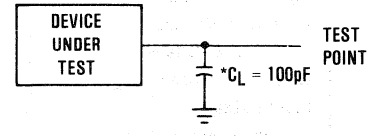
NOTES:
1. All devices guaranteed at worst case limits and over radiation.
2. Operating supply current (IDDOP) is proportional to operating frequency.
3. Output timings are measured with purely capacitive load.
4. For design purposes the limits are given as shown. For compatibility with the 80C85RH processor, the AC parameters are tested as maximums.
5. Parameter guaranteed by part design. Testing done only after a design change. No read and record data.
6. Parameter tested as part of the functional test. No read and record data available.

AC Testing Input, Output Waveform



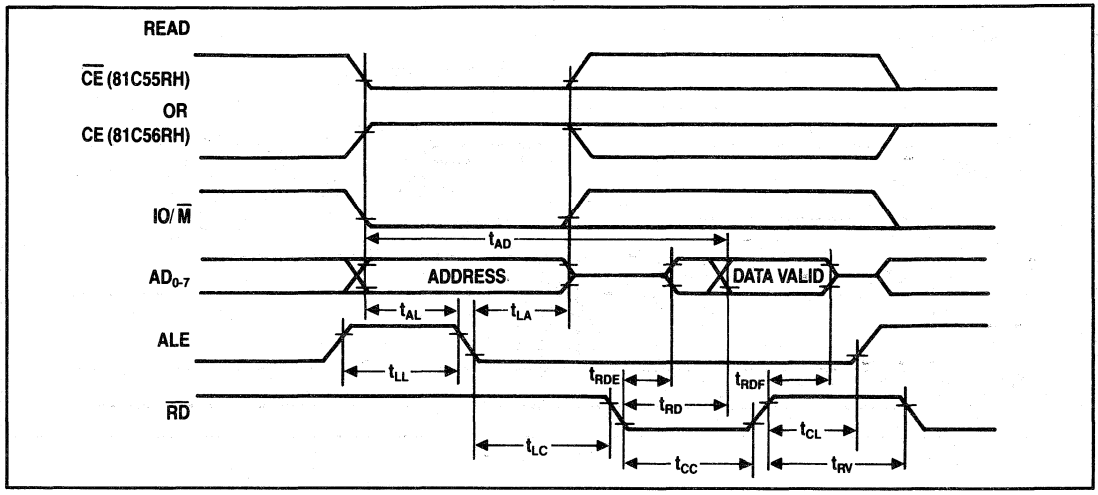
A.C. Testing: All input signals must switch between V_{IL} max and V_{IH} min, t_r and t_f must be less than or equal to 15ns.

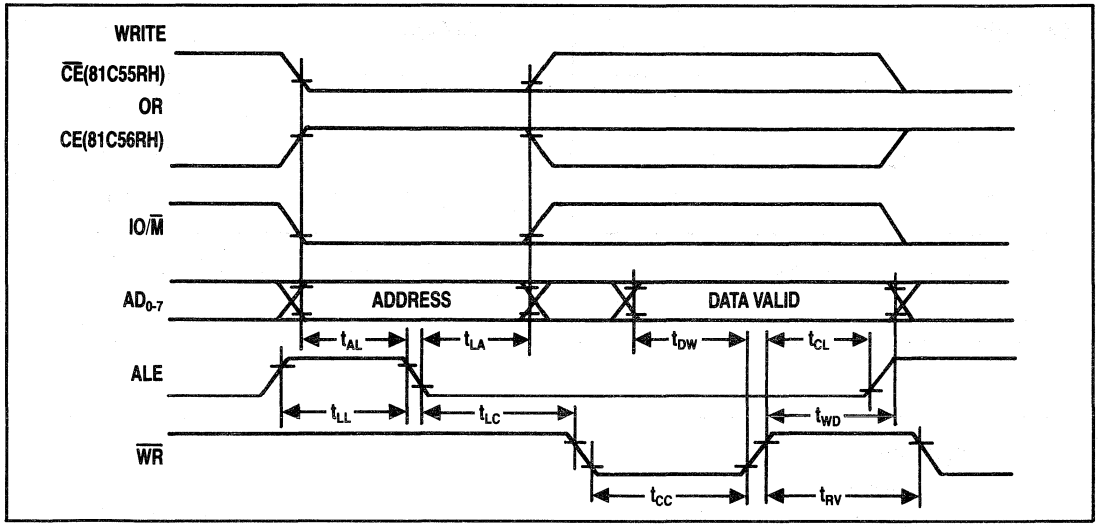
A.C. Testing Load Circuit (Note 3)

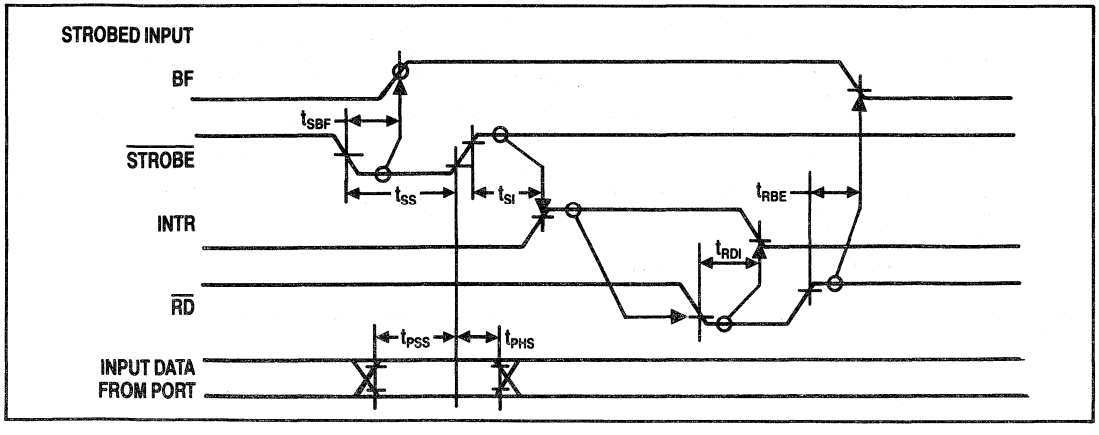


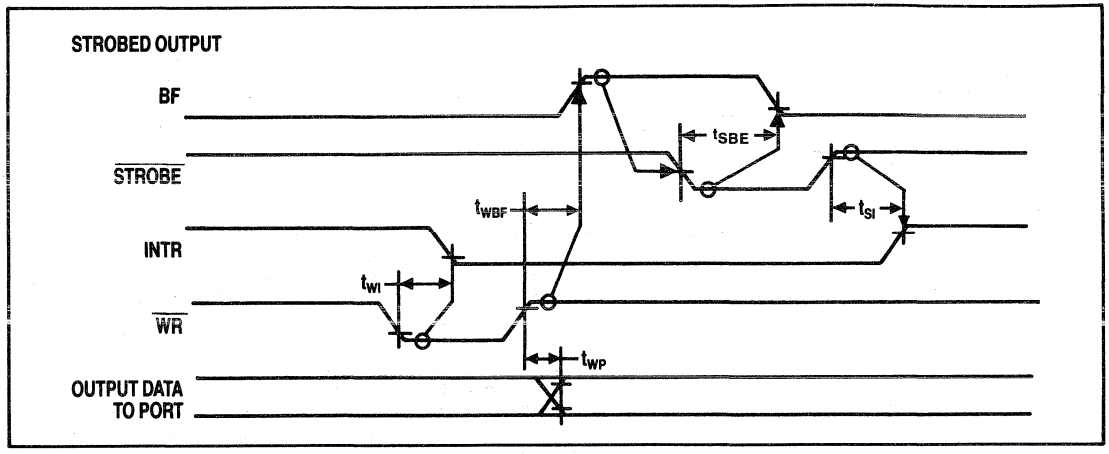
*C_L includes stray and jig capacitance.

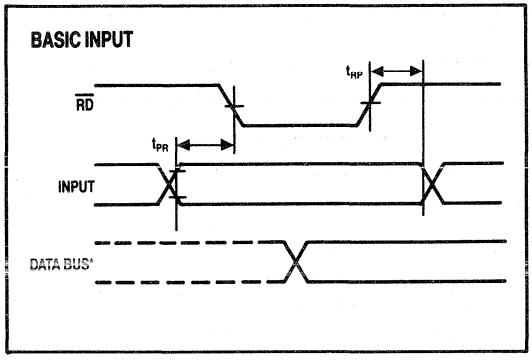
WAVEFORMS

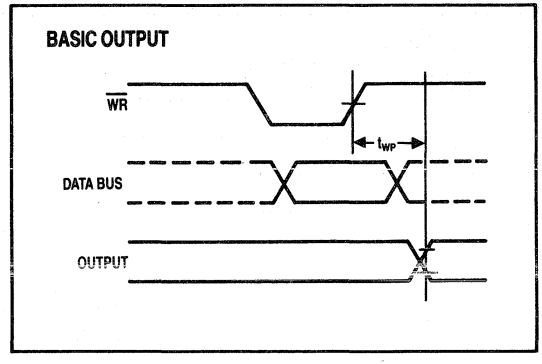

READ
CE (81C55RH)
OR
CE (81C56RH)
IO/M
AD0-7
ADDRESS
DATA VALID
ALE
RD
tAD
tAL
tLA
tLL
tRDE
tRDF
tRD
tCL
tLC
tCC
tRV

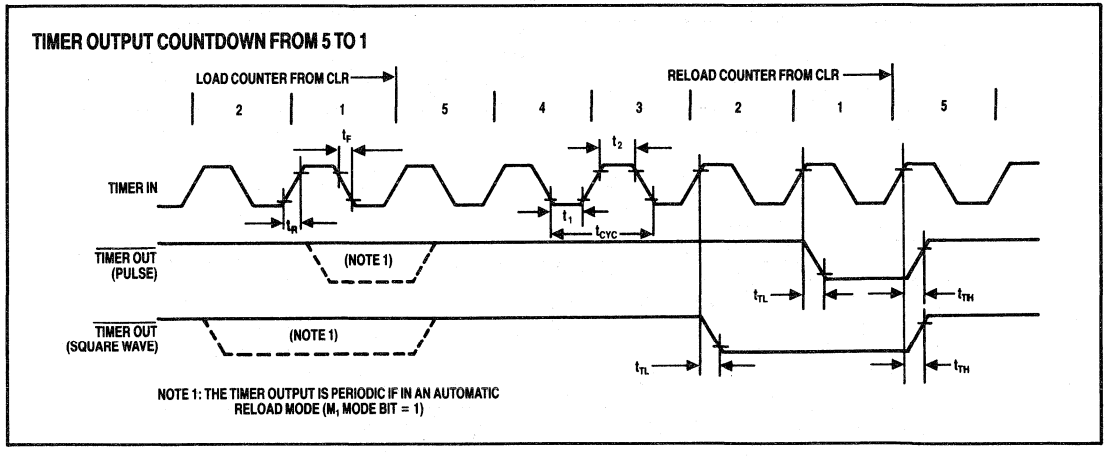

WRITE
CE(81C55RH)
OR
CE(81C56RH)
IO/M
AD0-7
ADDRESS
DATA VALID
ALE
WR
tAL
tLA
tDW
tCL
tLL
tLC
tWD
tCC
tRV


STROBED INPUT
BF
STROBE
INTR
RD
INPUT DATA
FROM PORT
tSBF
tSS
tSI
tRBE
tRDI
tPSS
tPHS









NOTE 1: THE TIMER OUTPUT IS PERIODIC IF IN AN AUTOMATIC RELOAD MODE (M_2 MODE BIT = 1)

Radiation Screening Procedure

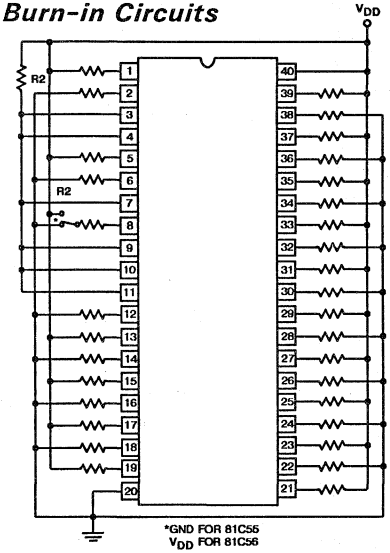
1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested to the customer's specification for proper operation.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad-Si (±10%) from a Gamma-cell 220 Cobalt 60 source or equivalent. The samples shall be biased at V_{DD} with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The lot will be accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-81C55/56RH has been designed to survive in a radiation environment and to meet the electrical characteristcs. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

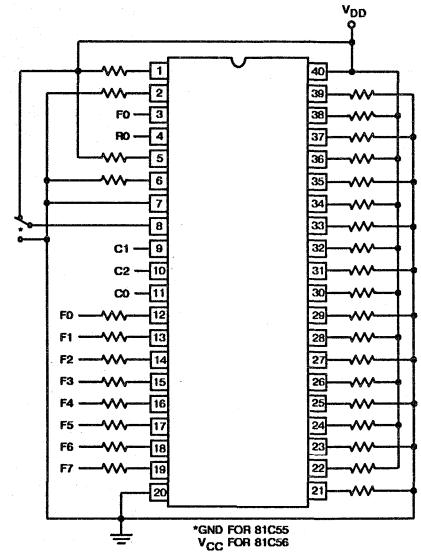
- Latch-up free to doses $\geq$ 1 x 10^{12} rads/sec.
- Upset (loss of stored data) $\geq$ 1 x 10^8 rads/sec.

Burn-in Circuits



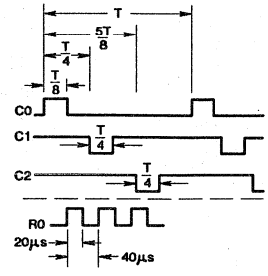
STATIC CONFIGURATION

V_{DD} = 10V ± 10%
All resistors R1 = 100kΩ unless otherwise marked:
R2 = 50K
Pin 8 tied through a resistor to two position switch. Label ground side "81C55" and V_{DD} side "81C56".



DYNAMIC CONFIGURATION

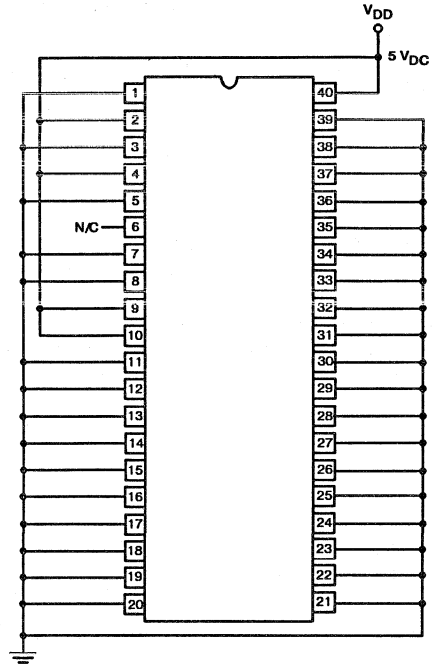
Minimum Temperature +125°C
All resistors 100kΩ 1/4 Watt. V_{DD} = 10V ± 10%.
Pin 8 tied to two position switch. Label ground side "81C55" and V_{DD} side "81C56".
Period of C0 = C1 = C2 = T = 10µs
C0 active HIGH, C1 & C2 active LOW.
C0, C1, C2 cannot overlap each other.
R0 shall have at least 3 pulses on power up as indicated below.
Pulses shall stop and R0 shall go to 0V no more than 60 seconds after power-up.



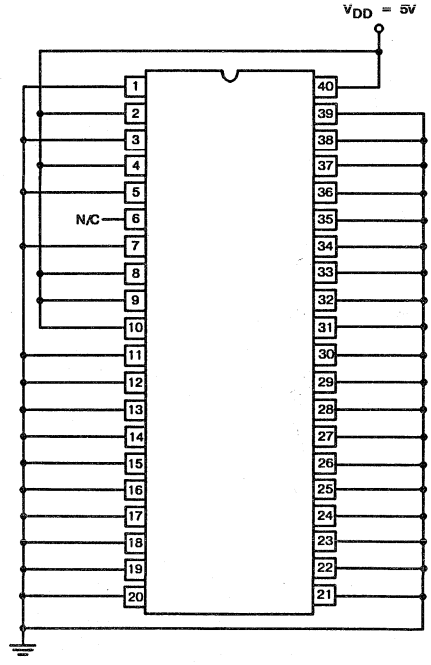
SIGNAL NAME	FREQUENCY	DUTY CYCLE
F0	50KHz	50%
F1	F0/2	50%
F2	F1/2	50%
F3	F2/2	50%
F4	F3/2	50%
F5	F4/2	50%
F6	F5/2	50%
F7	F6/2	50%

Irradiation Circuits

HS-81C55RH



HS-81C56RH



HARRIS HS-82C08RH

Radiation Hardened 8-Bit Bus Transceiver

July 1990

Features

- Radiation Hardened
  - Total Dose ..... 1×10^5 RAD(Si)
  - Latch-Up Immune EPI-CMOS ..... $> 1 \times 10^{12}$ RAD(Si)/s
- Bidirectional Three-State Input/Outputs
- Low Propagation Delay Time
- Low Power Consumption
- Single Power Supply ..... +5V
- Electrically Equivalent to Sandia SA2997
- Military Temperature Range ..... -55°C to +125°C

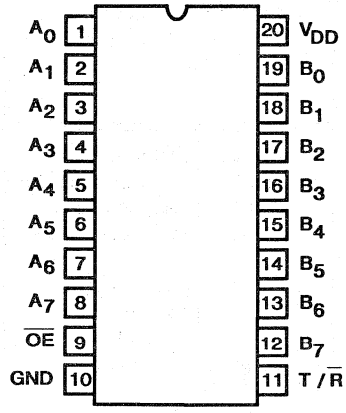
Description

The Harris HS-82C08RH is a radiation-hardened octal bus transceiver with three-state outputs. It is manufactured using a self-aligned, junction isolated CMOS process and is designed for use with the HS-80C85RH radiation-hardened microprocessor. The HS-82C85RH allows asynchronous two-way communication between data buses. The direction of data flow is determined by the logic level on the transmit/receive ($T/\overline{R}$) input. A logic high on the $T/\overline{R}$ input specifies data flow from Port A to Port B of the device. Conversely, a logic low on the $T/\overline{R}$ input specifies data flow from Port B to Port A. The Output Enable input disables both ports by placing them in the high impedance state.

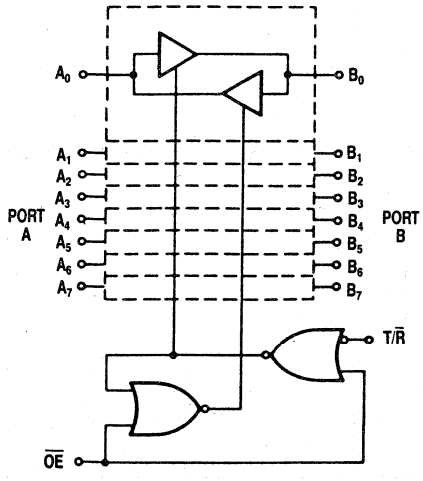
The HS-82C08RH is ideally suited for a wide variety of buffering applications in radiation-hardened microcomputer systems.

Pinout

TOP VIEW



Functional Diagram



PIN NAMES

A_0-A_7	Local Bus Data I/O Pins
B_0-B_7	System Bus Data I/O Pins
$T/\overline{R}$	Transmit/Receive Input
$\overline{OE}$	Active Low Output Enable

Truth Table

INPUTS		OPERATION	
OUTPUT ENABLE	TRANSMIT/ RECEIVE	PORT A	PORT B
0	0	Out	In
0	1	In	Out
1	X	High Z	High Z

X = Don't Care

Absolute Maximum Ratings

Supply Voltage (VDD to GND).....+7.0 Volts
Input or Output Voltage Applied ...(GND-0.3V)to(VDD+0.3V)
Storage Temperature Range .....-65°C to +150°C

Operating Range

Operating Supply Voltage..... +4.75V to +5.25V
Operating Temperature Range.....-55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

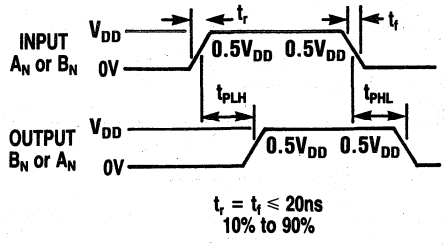
Electrical Specifications ②

			Radiation,① Temp. & VDD = Operating Range 5V ± 5%		Temp = 25°C VDD = 5.0V Typical			
	SYMBOL	PARAMETER	MIN	MAX	PRE-RAD	POST 100K RADS	UNITS	TEST CONDITIONS
D.C.	SIDD	Standby Supply Current		100	.008	.008	uA	VDD = 5.25V, Vin = VDD or GND.
	IIL	Input Leakage Current Low	−1		−.003	−.003	uA	VDD = 5.25V, Pin Under Test = 0V, Else VIN = VDD
	IIH	Input Leakage Current High		1	.005	.003	uA	VDD = 5.25V, Pin Under Test = 5.25V, Else VIN = OV
	VOL	Output Low Voltage		.5	.21	.225	V	VDD = 5.25V, Isink = 2.0mA, VIL = 1.0V, VIH = 4.25V
	VOH	Output High Voltage	4.25		4.55	4.45	V	VDD = 4.75V, Isource = −2.0mA, VIL = 1.0V, VIH = 3.75V
	VIL	Input Low Voltage		1.0			V	
	VIH	Input High Voltage	VDD − 1.0				V	
A.C.		**PORT DATA/MODE SPECIFICATIONS**						
	TPDLH	Propagation Delay to Logical "1" from Port A,B to Port B,A		65	45	40	ns	VDD = 4.75V, VIL = 1V, VIH = 3.75V, CL = 100pF
	TPDHL	Propagation Delay to Logical "0" from Port A,B to Port B,A		80	55	50	ns	
	TPRTH	Propagation Delay from High Impedance to Logical "1" from T/R to Port		75	45	45	ns	
	TPTRL	Propagation Delay from High Impedance to Logical "0" from T/R to Port		130	80	60	ns	
	TPZH	Propagation Delay from High Impedance to Logical "1" from OE to Port		70	40	40	ns	
	TPZL	Propagation Delay from High Impedance to Logical "0" from OE to Port		130	75	60	ns	
		TRANSMIT/RECEIVE MODE SPECIFICATIONS						
	TPHZTR	Propagation Delay from Logical "1" to High Impedance from T/R to Port ③		45	30	30	ns	
	TPLZTR	Propagation Delay from Logical "0" to High Impedance from T/R to Port ③		45	35	35	ns	
	TPHZ	Propagation Delay from Logical "1" to High Impedance from $\overline{OE}$ to Port ③		45	30	30	ns	
	TPLZ	Propagation Delay from Logical "0" to High Impedance from $\overline{OE}$ to Port ③		45	30	35	ns	

NOTES: ① All devices guaranteed at worst case limits. Room temperature typical data provided for information and not guaranteed. Post radiation data at Total Dose = 1×10^5 Rad(Si).
② Pre-radiation and Post-radiation limits.
③ Tested at initial device design and after major process/design changes.

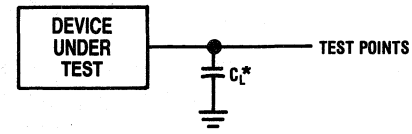
Switching Time Waveforms

Port to Port



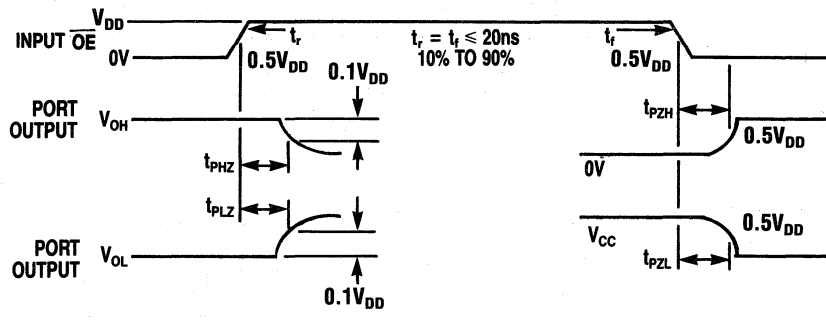
$t_r = t_f \leq 20ns$
10% to 90%

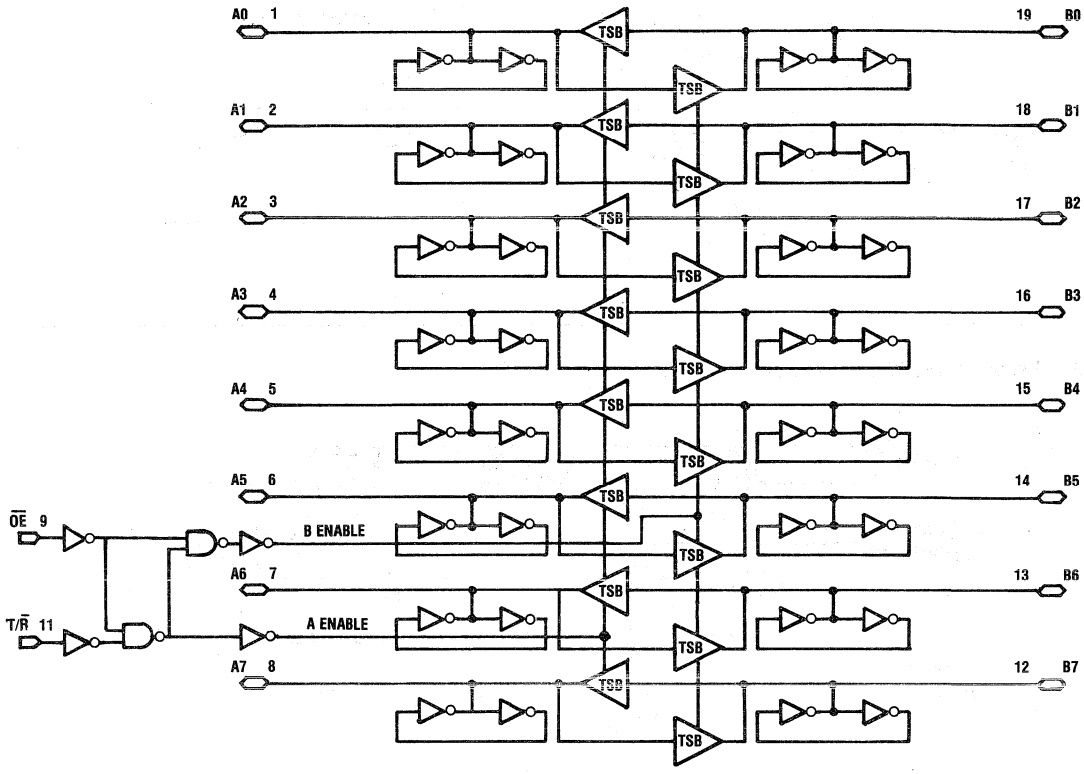
A.C. TESTING LOAD CIRCUIT



*C_L INCLUDES STRAY AND JIG CAPACITANCE

$\overline{OE}$ to High-Impedance, $\overline{OE}$ to Port Output





NOTE:
An important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule applies to inputs connected to a three-state bus. The need for external pull-up resistors during three-state bus conditions is eliminated by the presence of regenerative latches on the following HS-82C08RH pins: A0-7 and B0-7. The functional block diagram depicts one of these pins with the regenerative latch. When the CMOS driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the three-state condition. A transient drive current of ± 1.5mA at $V_{DD}/2$ ± 0.5V for 10ns is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during three-state conditions.

Radiation Screening Procedure

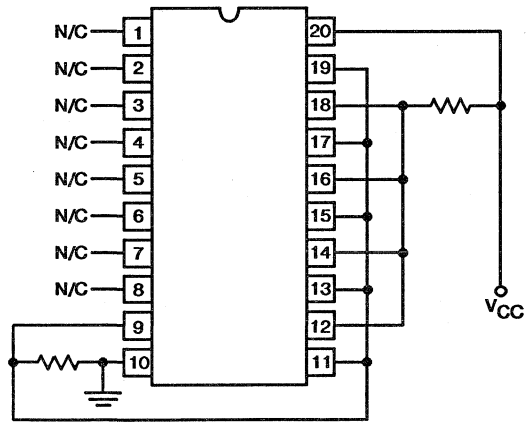
1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested to the customer's specification for proper operation.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad-Si (±10%) from a Gamma-cell 220 Cobalt 60 source or equivalent. The samples shall be biased at V_{DD} with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The lot will be accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact the factory for details.

Radiation Effects

The HS-82C08RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

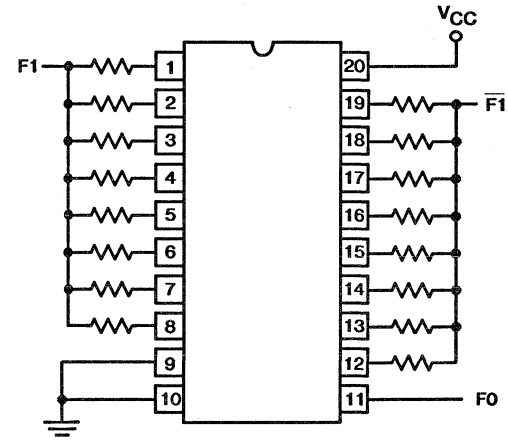
- Latch-up free to doses $\geq$ 1 x 10^{12} rads/sec.

Burn-In Circuits



STATIC CONFIGURATION

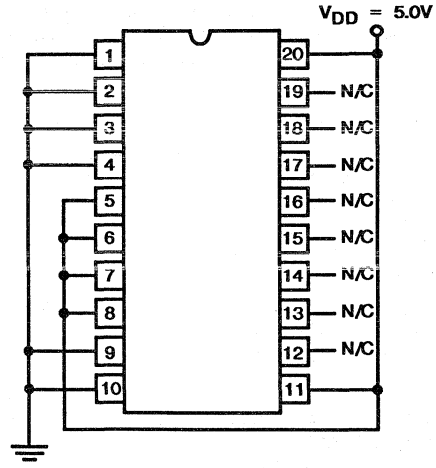
Minimum Temperature = +125°C
V_{CC} = 10V ± 5%
All resistors = 10kΩ, 1/4 Watt



DYNAMIC CONFIGURATION

Minimum Temperature = +125°C, V_{CC} = 10V ± 5%
All resistors = 10kΩ, 1/4 Watt
F1 = 100kHz, 50% Duty Cycle
F0 = F1/2, F1 = Complement of F1

Irradiation Circuit



HARRIS

HS-82C12RH

Radiation Hardened 8-Bit Input/Output Port

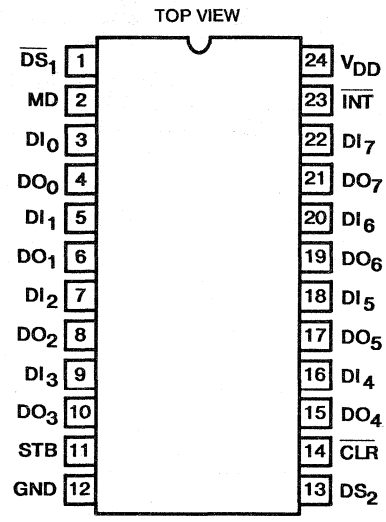
July 1990

Features

- Radiation Hardened CMOS Process
  - Total Dose ..... 1×10^5 RAD(Si)
  - Transient Upset ..... $> 1 \times 10^8$ RAD(Si)/s
  - Latch-Up Immune EPI-CMOS ..... $> 1 \times 10^{12}$ RAD(Si)/s
- Low Power Dissipation
- High Noise Immunity
- Single Power Supply ..... +5V
- Low Input Load Current
- 8-Bit Data Register and Buffer
- Asynchronous Register Clear
- Service Request Flip-Flop for Interrupt Generation
- Three-State Outputs
- Bus-Compatible with HS-80C85RH CPU
- Electrically Equivalent to Sandia SA3026
- Military Temperature Range..... -55°C to +125°C

Pinout

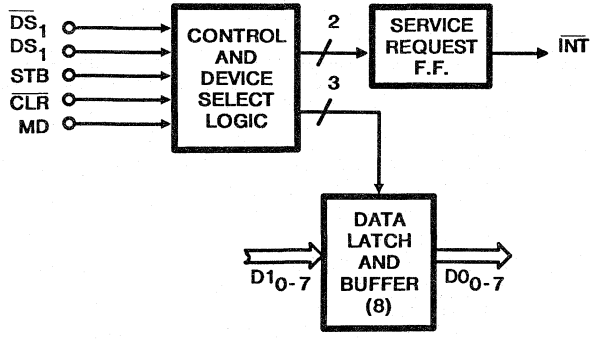
TOP VIEW



Description

The Harris HS-82C12RH is a radiation hardened 8-bit input/output port designed for use with the HS-80C85RH radiation hardened microprocessor. It is manufactured using a self-aligned, junction-isolated EPI-CMOS process and features three-state output buffers and device selection and control logic. A service request flip-flop is included for the generation and control of interrupts to the microprocessor. The device can be used in implement many of the peripheral and input/output functions of a microcomputer system. The HS-82C12RH is pinout- and function-compatible with industry-standard 8212 devices.

Functional Diagram

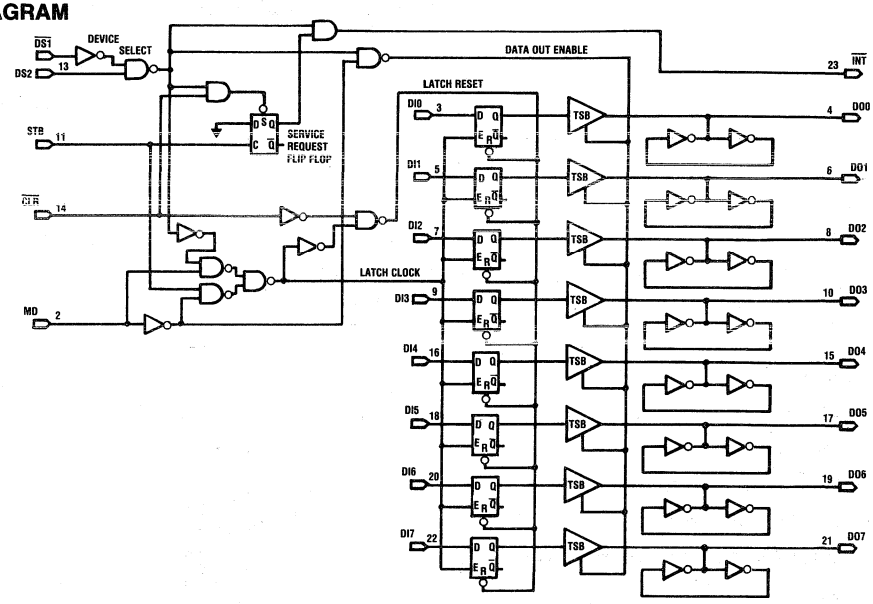


DI0-DI7	Data In
DO0-DO7	Data Out
DS1, DS2	Device Select
MD	Mode
STB	Strobe
INT	Interrupt
CLR	Clear

9 MICROPROCESSOR PERIPHERALS

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

LOGIC DIAGRAM



Truth Table I
DATA OUT

STB	MD	$\overline{DS_1} \cdot DS_2$	DATA OUT EQUALS
0	0	0	HIGH-Z STATE
1	0	0	HIGH-Z STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

Truth Table II
$\overline{INT}$

$\overline{CLR}$	$\overline{DS_1} \cdot DS_2$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌐	1	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop.

FUNCTIONAL DESCRIPTION

Data Latch

The data latch is comprised of eight "D" type flip-flops. The output of each flip-flop will follow the corresponding data input (DI_{0-7}) when the clock (C) is high. The clock input is level sensitive and the data becomes latched when the clock returns low.

An asynchronous reset ($\overline{CLR}$) is used to clear the latched data. Since the clock (C) overrides the reset ($\overline{CLR}$), the data must be in the latched state in order to clear the flip-flops. If the data is not latched (i.e., clock is high) when $\overline{CLR}$ goes low, then the Q outputs of the data latch will continue to follow the data inputs, overriding the reset signal.

Output Buffer

Three-state buffers are used to provide output drive for the data latch. A high level on the "output buffer enable" control line enables the buffer outputs. When "output buffer enable" is low the buffer outputs are forced to the high-impedance state.

Device Select Logic

The inputs $\overline{DS1}$ and DS2 are used for device selection. When $\overline{DS1}$ is low and DS2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously cleared when the device is selected.

Mode

The mode input (MD) is used to control the state of the output buffer and to determine the source of the data latch clock (C). When MD is high, the output buffers are enabled and the source of the data latch clock (C) is the device select logic ($\overline{DS1} \cdot DS2$).

When MD is low, the state of the output buffer is controlled by the device select logic ($\overline{DS1} \cdot DS2$) and the source of the data latch clock is the strobe (STB) input.

Strobe

The strobe input (STB) is used as the data latch clock (C) when the mode input (MD) is low. The service request flip-flop is synchronously set on the negative going edge of STB.

Service Request Flip-Flop

The service request flip-flop is to generate interrupts to microcomputer systems. It is negative edge triggered and asynchronously cleared (reset).

The output of the service request flip-flop is AND-gated with the device select logic ($\overline{DS1} \cdot DS2$). The output of the AND gate is the active low interrupt ($\overline{INT}$) signal.

Absolute Maximum Ratings

Supply Voltage (VDD to GND) ..... +7.0 Volts
Input or Output Voltage Applied
..... (GND − 0.3V) to (VDD + 0.3V)
Storage Temperature ..... −65°C to +150°C

Operating Conditions

Operating Supply Voltage ..... +4.75V to +5.25V
Operating Temperature Range ..... −55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications ②④

			Radiation,① Temp. & VDD = Operating Range 5V ± 5%		Temp = 25°C VDD = 5.0V Typical			
	SYMBOL	PARAMETER	MIN	MAX	PRE-RAD	POST RAD	UNITS	TEST CONDITIONS
D.C.	IDDSB	Standby Supply Current		100	1	1	uA	VDD = 5.25, Vin = GND or VDD.
	IIL	Input Leakage Current Low	−1		−.005	−.001	uA	VDD = 5.25, Pin Under Test VIN = 0V, Else VIN = 5.25V
	IIH	Input Leakage Current High		1	.004	.004	uA	VDD = 5.25, Pin Under Test VIN = 5.25V, Else VIN = 0V
	VOH	Output High Voltage	4.25		4.52	4.51	V	Isource = −2.0mA, VIL = 1.0V, VIH = 3.75V, VDD = 4.75V
	VOL	Output Low Voltage		.5	.28	.24	V	Isink = 2.0mA, VIL = 1.0V, VIH = 4.25V, VDD = 5.25V
	VIL	Input Low Voltage		1.0			V	
	VIH	Input High Voltage	VDD − 1.0				V	
A.C.	Tpw③	Pulse Width	50		20	20	ns	VDD = 4.75V, VIL = 1.0V, VIH = 3.75V, CL = 100pF
	Tpd	Data to Output Delay		105	75	75	ns	
	Twe	Write enable to Output Delay		200	135	120	ns	
	Tset③	Data Setup Time	30		10	10	ns	
	Th③	Data Hold Time	40		16	16	ns	
	Tr	Reset to Output Delay		145	90	75	ns	
	Ts	Set to Output Delay		100	60	85	ns	
	Tc	Clear to Output Delay		135	90	80	ns	
	Te	Output Enable Time		125	80	60	ns	
	Td	Output Disable Time		85	65	65	ns	

NOTES

① All devices guaranteed at worst case limits. Room temperature typical data provided for information and not guaranteed. Post radiation data at Total Dose = 1×10^5 Rad(Si).

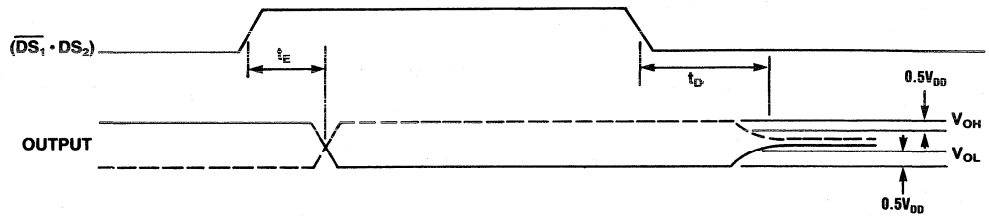
② Pre-radiation and Post-radiation limits.

③ Guaranteed but not tested.

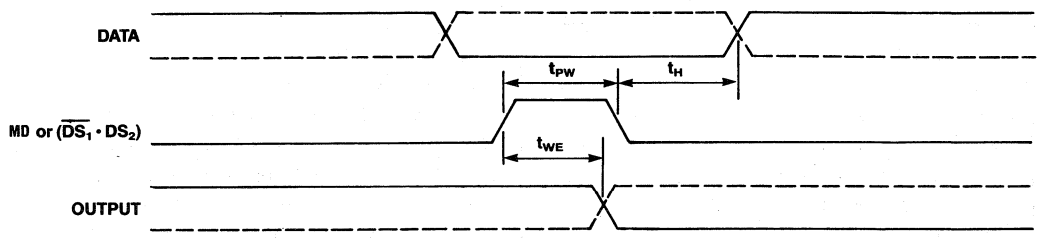
④ A caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule applies to inputs connected to a three-state bus. The need for external pull-up resistors during three-state bus conditions is eliminated by the presence of regenerative latches on the following HS-82C12RH pins: DO0-7. The functional block diagram depicts one of these pins with the regenerative latch. When the CMOS driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the three-state condition. A transient drive current of ±1.0mA at $V_{DD}/2$ ±0.5V for 10ns is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during three-state conditions.

TIMING WAVEFORMS

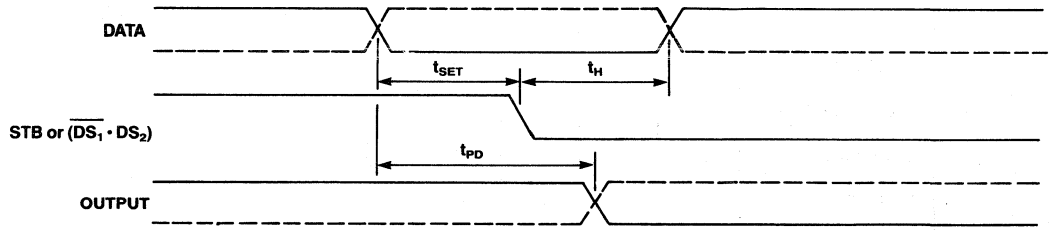
Read Timing



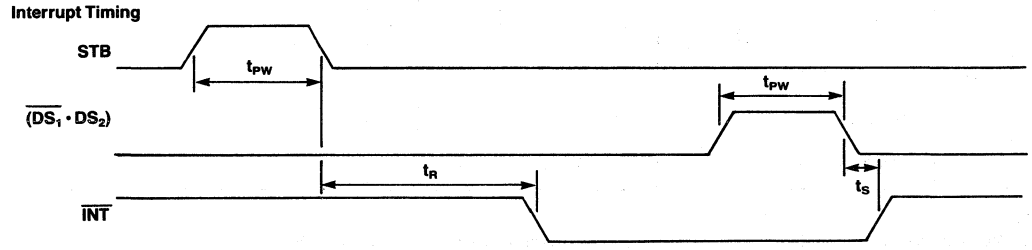
Write Timing



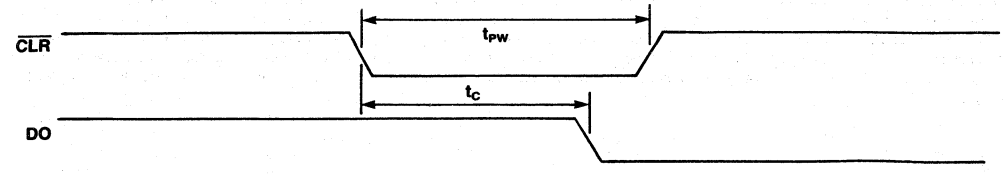
Data Setup, Hold, Propagation Delay Timing



Interrupt Timing



Clear Timing



Radiation Screening Procedure

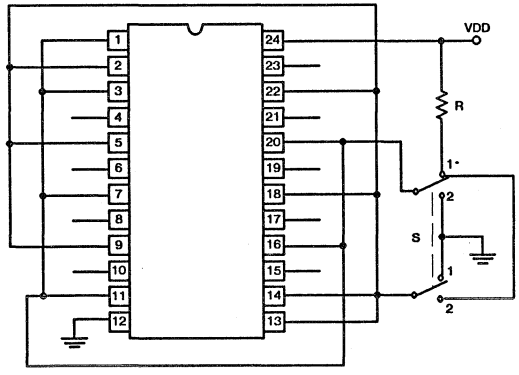
1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested to the customer's specification for proper operation.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad-Si (±10%) from a Gamma-cell 220 Cobalt 60 source or equivalent. The samples shall be biased at V_{DD} with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The lot will be accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact the factory for details.

Radiation Effects

The HS-6514RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

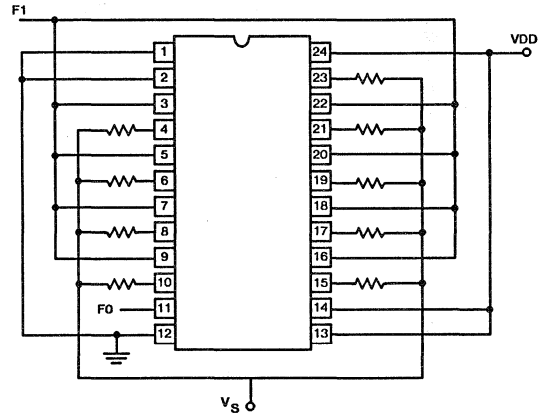
- Latch-up free to doses ≥ 1 x 10^{12} rads/sec.
- Upset (loss of stored data) ≥ 10^8 rads/sec.

Burn-In Circuits



STATIC CONFIGURATION

VDD = +10.0V ± 10%, TA Min = +125°C,
Resistors: R1 = 10kΩ ± 10%, 1/4 Watt
Part is Static Sensitive, Voltage Must Be Ramped
Package: 24 Lead DIP/FP, Package Code: SZ/WL
S (DPDT) in Position 1 for Static Burn-In I
S (DPDT) in Position 2 for Static Burn-In II



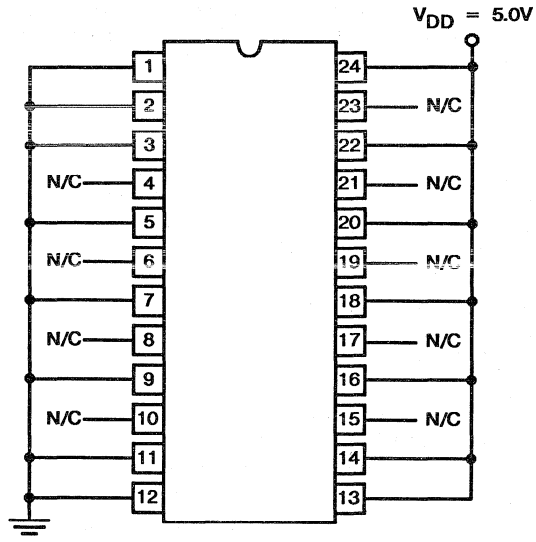
DYNAMIC CONFIGURATION

VDD = 10V ± 10%, VS = 5V ± 10%, TA Min = +125°C,
All Resistors are 10kΩ ± 10%, 1/4 Watt.
Part is Static Sensitive, Voltages Must Be Ramped.
Package: 24 Pin DIP, Package Code: SZ

SIGNAL TIMING

F0 = 1.0kHz 50% Duty Cycle, F1 = F0/2 50% Duty Cycle
VIH = 4.5V, VIL = 0.8V, Part is Static Sensitive

Irradiation Circuit



HARRIS HS-82C37ARH

Radiation Hardened CMOS High Performance Programmable DMA Controller

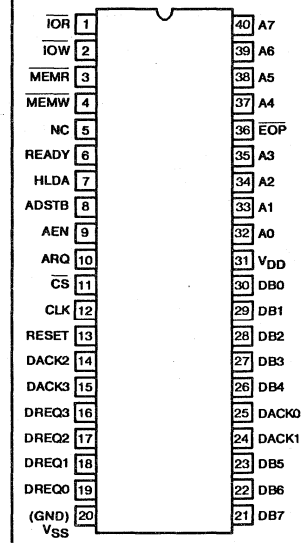
July 1990

Features

- Radiation Hardened
  - Total Dose ..... > 10^5 RAD (Si)
  - Transient Upset .....> 10^8 RAD (Si)/sec
  - Latch Up Free EPI-CMOS
  - Functional After Total Dose ... 10^6 RAD(Si)
- Low Power Consumption
  - IDDSB = 50µA Maximum
  - IDDOP = 4.0mA/MHz Maximum
- Pin Compatible with NMOS 8237A and the Harris 82C37A
- High Speed Data Transfers Up To 2.5 MBPS With 5MHz Clock
- Four Independent Maskable Channels With Autoinitialization Capability
- Expandable to Any Number of Channels
- Memory-to-Memory Transfer Capability
- CMOS Compatible
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- Military Temperature Range ..... -55°C to +125°C

Pinout

DIP
TOP VIEW



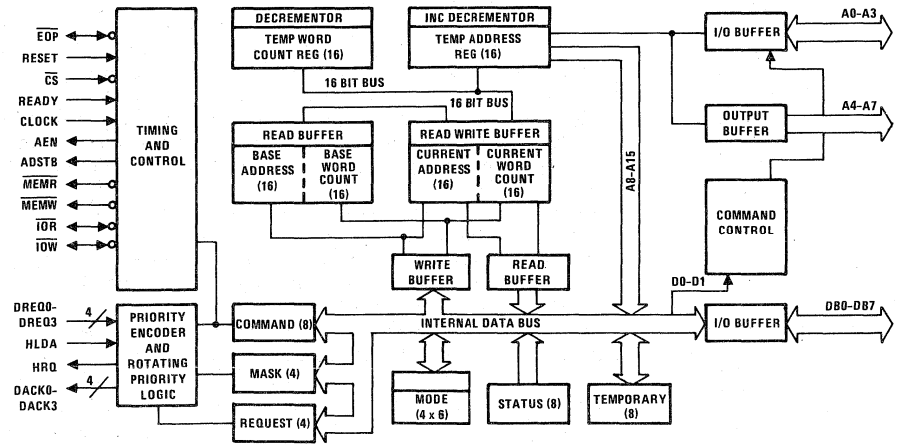
Description

The Harris HS-82C37ARH is an enhanced, radiation hardened CMOS version of the industry standard 8237A Direct Memory Access (DMA) controller, fabricated using the Harris hardened field, self-aligned silicon gate CMOS process. The HS-82C37ARH offers increased functionality, improved performance, and dramatically reduced power consumption for the radiation environment. The high speed, radiation hardness, and industry standard configuration of the HS-82C37ARH make it compatible with radiation hardened microprocessors such as the HS-80C85RH and the HS-80C86RH.

The HS-82C37ARH can improve system performance by allowing external devices to transfer data directly to or from system memory. Memory-to-memory transfer capability is also provided, along with a memory block initialization feature. DMA requests may be generated by either hardware or software, and each channel is independently programmable with a variety of features for flexible operation.

Static CMOS circuit design insures low operating power and allows gated clock operation for an even further reduction of power. Multimode programmability allows the user to select from three basic types of DMA services, and reconfiguration under program control is possible even with the clock to the controller stopped. Each channel has a full 64K address and word count range, and may be programmed to autoinitialize these registers following DMA termination (end of process). The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VDD	31		VDD: is the +5V power supply pin. A 0.1μF capacitor between pins 31 and 20 is recommended for decoupling.
GND	20		Ground
CLK	12	I	CLOCK INPUT: The Clock Input is used to generate the timing signals which control HS-82C37ARH operations. This input may be driven from DC to 5 MHz and may be stopped in either high or low state for standby operation.
$\overline{CS}$	11	I	CHIP SELECT: Chip Select is an active low input used to enable the controller onto the data bus for CPU communications.
RESET	13	I	RESET: This is an active high input which clears the Command, Status, Request, and Temporary Registers, the First/Last Flip-Flop, and the Mode Register Counter. The Mask Register is set to ignore requests. Following a Reset, the controller is in an Idle cycle.
READY	6	I	READY: This signal can be used to extend the memory read and write pulses from the HS-82C37ARH to accommodate slow memories or I/O devices. Ready must not make transitions during its specified set-up and hold times. Ready is ignored in Verify transfer mode.
HLDA	7	I	HOLD ACKNOWLEDGE: The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.
DREQ0-DREQ3	16-19	I	DMA REQUEST: The DMA Request (DREQ) lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled High or Low (inactive) and the corresponding mask bit set.
DB0-DB7	21-23 26-30	I/O	DATA BUS: The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program Condition during the I/O Read to output the contents of a register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the HS-82C37ARH Control Registers. During DMA cycles, the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In Memory-to-Memory operations, data from the memory enters the HS-82C37ARH on the data bus during the read-from-memory transfer, then during the write-to-memory transfer, the data bus outputs write the data into the new memory location.
$\overline{IOR}$	1	I/O	I/O READ: I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the internal registers. In the Active cycle, it is an output control signal used by the HS-82C37ARH to access data from a peripheral during a DMA Write transfer.
$\overline{IOW}$	2	I/O	I/O WRITE: I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the HS-82C37ARH. In the Active cycle, it is an output control signal used by the HS-82C37ARH to load data to the peripheral during a DMA Read transfer.

TABLE 1. PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{EOP}$	36	I/O	END OF PROCESS: End of Process ($\overline{EOP}$) is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The HS-82C37ARH allows an external signal to terminate an active DMA service by pulling the $\overline{EOP}$ pin low. A pulse is generated by the HS-82C37ARH when terminal count (TC) for any channel is reached, except for channel 0 in Memory-to-Memory mode. During Memory-to-Memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. The $\overline{EOP}$ pin is driven by an open drain transistor on-chip, and requires an external pull-up resistor. When an $\overline{EOP}$ pulse occurs, whether internally or externally generated, the HS-82C37ARH will terminate the service, and if Autoinitialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the Status Register will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains clear.
A0-A3	32-35	I/O	Address: The four least significant address lines are bidirectional three-state signals. In the Idle cycle, they are inputs and are used by the HS-80C86RH to address the internal registers to be loaded or read. In the Active cycle, they are outputs and provide the lower 4 bits of the output address.
A4-A7	37-40	O	Address: The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the Active cycle.
HRQ	10	O	Hold Request: The Hold Request (HRQ) output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the HS-82C37ARH issues HRQ. The HLDA signal then informs the controller when access to the system busses is permitted. For stand-alone operation where the HS-82C37ARH always controls the busses, HRQ may be tied to HLDA. This will result in one S0 state before the transfer.
DACK0- DACK 3	14,15 24,25	O	DMA Acknowledge: DMA acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	9	O	Address Enable: Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	8	O	Address Strobe: This is an active high signal used to control latching of the upper address byte. It will drive directly the strobe input of external transparent octal latches, such as the 82C82. During block operations, ADSTB will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. (See Note 2).
$\overline{MEMR}$	3	O	Memory Read: The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a Memory-to-Memory transfer.
$\overline{MEMW}$	4	O	Memory Write: The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a Memory-to-Memory transfer.
NC	5		No connect. Pin 5 is open and should not be tested for continuity.

Functional Description

The HS-82C37ARH Direct Memory Access Controller is designed to improve the data transfer rate in systems which must transfer data from an I/O device to memory, or move a block of memory to an I/O device. It will also perform memory-to-memory block moves, or fill a block of memory with data from a single location. Operating modes are provided to handle single byte transfers a well as discontinuous data streams, which allows the HS-82C37ARH to control data movement with software transparency.

The DMA controller is a state-driven address and control signal generator, which permits data to be transferred directly from an I/O device to memory or vice versa without ever being stored in a temporary register. This can greatly increase the data transfer rate for sequential operations, compared with processor moves or repeated string instructions. Memory-to-Memory operations require temporary internal storage of the data byte between generation of the source and destination addresses, so Memory-to-Memory transfers take place at less than half the rate of I/O operations, but still much faster than with central processor techniques. The maximum data transfer rate obtainable with the HS-82C37ARH is approximately 2.5 Mbytes/second, for an I/O operation using the compressed timing option and 5 MHz clock.

The block diagram of the HS-82C37ARH is shown on page 1. The Timing and Control Block, Priority Block, and internal registers are the main components. Figure 1 lists the name and size of the internal registers. The Timing and Control Block derives internal timing from the CLOCK input, and generates external control signals. The Priority Encoder Block resolves priority contention between DMA channels requesting service simultaneously.

NAME	SIZE	NUMBER
Base Address Registers	16 Bits	4
Base Word Count Registers	16 Bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Registers	4 bits	1
Request Register	4 bits	1

FIGURE 1. HS-82C37ARH INTERNAL REGISTERS

DMA Operation

In a system, the HS-82C37ARH address and control outputs and data bus pins are basically connected in parallel with the system busses. An external latch is required for the upper address byte. While inactive, the controller's outputs are in a high impedence state. When activated by a DMA request and bus control is relinquished by the host, the HS-82C37ARH drives the busses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the Command, Mode, Address, and Word Count Registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the HS-82C37ARH Current and Base Address Registers for a particular channel, and the length of the block is loaded into that channel's Word Count Register. The corresponding Mode Register is programmed for a Memory-to-I/O operation (read transfer), and various options are selected by the Command Register and other Mode Register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ). The DREQ can either be a hardware signal or a software command.

Once initiated, the block DMA transfer will proceed as the controller outputs the data address, simultaneous $\overline{MEMR}$ and $\overline{IOW}$ pulses, and selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the Word Count Register underflows, or an external $\overline{EOP}$ is applied.

To further understand HS-82C37ARH operation, the states generated by each clock cycle must be considered. The DMA controller operates in two major cycles, Active and Idle. After being programmed, the controller is normally Idle until a DMA request occurs on an unmasked channel, or a software request is given. The HS-82C37ARH will then request control of the system busses and enter the Active cycle. The Active cycle is composed of several internal states, depending on what options have been selected and what type of operation has been requested.

The HS-82C37ARH can assume seven separate states, each composed of one full clock period. State I (SI) is the Idle state. It is entered when the HS-82C37ARH has no valid DMA requests pending, at the end of a transfer sequence, or when a Reset or Master Clear has occurred. While in SI, the DMA controller is inactive but may be in the Program Condition (being programmed by the processor.)

State 0 (S0) is the first state of a DMA service. The HS-82C37ARH has requested a hold but the processor has not yet returned an acknowledge. The HS-82C37ARH may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the HS-82C37ARH.

Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is not read into or driven out of the HS-82C37ARH in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-Memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14 are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service, the HS-82C37ARH will enter the Idle cycle and perform "SI" states. In this cycle, the HS-82C37ARH will sample the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that for standby operation where the clock has been stopped, DMA requests will be ignored. The device will respond to $\overline{CS}$ (chip select), in case of an attempt by the microprocessor to write or read the internal registers of the HS-82C37ARH. When $\overline{CS}$ is low and HLDA is low, the HS-82C37ARH enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers.

The HS-82C37ARH may be programmed with the clock stopped, provided that HLDA is low and at least one rising clock edge has occurred after HLDA was driven low, so the controller is in an SI state. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time the read or write operations. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. The bit is used to determine the upper or lower byte of the 16-bit Address and Word Count Registers. The flip-flop is reset by Master Clear or Reset. Separate software commands can also set or reset this flip-flop.

Special software commands can be executed by the HS-82C37ARH in the Program Condition. These commands are decoded as sets of addresses with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Set and Clear First/Last Flip-Flop, Master Clear, Clear Mode Register Counter, and Clear Mask Register.

Active Cycle

When the HS-82C37ARH is in the Idle cycle, and a software request or an unmasked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode — In Single Transfer mode, the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a terminal count (TC) bit in the Status Register is set, an $\overline{EOP}$ pulse is generated, and the channel will Autoinitialize if this option has been selected. If not programmed to Autoinitialize, the mask bit will be set, along with the TC bit and $\overline{EOP}$ pulse.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer (thereby triggering a second transfer), HRQ will still go inactive and release the bus to the system. Then it will again go active and, upon receipt of a new HLDA, another single transfer will be performed, unless a higher priority channel takes over. In HS-80C85RH or HS-80C86RH systems, this will ensure one full machine cycle execution between DMA transfers. Details of timing between the HS-82C37ARH and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode — In Block Transfer Mode, the device is activated by DREQ or software request and continues making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode — In Demand Transfer Mode the device continues making transfers until a TC or external $\overline{EOP}$ is encountered, or until DREQ goes inactive. Thus, transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is reestablished by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the HS-82C37ARH Current Address and Current Word Count Registers. Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an $\overline{EOP}$ can cause an Autoinitialization at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode — This mode is used to cascade more than one HS-82C37ARH for simple system expansion. The HRQ and HLDA signals from the additional HS-82C37ARH are connected to the DREQ and DACK signals respectively of a channel for the initial HS-82C37ARH. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial HS-82C37ARH is used only for prioritizing the additional device, it does not output an address or control signals of its own so that there is no conflict with the cascaded device. The HS-82C37ARH will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external $\overline{EOP}$ will be ignored by the initial device, but will have the usual effect on the added device.

Figure 2 shows two additional devices cascaded with an initial device using two of the previous channels. This forms a two-level DMA system. More HS-82C37ARHs could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

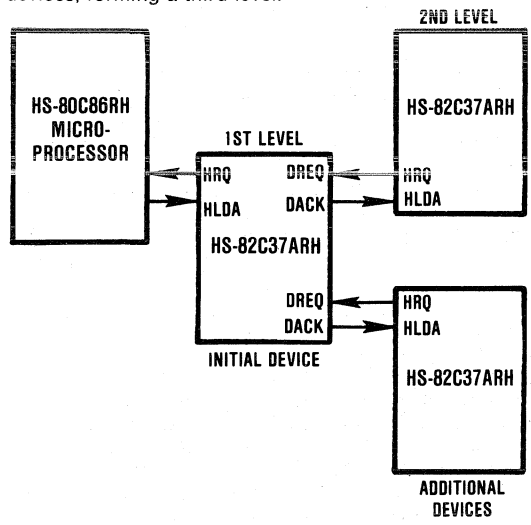


FIGURE 2. CASCADED HS-82C37ARHs

When programming cascaded controllers, start with the first level (closest to the microprocessor). After RESET, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. Also, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{\text{MEMW}}$ and $\overline{\text{IOR}}$. Read transfers move data from memory to an I/O device by activating $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$.

Verify transfers are pseudo-transfers. The HS-82C37ARH operates as in Read or Write transfers generating addresses and responding to $\overline{\text{EOP}}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not permitted for Memory-to-Memory operation. Ready is ignored during Verify transfers.

Autoinitialize — By programming a bit in the Mode Register, a channel may be set up as an Autoinitialize channel. During Autoinitialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following $\overline{\text{EOP}}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request made.

Memory-to-Memory — To perform block moves of data from one memory address space to another with minimum of program effort and time, the HS-82C37ARH includes a Memory-to-Memory transfer feature. Programming a bit in the Command Register selects channels 0 and 1 to operate as Memory-to-Memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The HS-82C37ARH requests a DMA service in the normal manner. After HLDA is true, the device, using four-state transfers in Block Transfer Mode, reads data from the memory. The channel 0 Current Address Register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the HS-82C37ARH internal Temporary Register. Another four-state transfer moves the data to memory using the address in channel 1's Current Address Register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count Register is decremented.

When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{\text{EOP}}$ output terminating the service. Channel 0 word count decrementing to FFFFH will not set the channel 0 TC bit in the Status Register or generate an $\overline{\text{EOP}}$ in this mode. It will cause an Autoinitialization of channel 0, if that option has been selected.

If full Autoinitialization for a Memory-to-Memory operation is desired, the channel 0 and channel 1 word counts must be set equal before the transfer begins. Otherwise, if channel 0 underflows before channel 1, it will Autoinitialize and set the data source address back to the beginning of the block. If the channel 1 word count underflows before channel 0, the Memory-to-Memory DMA service will terminate, and channel 1 will Autoinitialize but channel 0 will not.

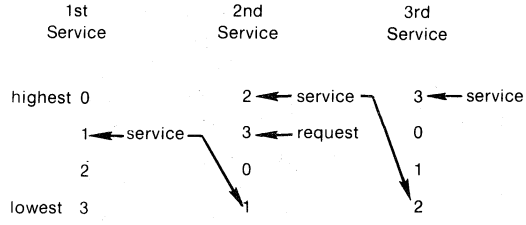
In Memory-to-Memory Mode, Channel 0 may be programmed to retain the same address for all transfers. This allows a single byte to be written to a block of memory. This channel 0 address hold feature is selected by bit 1 in the Command Register.

The HS-82C37ARH will respond to external $\overline{\text{EOP}}$ signals during Memory-to-Memory transfers, but will only relinquish the system busses after the transfer is complete (i.e., after an S24 state). Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of Memory-to-Memory transfers is found in Figure 9. Memory-to-Memory operations can be detected as an active AEN with no DACK outputs.

Priority — The HS-82C37ARH has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with the service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. The next lower channel from the channel serviced has highest priority on the following request: Priority rotates every time control of the system busses is returned to the processor.

Rotating Priority



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Regardless of which priority scheme is chosen, priority is evaluated every time a HLDA is returned to the HS-82C37ARH.

Compressed Timing — In order to achieve even greater throughput where system characteristics permit, the HS-82C37ARH can compress the transfer time to two clock cycles. From Figure 8 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 11. $\overline{EOP}$ will be output in S2 if compressed timing is selected. Compressed Timing is not allowed for Memory-to-Memory transfers.

Address Generation — In order to reduce pin count, the HS-82C37ARH multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the HS-82C37ARH directly. Lines A0-A7 should be connected to the address bus. Figure 8 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer Mode service, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the HS-82C37ARH executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may ocur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

Programming

The HS-82C37ARH will accept programming from the host processor anytime that HLDA is inactive, and at least one rising clock edge has occurred after HLDA went low. It is the responsibility of the host to assure that programming and HLDA are mutually exclusive.

Note that a problem can occur if a DMA request occurs on an unmasked channel while the HS-82C37ARH is being programmed. For instance, the CPU may be starting to reprogram the two byte Address Register of channel 1 when channel 1 receives a DMA request. If the HS-82C37ARH is enabled (bit 2 in the command register is 0), and channel 1 is unmasked, a DMA service will occur after only one byte of the Address Register has been reprogrammed. This condition can be avoided by disabling the controller (setting bit 2 in the Command Register) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations be loaded with some known value, even if some channels are unused. This will aid in debugging.

Register Description

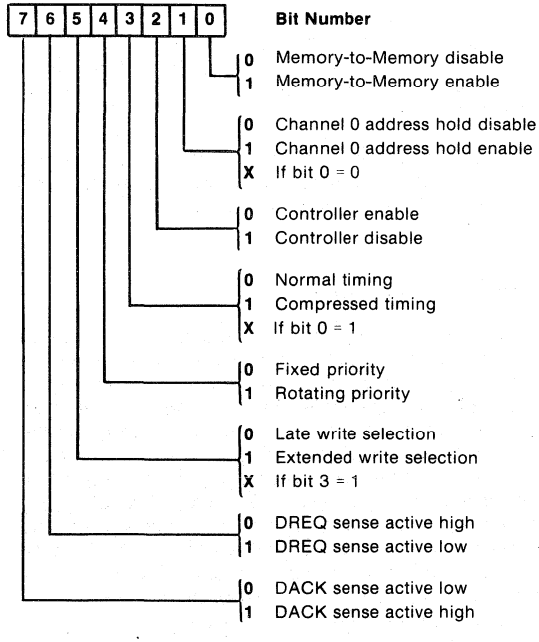
Current Address Register — Each channel has a 16-bit Current Address Register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the values of the address are stored in the Current Address Register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$. In Memory-to-Memory Mode, the channel 0 Current Address Register can be prevented from incrementing or decrementing by setting the address hold bit in the Command Register.

Current Word Register — Each channel has a 16-Bit Current Word Count Register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count Register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialization can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

Base Address and Base Word Count Registers — Each channel has a pair of Base Address and Base Word Count Registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialization, these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

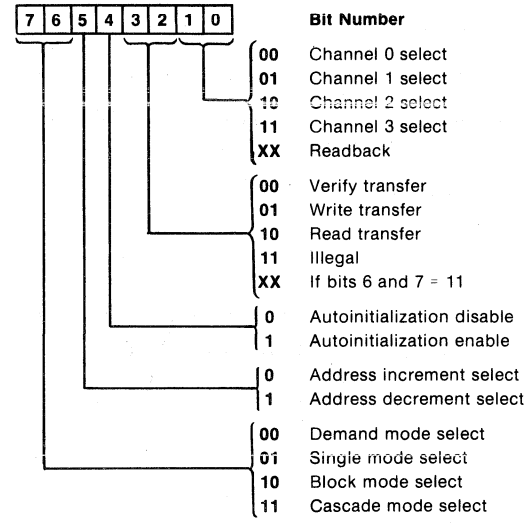
Command Register — This 8-bit register controls the operation of the HS-82C37ARH. It is programmed by the microprocessor and is cleared by Reset or a Master Clear instruction. The adjacent table lists the function of the command bits. See Figure 3 for Read and Write addresses.

Command Register



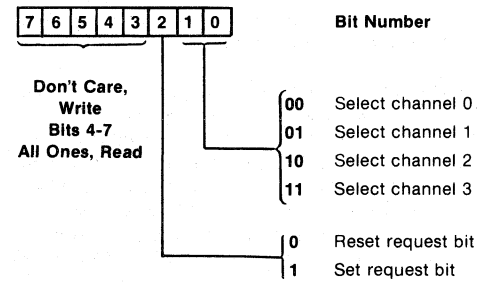
Mode Register — Each channel has a 6-bit Mode Register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode Register is to be written. When the processor reads a Mode Register, bits 0 and 1 will both be ones. See the adjacent table and Figure 3 for Mode Register functions and addresses.

Mode Register



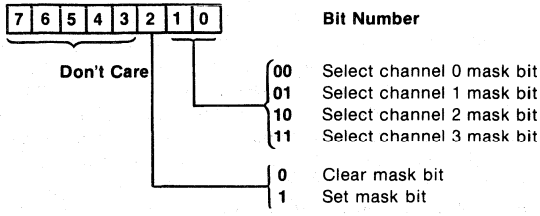
Request Register — The HS-82C37ARH can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request Register. These are non-maskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 3 for register address coding, and the following table for Request Register format. A software request for DMA operation can be made in Block or Single Modes. For Memory-to-Memory transfers, the software request for channel 0 should be set. When reading the Request Register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

Request Register

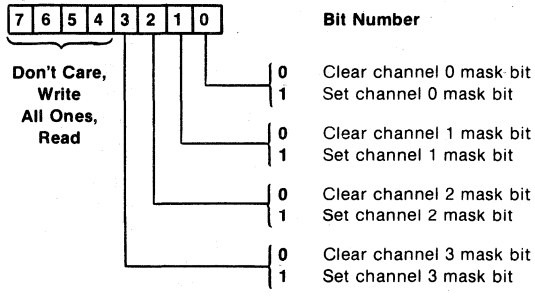


Mask Register — Each channel has associated with it a mask bit which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to Autoinitialize. Each bit of the 4-bit Mask Register may also be set or cleared separately or simultaneously under software control. The entire register is also set by a Reset or Master Clear. This disables all hardware DMA requests until a clear Mask Register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request Register. Refer to the following table and Figure 3 for details. When reading the Mask Register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channel 0-3, respectively. The 4 bits of the Mask Register may be cleared simultaneously by using the Clear Mask Register command (see software commands section).

Mask Register

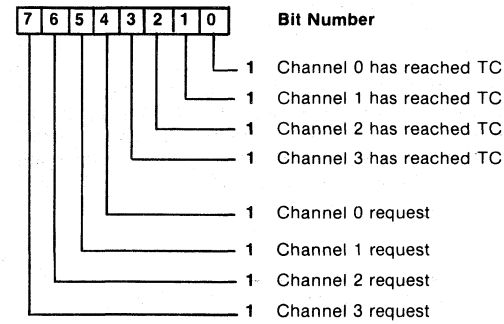


All four bits of the Mask Register may also be written with a single command.



Status Register — The Status Register contains information about the present status of the HS-82C37ARH and can be read by the microprocessor. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset, Master Clear, and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the Status Register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status Bits 4-7 are cleared upon Reset or Master Clear.

Status Register



Temporary Register — The Temporary Register is used to hold data during Memory-to-Memory transfers. Following the completion of the transfer, the last word moved can be read by the microprocessor by accessing this register. The Temporary Register always contains the last byte transferred in the previous Memory-to-Memory operation, unless cleared by a Reset or Master Clear.

OPERATION	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Mask Bit	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set Byte Pointer F/F	1	1	0	0	0	1
Clear Byte Pointer F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Reg. Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

FIGURE 3. SOFTWARE COMMAND CODES AND REGISTER CODES

Software Commands

There are special software commands which can be executed by reading or writing to the HS-82C37ARH. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself. On read type commands, the data value is not guaranteed. These commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the HS-82C37ARH. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Set First/Last Flip-Flop: This command will set the flip-flop to select the high byte first on read and write operations to Address and Word Count registers.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, and Temporary Registers, and Internal First/Last Flip-Flop and Mode Register Counter are cleared and the Mask Register is set. The HS-82C37ARH will enter the Idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter: Since only one address location is available for reading the Mode Registers, an internal two-bit counter has been included to select Mode Registers during read operations. To read the Mode Registers, first execute the Clear Mode Register Counter command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last. The lower two bits on all Mode Registers will read as ones.

External $\overline{EOP}$ Operation

The $\overline{EOP}$ pin is a bidirectional, open drain pin which may be driven by external signals to terminate DMA operation. Because $\overline{EOP}$ is an open drain pin an external pull-up resistor is required. The value of the external pull-up resistor used should guarantee a rise time of less than 125ns. It is important to note that the HS-82C37ARH will not accept external $\overline{EOP}$ signals when it is in an SI (Idle) state. The controller must be active to latch EXT $\overline{EOP}$. Once latched, the EXT $\overline{EOP}$ will be acted upon during the next S2 state, unless the HS-82C37ARH enters an Idle

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

FIGURE 4. WORD COUNT AND ADDRESS REGISTER COMMAND CODES.

state first. In the latter case the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses occurring between active DMA transfers in demand mode will not be recognized, since the HS-82C37ARH is in an SI state.

Application Information

Figure 5 shows an application for a DMA system utilizing the HS-82C37ARH DMA controller and the HS-80C86RH Microprocessor. In this application, the HS-82C37ARH DMA controller is used to improve system performance by allowing an I/O device to transfer data directly to or from system memory.

Components

The system clock is generated by the HS-82C85RH clock controller/generator and is inverted to meet the clock high and low times required by the HS-82C37ARH DMA controller. The four OR gates are used to support the HS-80C86RH Microprocessor in minimum mode by producing the control signals used by the processor to access memory or I/O. A decoder is used to generate chip select for the DMA controller and memory. The HS-82C37ARH multiplexes the most significant bits of the address on its data outputs (DB0 - 7), so the 82C82 octal latch is used to demultiplex the address. A three-state inverter is used to generate the $\overline{BHE}$ signal using the A_0 output of the HS-82C37ARH. Hold Acknowledge (HLDA) and Address Enable (AEN) are "ORed" together and used to deactivate the microprocessors 82C82 transceiver to insure that the DMA controller does not have bus contention with the microprocessor.

Operation

A DMA request (DREQ) is generated by the I/O device. After receiving the DMA request, the DMA controller will issue a Hold Request (HRQ) to the processor. The system busses are not released to the DMA controller until a Hold Acknowledge (HLDA) signal is returned to the DMA controller from the HS-80C86RH processor. After the Hold Acknowledge has been received, addresses and control signals are generated by the DMA controller to accomplish the DMA transfers. Data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active. Note that data is not read into or driven out of the DMA controller in I/O-to-Memory or Memory-to-I/O data transfers.

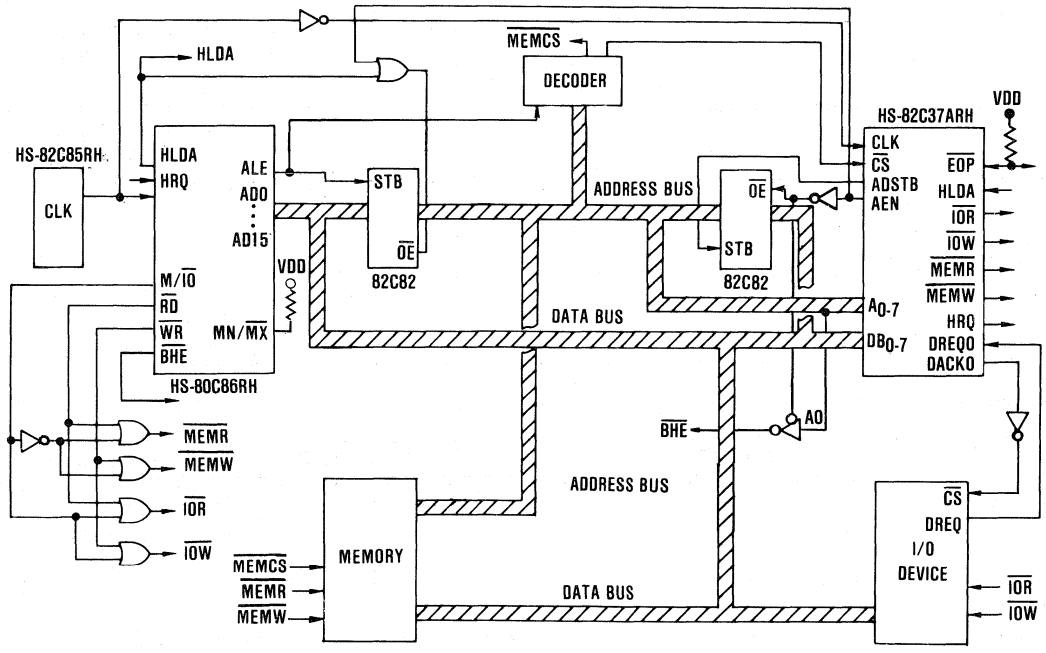


FIGURE 5. APPLICATION FOR DMA SYSTEM

Absolute Maximum Ratings

Supply Voltage ..... +7.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.5V to VCC +0.5V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications

VDD = 5.0V ±10%, TA = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	VDD -1.5V		V	
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Output High Voltage	3.0 VDD -0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	+1.0	μA	VIN = GND or VDD pins 11, 12, 13, 6, 7, 16-19
IO	I/O and Output Leakage Current	-10.0	+10.0	μA	VO = GND or VDD pins 21-23, 26-30, 1, 2, 36, 32-35, 37-40, 3, 4
IDDSB	Standby Power Supply Current		50	μA	VDD = 5.5V VIN = VDD or GND Outputs Open
IDDOP	Operating Power Supply Current		4.0	mA/MHz	VDD = 5.5V CLK FREQ = 5MHz VIN = VDD or GND Outputs Open

Capacitance

TA = 25°C; VDD = GND = OV; VIN = +5V or GND

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CIN*	Input Capacitance	15	pF	FREQ = 1MHz Unmeasured pins returned to GND
COUT*	Output Capacitance	15	pF	
CI/O*	I/O Capacitance	20	pF	

* Guaranteed, but not tested.

A.C. Specifications

VCC = +5V ±10%, GND = 0V, TA = -55°C to +125°C

DMA (Master) Mode

SYMBOL	PARAMETER	HS-82C37ARH MIN	HS-82C37ARH MAX	UNITS
TCLAEH	AEN HIGH from CLK LOW (S1) Delay Time		175	ns
TCHAEL	AEN LOW from CLK HIGH (SI) Delay Time		130	ns
TCHAZ	ADR Active to Float Delay from CLK HIGH *		90	ns
TCHRWZ	$\overline{READ}$ or $\overline{WRITE}$ Float Delay from CLK HIGH *		120	ns
TCHDZ	DB Active to Float Delay from CLK HIGH *		170	ns
TRHAX	ADR from $\overline{READ}$ HIGH Hold Time	TCLCL-100		ns
TSLDZ	DB from ADSTB LOW Hold Time	TCLCH-18		ns
TWHAX	ADR from $\overline{WRITE}$ HIGH Hold Time	TCLCL-50		ns
TCLDAV	DACK Valid from CLK LOW Delay Time		170	ns
TCHIPH	$\overline{EOP}$ HIGH from CLK HIGH Delay Time		170	ns
TCHIPL	$\overline{EOP}$ LOW from CLK HIGH Delay Time		100	ns
TCHAV	ADR Stable from CLK HIGH		110	ns
TDVSL	DB to ADSTB LOW Setup Time	TCHCL +10		ns
TCHCL	Clock HIGH Time (Transitions 10ns)	70		ns
TCLCH	Clock LOW Time (Transitions 10ns)	50		ns
TCLCL	CLK Cycle Time	200		ns
TCHRWL	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay		190	ns
TCHRH	$\overline{READ}$ HIGH from CLK HIGH (S4) Delay Time		190	ns
TCHWH	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay Time		130	ns
TCHRQV	HRQ Valid from CLK HIGH Delay Time		120	ns
TEPLCL	$\overline{EOP}$ LOW to CLK LOW Setup Time	40		ns
TEPLEPH	$\overline{EOP}$ Pulse Width	220		ns
TCHRWV	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH		150	ns
TCHDV	DB Float to Active Delay from CLK HIGH		110	ns
TRAVCH	HLDA Valid to CLK HIGH Setup Time	75		ns
TMRHDX	Input Data from $\overline{MEMR}$ HIGH Hold Time	0		ns
TDVMRH	Input Data to $\overline{MEMR}$ HIGH Setup Time	155		ns
TMWHDZ	Output Data from $\overline{MEMW}$ HIGH HOLD Time	15		ns
TDVMWH	Output Data Valid to $\overline{MEMW}$ HIGH	TCLCL-35		ns
TDQVCL	DREQ to CLK LOW (SI, S4) Setup Time	0		ns
TCLRYX	CLK LOW to READY Hold Time	20		ns
TRYVCL	READY to CLK LOW Setup Time	60		ns
TCLSH	ADSTB HIGH from CLK LOW Delay Time		80	ns
TCLSL	ADSTB LOW from CLK LOW Delay Time		120	ns

NOTE: $\overline{READ}$ refers to both $\overline{IOR}$ and $\overline{MEMR}$ outputs, and $\overline{WRITE}$ refers to both $\overline{IOW}$ and $\overline{MEMW}$ outputs, during memory to I/O and I/O to memory transfers.

A.C. Specifications

DMA Master Mode

SYMBOL	PARAMETER	HS-82C37ARH MIN	HS-82C37ARH MAX	UNITS
TWHRH	$\overline{\text{READ}}$ HIGH Delay from $\overline{\text{WRITE}}$ HIGH	0		ns
TRLRH1	$\overline{\text{READ}}$ Pulse Width, Normal Timing	2TCLCL -50		ns
TSHSL	ADSTB Pulse Width	TCLCL -80		ns
TWLWH1	Extended $\overline{\text{WRITE}}$ Pulse Width	2TCLCL -100		ns
TWLWH2	$\overline{\text{WRITE}}$ Pulse Width	TCLCL -100		ns
TRLRH2	$\overline{\text{READ}}$ Pulse Width, Compressed	TCLCL -50		ns
Peripheral (Slave) Mode	NOTE: $\overline{\text{READ}}$ refers to both $\overline{\text{IOR}}$ and $\overline{\text{MEMR}}$, and $\overline{\text{WRITE}}$ refers to both $\overline{\text{IOW}}$ and $\overline{\text{MEMW}}$, during memory to I/O and I/O to memory transfers.			
TAVIRL	ADR Valid or $\overline{\text{CS}}$ LOW to $\overline{\text{IOR}}$ LOW	10		ns
TAVIWL	ADR Valid or $\overline{\text{CS}}$ LOW to $\overline{\text{IOW}}$ LOW Setup Time	0		ns
TDVIWH	Data Valid to $\overline{\text{IOW}}$ HIGH Setup Time	150		ns
TIRHAX	ADR or $\overline{\text{CS}}$ Hold from $\overline{\text{IOR}}$ HIGH	0		ns
TIRLDV	Data Access from $\overline{\text{IOR}}$		150	ns
TIRHDZ	DB Float Delay from $\overline{\text{IOR}}$ HIGH *	10	85	ns
TPHRSL	Power Supply HIGH to RESET LOW Setup Time *	500		ns
TRSLIRWL	RESET to First $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$	2TCLCL		ns
TRSHRSL	RESET Pulse Width	300		ns
TIRLIRH	$\overline{\text{IOR}}$ Width	200		ns
TIWHAX	ADR or $\overline{\text{CS}}$ HIGH from $\overline{\text{IOW}}$ HIGH Hold Time	0		ns
TIWHDX	Data from $\overline{\text{IOW}}$ HIGH Hold Time	10		ns
TIWLIWH	$\overline{\text{IOW}}$ Width	150		ns

* Guaranteed, but not 100% tested.

Waveforms

(Slave) Mode Write Timing

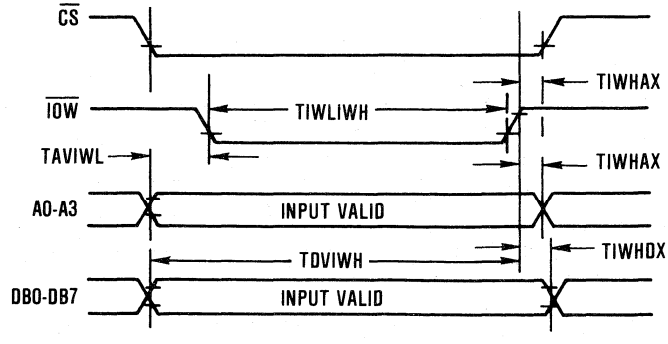
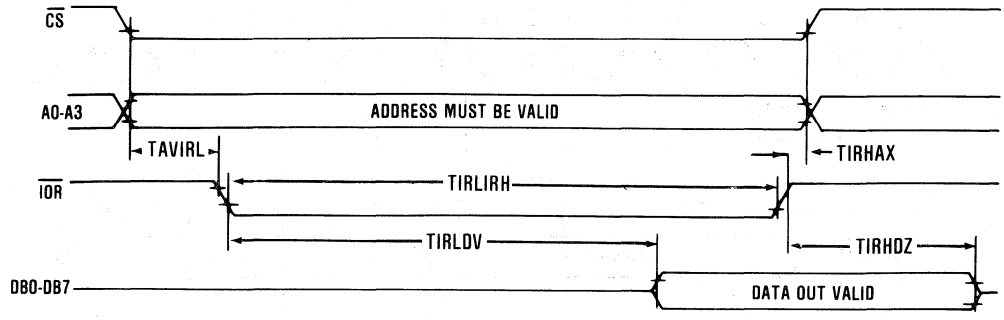


FIGURE 6. SLAVE MODE TIMING

NOTE: Host system must allow at least TCLCL as recovery time between successive write accesses.

Waveforms

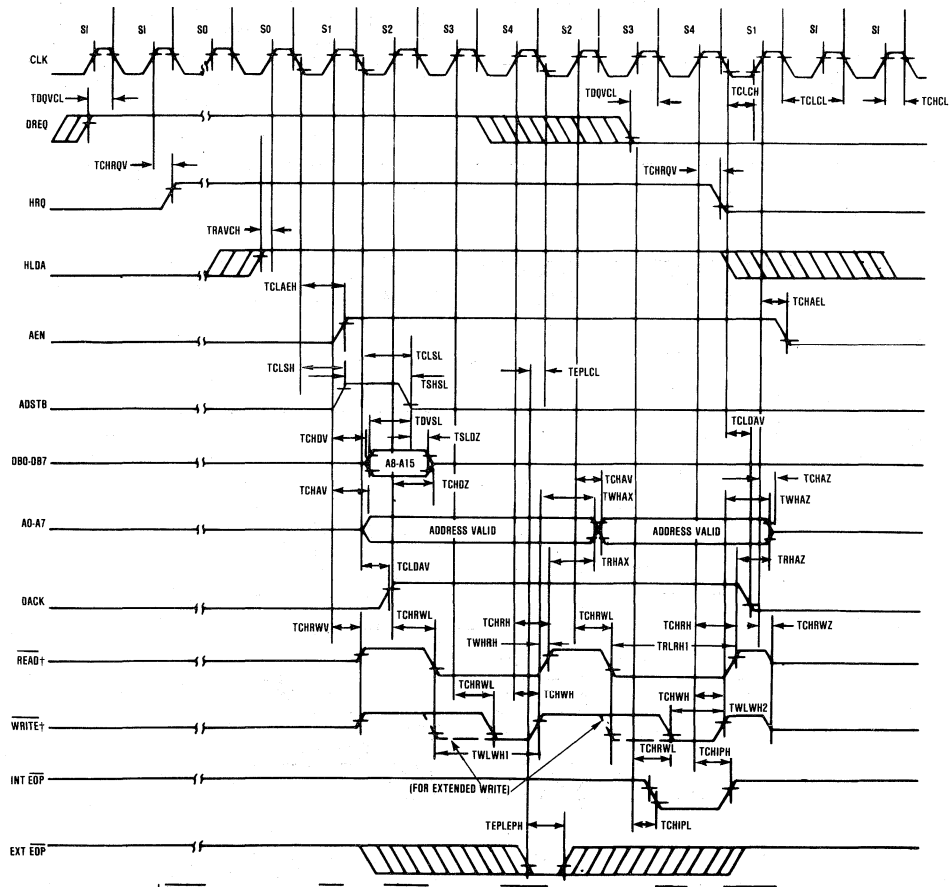
Slave Mode Read Timing



NOTE: Host system must allow at least TCLCL as recovery time between successive read accesses.

FIGURE 7. SLAVE MODE READ

DMA Transfer Timing



†READ refers to both IOR and MEMR outputs; WRITE refers to both IOW and MEMW outputs.

FIGURE 8. DMA TRANSFER

Waveforms

Memory-to-Memory Transfer Timing

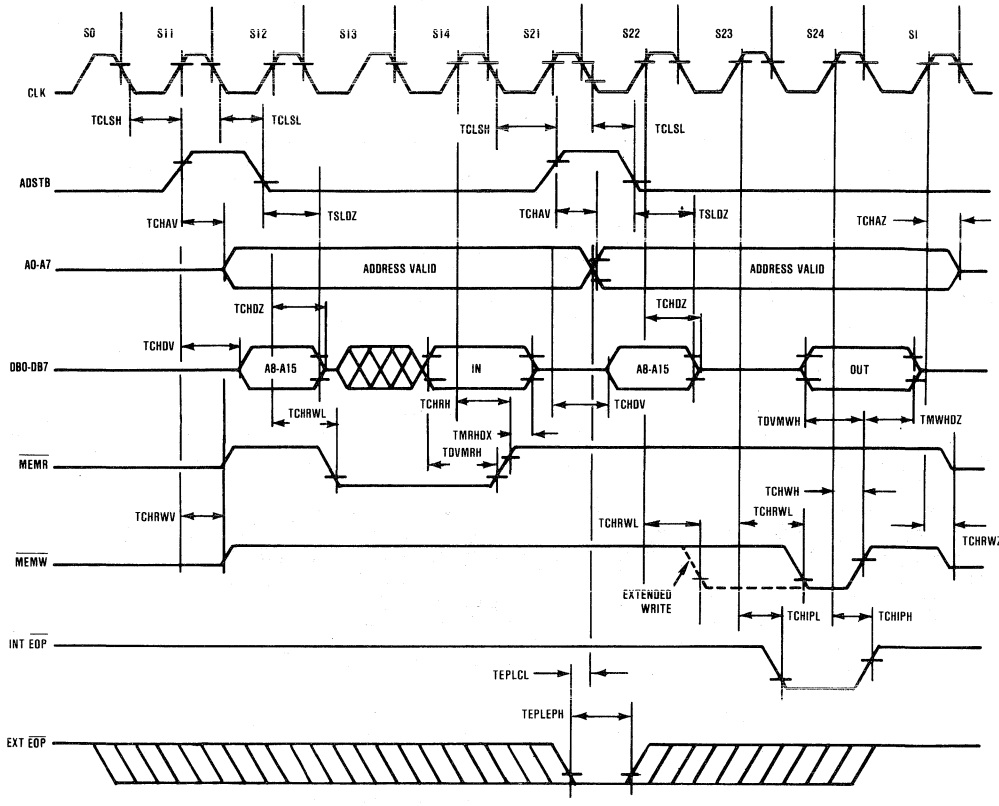
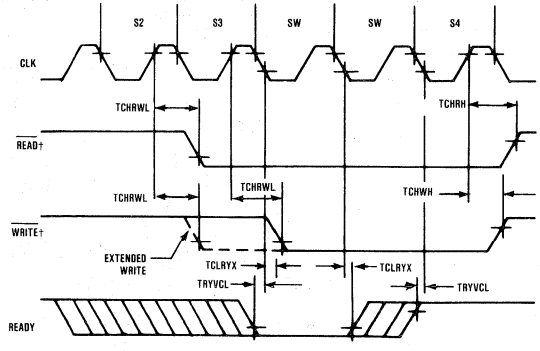


FIGURE 9. MEMORY-TO-MEMORY TRANSFER

Ready Timing

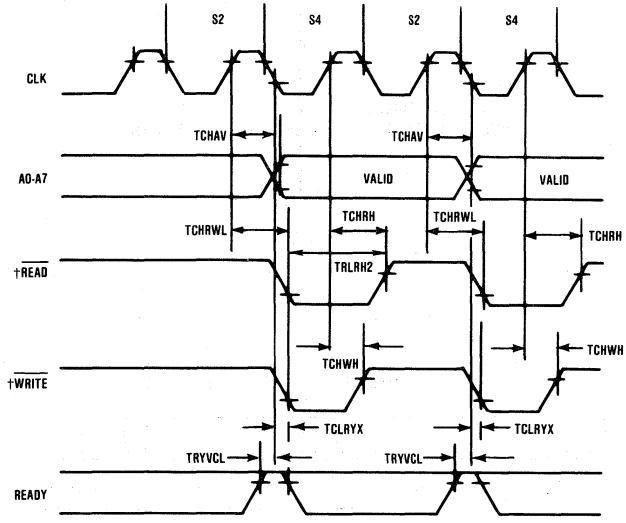


†$\overline{\text{READ}}$ refers to both $\overline{\text{IOR}}$ and $\overline{\text{MEMR}}$ outputs; $\overline{\text{WRITE}}$ refers to both $\overline{\text{IOW}}$ and $\overline{\text{MEMW}}$ outputs.

FIGURE 10. READY

Waveforms

Compressed Transfer Timing



†$\overline{\text{READ}}$ refers to both $\overline{\text{IOR}}$ and $\overline{\text{MEMR}}$ outputs; $\overline{\text{WRITE}}$ refers to both $\overline{\text{IOW}}$ and $\overline{\text{MEMW}}$ outputs.

FIGURE 11. COMPRESSED TRANSFER

Reset Timing

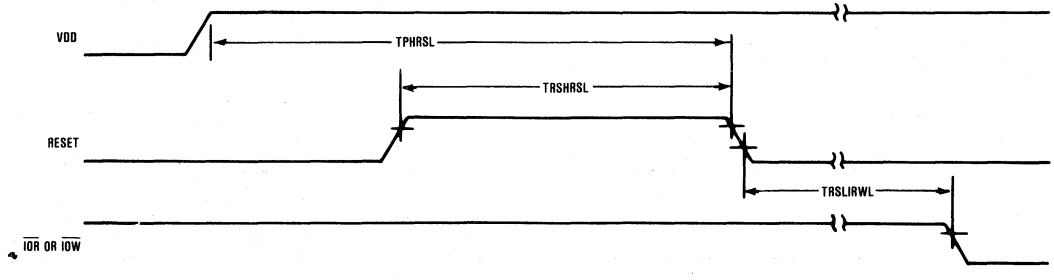
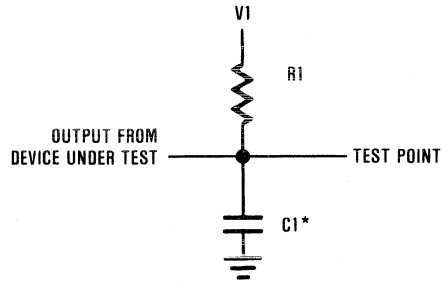


FIGURE 12. RESET

A.C. Test Circuits

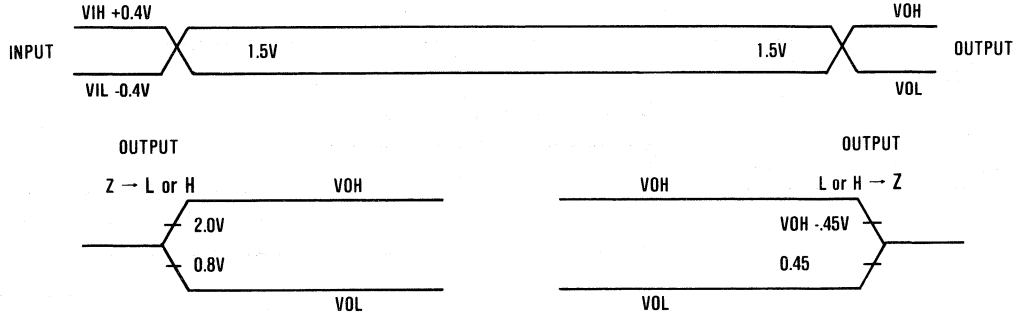


*Includes Stray and Jig Capacitance

TEST CONDITION DEFINITION TABLE

PINS	V1	R1	C1
All Outputs Except EOP	1.7V	510Ω	100pF
EOP	V_{DD}	1.6KΩ	50pF

A.C. Testing Input, Output Waveforms



A.C. Testing: All A.C. Parameters tested as per test circuits. Input RISE and FALL times are driven at 1ns/V.

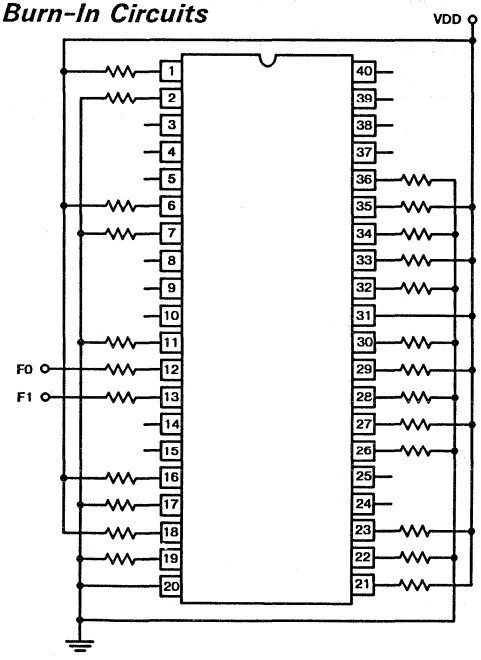
Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad(Si) ±10% from a Gamma Cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = +5.5V. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The sample devices shall be tested within one hour after irradiation. The wafers are accepted only if the sample, exclusive of nonradiation failures, meets all electrical specifications at room temperature.

Radiation Effects

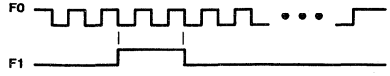
1. TOTAL DOSE:
   No degradation of any parameter will be seen at 1 x 10^5 Rad(Si). Minimal (10%) increases in **static** supply current due to leakages will begin to appear between 1 x 10^5 Rad(Si) and 5 x 10^5 Rad(Si), increasing to 50% after exposure to 1 x 10^6 Rad(Si), although the device will remain functional within specifications.
2. DOSE RATE:
   The HS-83C37ARH is manufactured on EPI material and is consequently latch-up free. Transient upset can be expected at dose rates higher than 1 x 10^9 Rad(Si)/sec.
3. SINGLE EVENT UPSET:
   The HS-82C37ARH is manufactured on EPI material and is consequently latch-up free. Preliminary testing has shown the device has a LET threshold of 24MeV/mg/cm^2.

Burn-In Circuits



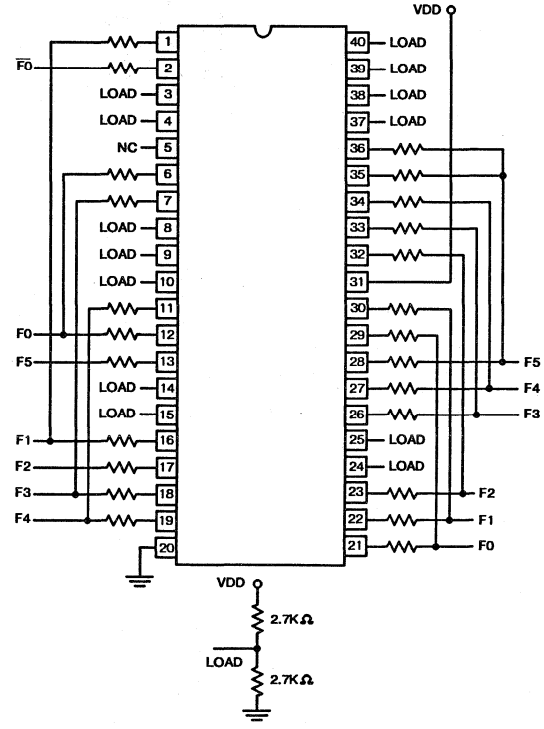
STATIC CONFIGURATION

VDD = +6.0V ± 5% Part is Static Sensitive
TA = 125°C Minimum Voltage Must Be Ramped
Resistors: R1 = 10kΩ ± 10% (Pins 6, 7, 11-13, 16-19)
R2 = 2.7kΩ ± 5% (Pins 1, 2, 21-23, 26-30, 32-36)



START-UP TIMING

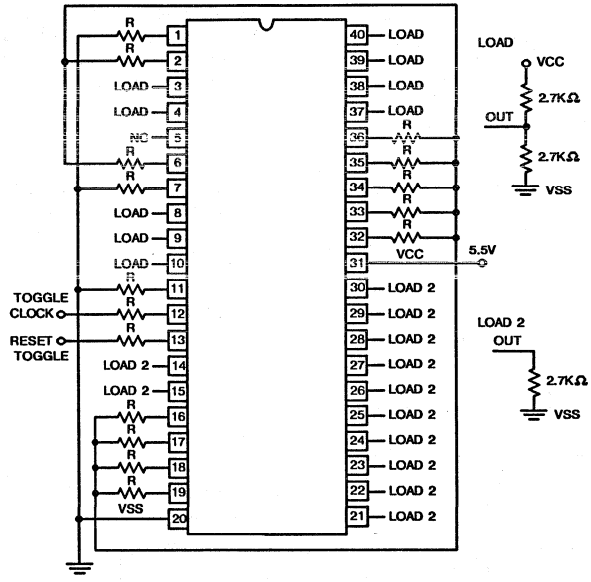
F0 is 50% duty cycle square wave pulse burst.
1.0kHz < = F0 < = 100kHz F0 is left High after pulse burst.
10 cycles < = F0 Pulse Burst < = 1.0 sec.
F1 = Single pulse with width equal to 2 cycles of F0.
F1 is left Low after pulse burst.
NOTE: F1 pulse occurs after start of F0 and ends before F0.
Input levels: 0.9VDD < = VIH < = VDD, -0.3V < = VIL < = 0.7V



DYNAMIC CONFIGURATION

VDD = 6.0V ± 5% (Burn-In)
VDD = 6.0V ± 5% (Life Test)
TA = 125°C Minimum
Part is Static Sensitive, Voltage Must Be Ramped
Resistors: R1 = 10kΩ ± 10% (Pins 6, 7, 11-13, 16-19)
R2 = 2.7kΩ ± 10% (Pins 1, 2, 21-23, 26-30, 32-36, and LOADS)

Irradiation Circuit



R = 47kΩ
Pins With Load: 3, 4, 8, 9, 10, 37-40
Pins With Load2: 14, 15, 21-30
Pins Brought Out: 12 (Clock), 13 (Reset)

HARRIS

HS-82C54RH

Radiation Hardened CMOS Programmable Interval Timer

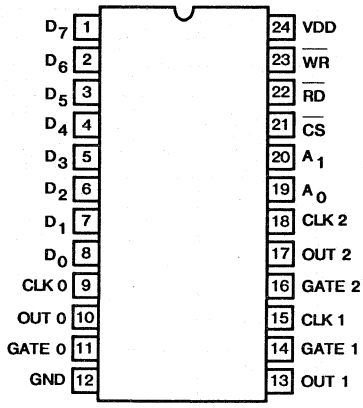
July 1990

Features

- Radiation Hardened
  - Total Dose ..... $> 10^5$ RAD(Si)
  - Transient Upset ..... $> 10^8$ RAD(Si)/sec
  - Latch Up Free EPI-CMOS
  - Functional After Total Dose ..... 1×10^6 RAD(Si)
- Low Power Consumption
  - IDDSB = 20mA
  - IDDOP = 12mA
- Pin Compatible with NMOS 8254 and the Harris 82C54
- High Speed, "No Wait State" Operation with 5MHz HS-80C86RH
- Three Independent 16-Bit Counters
- Six Programmable Counter Modes
- Binary or BCD Counting
- Status Read Back Command
- Fully TTL Compatible
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- Military Temperature Range ..... -55°C to +125°C

Pinout

DIP
TOP VIEW

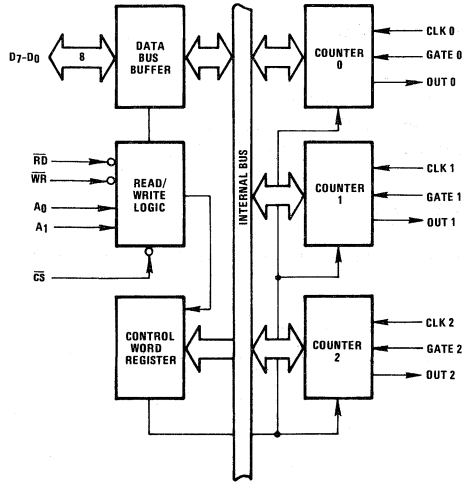


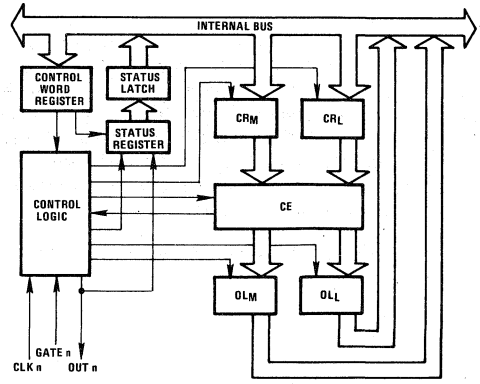
Description

The Harris HS-82C54RH is a high performance, radiation hardened CMOS version of the industry standard 8254 and is manufactured using a hardened field, self-aligned silicon gate CMOS process. It has three independently programmable and functional 16-bit counters, each capable of handling clock input frequencies of up to 5MHz. Six programmable timer modes allow the HS-82C54RH to be used as an event counter, elapsed time indicator, a programmable one-shot, or for any other timing application. The high performance, radiation hardness, and industry standard configuration of the HS-82C54RH make it compatible with the HS-80C86RH radiation hardened microprocessor.

Static CMOS circuit design insures low operating power. The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Functional Diagram





CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
D_7-D_0	1-8	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
OUT 1	13	O	OUT 1: Output of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 2	16	I	GATE 2: Gate input of Counter 2.
OUT 2	17	O	OUT 2: Output of Counter 2.
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.
A_0, A_1	19-20	I	ADDRESS: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus. A_1 A_0 Selects 0 0 Counter 0 0 1 Counter 1 1 0 Counter 2 1 1 Control Word Register
$\overline{CS}$	21	I	CHIP SELECT: A low on this input enables the HS-82C54RH to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	READ: This input is low during CPU read operations.
$\overline{WR}$	23	I	WRITE: This input is low during CPU write operations.
VDD	24		VDD: The +5V power supply pin. A 0.1μF capacitor between pins 12 and 24 is recommended for decoupling.

Functional Description

General

The HS-82C54RH is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The HS-82C54RH solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the HS-82C54RH to match his requirements and programs one of the counters for the desired delay. After the desired delay, the HS-82C54RH will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other timer functions common to microcomputers which can be implemented with the HS-82C54RH are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This three-state, bi-directional, 8-bit buffer is used to interface the HS-82C54RH to the system bus (see Figure 1).

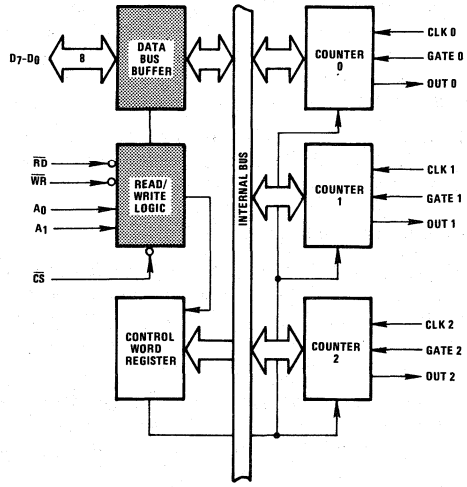


FIGURE 1. DATA BUS BUFFER AND READ/WRITE LOGIC FUNCTION

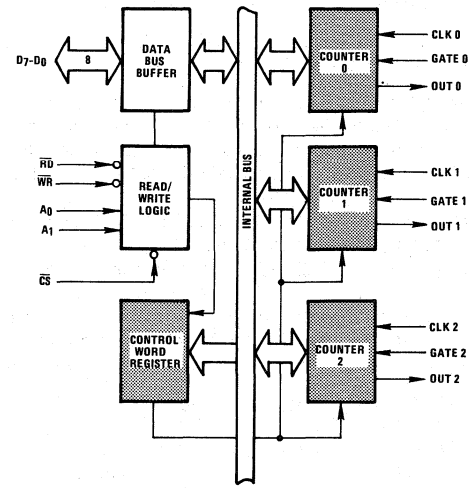


FIGURE 2. CONTROL WORD REGISTER AND COUNTER FUNCTIONS

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the HS-82C54RH. A_1 and A_0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the HS-82C54RH that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the HS-82C54RH that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the HS-82C54RH has been selected by holding $\overline{CS}$ low.

Control Word Register

The Control Word Register (Figure 2) is selected by the Read/Write Logic when $A_1, A_0 = 11$. If the CPU then does a write operation to the HS-82C54RH, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

Counter 0, Counter 1, Counter 2

These three functional clocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 3. The counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

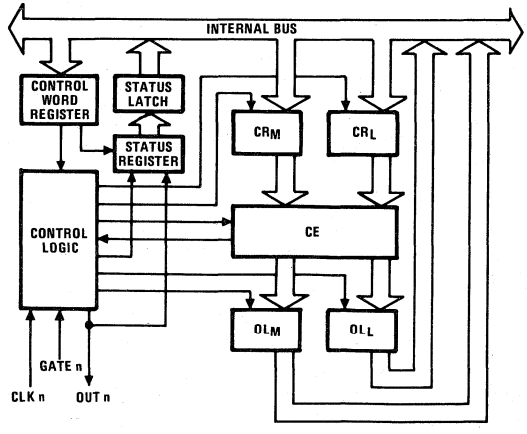


FIGURE 3. COUNTER INTERNAL BLOCK DIAGRAM

The Status Register, shown in the figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back Command.)

The actual counter is labeled CE for "Counting Element". It is a 16-bit presettable synchronous down counter.

OL_M and OL_L are two 8-bit latches. OL stands for "Output Latch", subscripts M and L for "Most significant byte" and "Least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the HS-82C54RH, the OL latches the present count until read by the CPU and then returns to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CR_M and CR_L (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR_M and CR_L are cleared when the Counter is programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

HS-82C54RH System Interface

The HS-82C54RH is treated by the system software as an array of peripheral I/O ports; three are Counters and the fourth is a Control Word Register for MODE programming.

Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder, such as a Harris HD-6440 for larger systems.

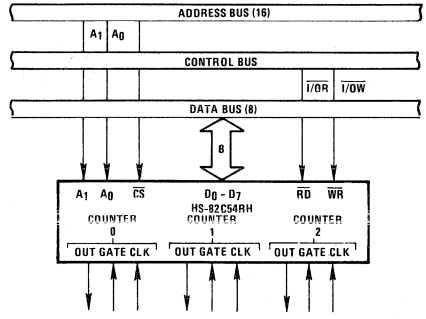


FIGURE 4. HS-82C54RH SYSTEM INTERFACE

Operational Description

General

After power-up, the state of the HS-82C54RH is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused Counters need not be programmed.

Programming The HS-82C54RH

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when $A_1, A_0 = 11$. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A_1, A_0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Write Operations

The programming procedure for the HS-82C54RH is very flexible. Only two conventions need to be remembered:

1. For each Counter, the Control Word must be written before the initial count is written.

2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A_1, A_0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

Control Word Format

A_1, A_0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW — Read/Write:

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M — Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD — Binary Coded Decimal:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

FIGURE 5. CONTROL WORD FORMAT

	A_1	A_0
Control Word — Counter 0	1	1
LSB of count — Counter 0	0	0
MSB of count — Counter 0	0	0
Control Word — Counter 1	1	1
LSB of count — Counter 1	0	1
MSB of count — Counter 1	0	1
Control Word — Counter 2	1	1
LSB of count — Counter 2	1	0
MSB of count — Counter 2	1	0

	A_1	A_0
Control Word — Counter 2	1	1
Control Word — Counter 1	1	1
Control Word — Counter 0	1	1
LSB of count — Counter 2	1	0
MSB of count — Counter 2	1	0
LSB of count — Counter 1	0	1
MSB of count — Counter 1	0	1
LSB of count — Counter 0	0	0
MSB of count — Counter 0	0	0

	A_1	A_0
Control Word — Counter 0	1	1
Control Word — Counter 1	1	1
Control Word — Counter 2	1	1
LSB of count — Counter 2	1	0
LSB of count — Counter 1	0	1
LSB of count — Counter 0	0	0
MSB of count — Counter 0	0	0
MSB of count — Counter 1	0	1
MSB of count — Counter 2	1	0

	A_1	A_0
Control Word — Counter 1	1	1
Control Word — Counter 0	1	1
LSB of count — Counter 1	0	1
Control Word — Counter 2	1	1
LSB of count — Counter 0	0	0
MSB of count — Counter 1	0	1
LSB of count — Counter 2	1	0
MSB of count — Counter 0	0	0
MSB of count — Counter 2	1	0

NOTE: In all four examples, all counters are programmed to Read/Write two-byte counts. These are only four of many possible programming sequences.

FIGURE 6. A FEW POSSIBLE PROGRAMMING SEQUENCES

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the HS-82C54RH.

There are three possible methods for reading the Counters. The first is through the Read-Back Command, which is explained later. The second is a simple read operation of the Counter, which is selected with the A_1, A_0 inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

Counter Latch Command

The other method for reading the Counters involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A_1, A_0 = 11. Also, like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D_5 and D_4, distinguish this command from a Control Word.

A_1, A_0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 — specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5, D4 — 00 designates Counter Latch Command
X — Don't Care

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

FIGURE 7. COUNTER LATCH COMMAND FORMAT

The selected Counter's Output Latch (OL) latches the count when the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the Counting Element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the HS-82C54RH is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read or write two-byte counts, the following precaution applies: A program MUST NOT transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The Read-Back Command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected Counter(s).

The command is written into the Control Word Register and has the format shown in Figure 8. The command applies to the Counters selected by setting their corresponding bits D_3, D_2, D_1 = 1.

A_0, A_1 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D_5: 0 = Latch count of selected Counters(s)
D_4: 0 = Latch status of selected Counters(s)
D_3: 1 = Select Counter 2
D_2: 1 = Select Counter 1
D_1: 1 = Select Counter 0
D_0: Reserved for future expansion; Must be 0

FIGURE 8. READ-BACK COMMAND FORMAT

The Read-Back Command may be used to latch multiple Counter Output Latches (OL) by setting the COUNT bit $D_5 = 0$ and selecting the desired Counter(s). This single command is functionally equivalent to several Counter Latch Commands, one for each Counter latched. Each Counter's latched count is held until it is read (or the Counter is reprogrammed). That Counter is automatically unlatched when read, but other Counters remain latched until they are read. If multiple count Read-Back Commands are issued to the same Counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first Read-Back Command was issued.

The Read-Back Command may also be used to latch status information of selected Counter(s) by setting STATUS bit $D_4 = 0$. Status must be latched to be read; status of a Counter is accessed by a read from that Counter.

The Counter status format is shown in Figure 9. Bits D_5 through D_0 contain the Counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D_7 contains the current state of the OUT pin. This allows the user to monitor the Counter's output via software, possibly eliminating some hardware from a system.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D_7 1 = Out Pin is 1
0 = Out pin is 0
D_6 1 = Null count
0 = Count available for reading
D_5-D_0 = Counter programmed mode (See Figure 5)

FIGURE 9. STATUS BYTE

NULL COUNT bit D_6 indicates when the last count written to the Counter Register (CR) has been loaded into the Counting Element (CE). The exact time this happens depends on the Mode of the Counter and is described in the Mode Definitions, but until the count is loaded into the Counting Element (CE), it can't be read from the Counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 10.

THIS ACTION:	CAUSES:
A. Write to the Control Word Register: (1)	Null Count = 1
B. Write to the Count Register (CR): (2)	Null Count = 1
C. New count is loaded into CE (CR → CE):	Null Count = 0

(1) Only the Counter specified by the Control Word will have its Null Count set to 1. Null Count bits of other Counters are unaffected.

(2) If the Counter is programmed for two-byte counts (least significant byte then most significant byte) Null Count goes to 1 when the second byte is written.

FIGURE 10. NULL COUNT OPERATION

If multiple status latch operations of the Counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the Counter at the time the first status Read-Back Command was issued.

Both count and status of the selected Counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D_5, $D_4 = 0$. This is functionally the same as issuing two separate Read-Back Commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status Read-Back Commands are issued to the same Counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 11.

If both count and status of a Counter are latched, the first read operation of that Counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the Counter is programmed for one or two byte counts) return latched count. Subsequent reads return unlatched count.

COMMAND									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DESCRIPTION	RESULT
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read-back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read-back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read-back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read-back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	1	0	0	Read-back status of Counter 1	Command ignored, status already latched for Counter 1

FIGURE 11. READ-BACK COMMAND EXAMPLE

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (Three-State)
1	X	X	X	X	No-Operation (Three-State)
0	1	1	X	X	No-Operation (Three-State)

FIGURE 12. READ/WRITE OPERATIONS SUMMARY

Mode Definitions

The following are defined for use in describing the operation of the HS-82C54RH.

CLK PULSE:

A rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER:

A rising edge of a Counter's Gate input.

COUNTER LOADING:

The transfer of a count from the CR to the CE (See "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1- Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).

2- Writing the second byte allows the new count to be loaded on next CLK pulse.

This allows the counting sequence to be synchronized by software. Again OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.

Mode 1: Hardware Retriggerable One-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the Counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

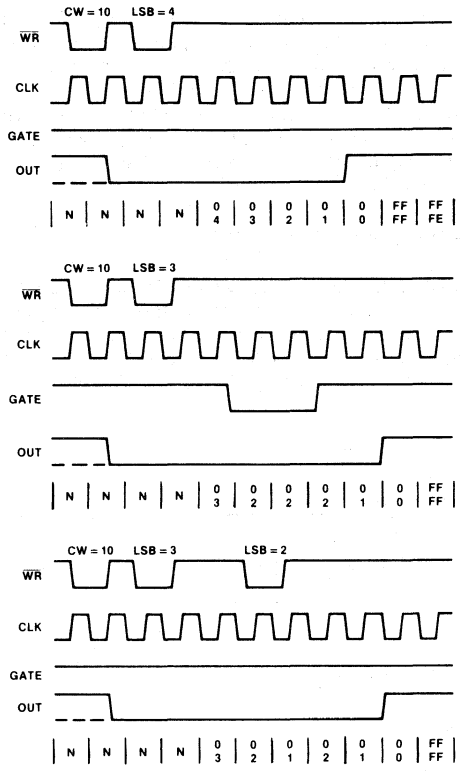
Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle.



NOTE: The following conventions apply to all mode timing diagrams.

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 13. MODE 0

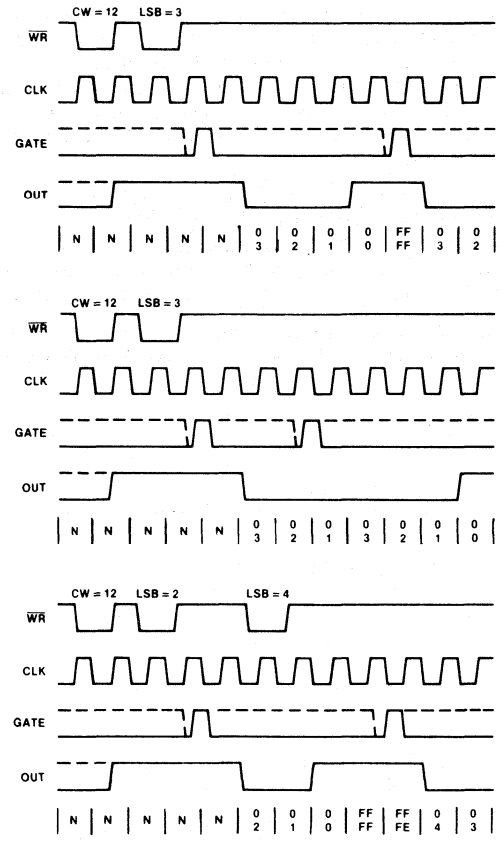


FIGURE 14. MODE 1

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

EVEN COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

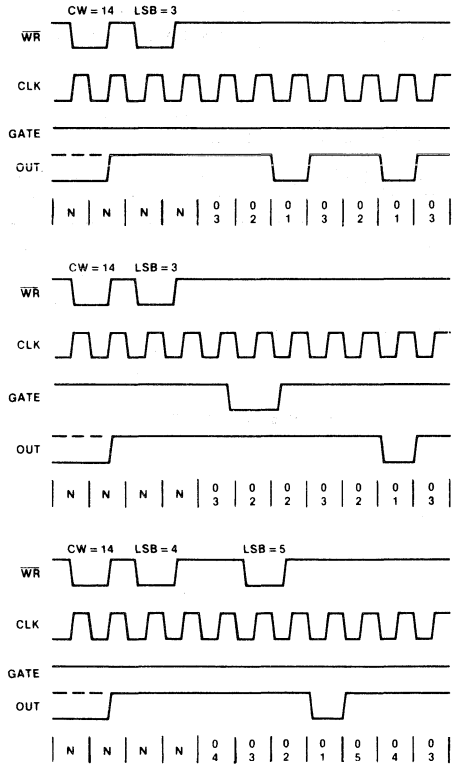


FIGURE 15. MODE 2

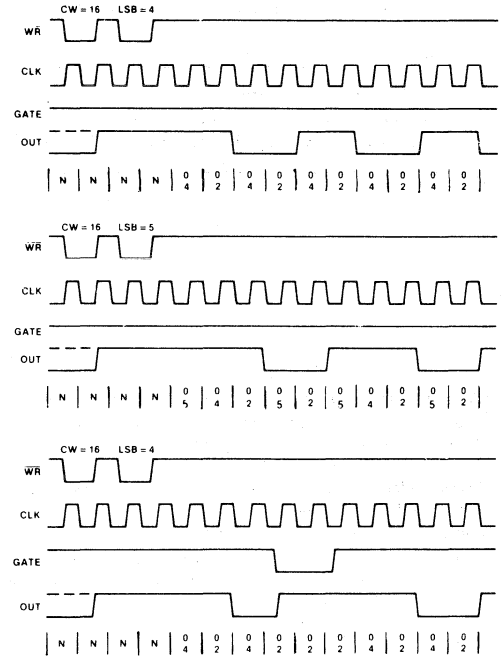


FIGURE 16. MODE 3

ODD COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse, decremented by one on the next CLK pulse, and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the Counter is reloaded with the initial count. The count is decremented by three on the next CLK pulse, and then by two on succeeding CLK pulses. When the count expires, OUT goes high again and the Counter is reloaded with the initial count. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Mode 4: Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse then go high again. The counting sequence is "Triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte has no effect on counting.
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

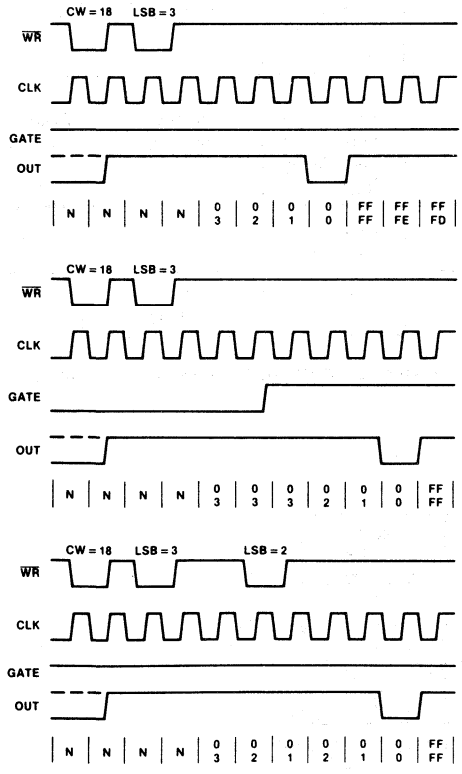


FIGURE 17. MODE 4

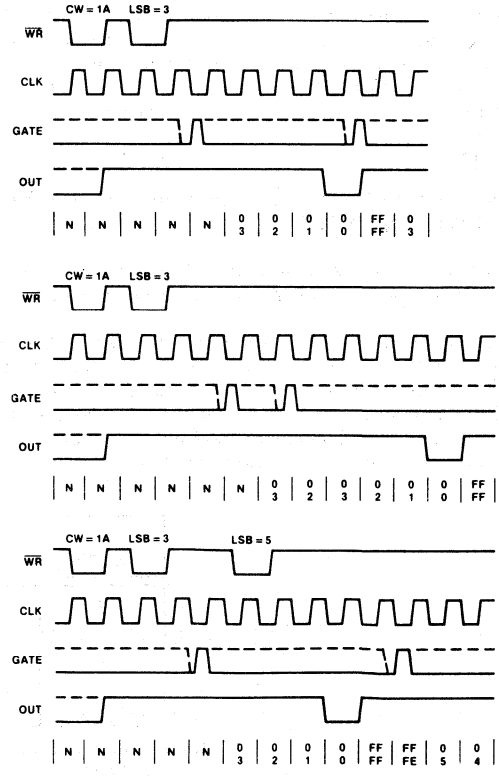


FIGURE 18. MODE 5

After writing the Control Word and initial count, the Counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. This allows the counting sequence to be retrigged. OUT strobes low N + 1 CLK pulses after any new trigger. GATE has no effect on the state of OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3 and 4 the GATE input is level sensitive, and logic level is sampled on the rising edge of CLK. In modes 1, 2, 3 and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of Gate (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK. The flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs - a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge-and level-sensitive.

Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4 and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

SIGNAL STATUS MODES	LOW OR GOING LOW	RISING	HIGH
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	1) Disables counting	—	Enables counting
5	—	Initiates counting	—

FIGURE 19. GATE PIN OPERATIONS SUMMARY

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

FIGURE 20. MINIMUM AND MAXIMUM INITIAL COUNTS

Absolute Maximum Ratings

Supply Voltage.....+7.0 Volts
Operating Voltage Range.....+4.5V to +5.5V
Input, Output or I/O Voltage Applied.....GND -0.5V to VDD +0.5V
Storage Temperature Range.....-65°C to +150°C
Operating Temperature Range:.....-55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

D. C. Electrical Specifications

VDD = 5.0V ± 10%
TA = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	VDD -1.5V		V	VDD = 5.5V
VIL	Logical Zero Input Voltage		0.8	V	VDD = 4.5V
IOH	Output High Current		-2.5 -100	mA µA	VOH = 3.0V VOH = 4.1V
IOL	Output Low Current	2.5		mA	VOL = 0.4V
II	Input Leakage Current	-1.0	+1.0	µA	VIN = GND or VDD Pins 9, 11, 14-16, 18-23
IO	Output Leakage Current	-10.0	+10.0	µA	VO = GND or VDD Pins 1-8
IDDSB	Standby Power Supply Current		20	µA	VDD = 5.5V VIN = VDD or GND, Outputs Open Counters Programmed
IDDOP	Operating Power Supply Current		12	mA	VDD = 5.5V CLK 0 = CLK 1 = CLK 2 = 5MHz, Outputs Open

Capacitance

TA = 25°C; VDD = GND = 0V; VIN = +5V or GND.

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
C_{IN}*	Input Capacitance	15	pF	FREQ = 1MHz Unmeasured pins returned to GND
C_{OUT}*	Output Capacitance	15	pF	
$C_{I/O}$*	I/O Capacitance	20	pF	

*Guaranteed but not tested

A.C. Electrical Specifications

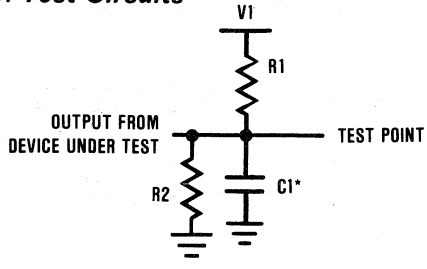
VDD = +5V ± 10%
TA = -55°C to +125°C

BUS PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
TAVRL	Address Stable Before $\overline{RD}$	75		ns	1
TSLRL	$\overline{CS}$ Stable Before $\overline{RD}$	0		ns	
TRHAX	Address Hold Time After $\overline{RD}$	0		ns	
TRLRH	$\overline{RD}$ Pulse Width	240		ns	
TRLDV	Data Delay from $\overline{RD}$		200	ns	
TRHDZ *	$\overline{RD}$ to Data Floating	8	145	ns	2
TRHRL	Command Recovery Time	320		ns	
WRITE CYCLE					
TAVWL	Address Stable Before $\overline{WR}$	0		ns	
TSLWL	$\overline{CS}$ Stable Before $\overline{WR}$	0		ns	
TWHAX	Address Hold Time After $\overline{WR}$	0		ns	
TWLWH	$\overline{WR}$ Pulse Width	240		ns	
TDVWH	Data Setup Time Before $\overline{WR}$	225		ns	
TWHDX	Data Hold Time After $\overline{WR}$	25		ns	
TWHWL	Command Recovery Time	320		ns	
CLOCK AND GATE					
TCLCL	Clock Period	200	DC	ns	1
TCHCL	High Pulse Width	100		ns	1
TCLCH	Low Pulse Width	100		ns	1
TCH1CH2*	Clock Rise Time		160	ns	
TCL1CL2*	Clock Fall Time		160	ns	
TGHGL	Gate Width High	80		ns	1
TGLGH	Gate Width Low	80		ns	
TGVCH	Gate Setup Time to CLK	80		ns	
TCHGX	Gate Hold Time After CLK	80		ns	
TCLOV	Output Delay from CLK		240	ns	
TGLOV	Output Delay from Gate		200	ns	
TAVAV	Data Delay From Address Read		275	ns	
TWHOV	Output Delay From WR High		260	ns	

*Guaranteed but not tested.

A.C. Test Circuits

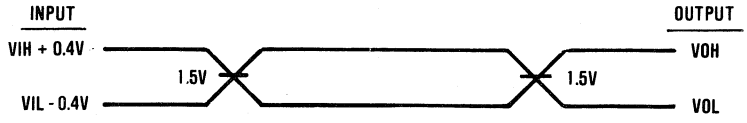


*Includes stray and jig capacitance

TEST CONDITION DEFINITION TABLE

TEST CONDITION	V1	R1	R2	C1
1	1.7V	510	OPEN	150pF
2	VDD	2K	1.8K	50pF

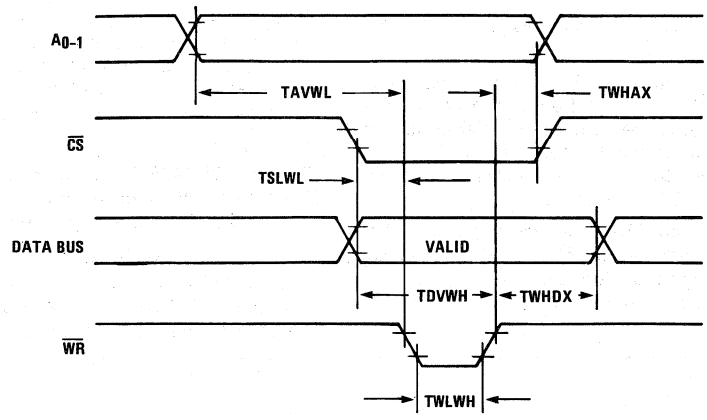
A.C. Testing Input, Output Waveform



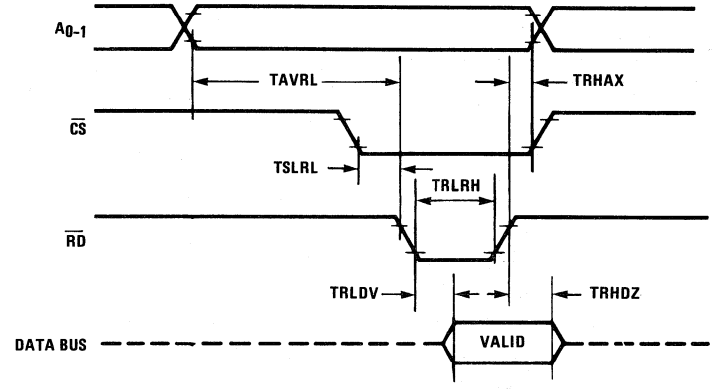
A. C. Testing: All input signals must switch between VIL -0.4V and VIH +0.4V. Input rise and fall times are driven at 1ns/V.

Waveforms

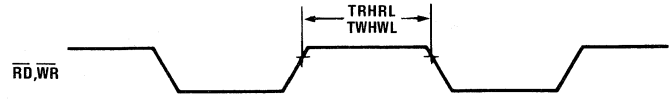
WRITE



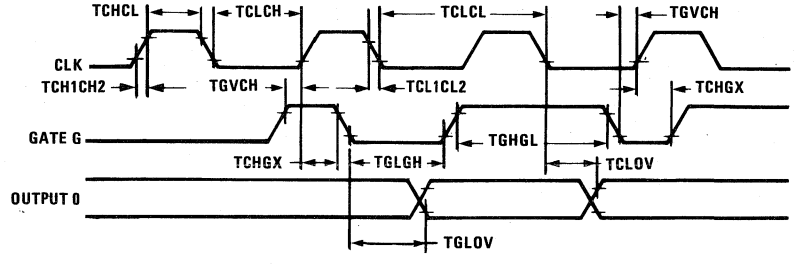
READ



RECOVERY



CLOCK AND GATE



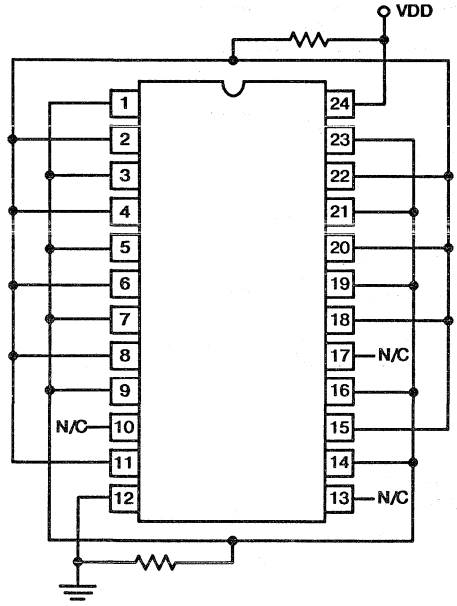
Radiation Screening Procedure

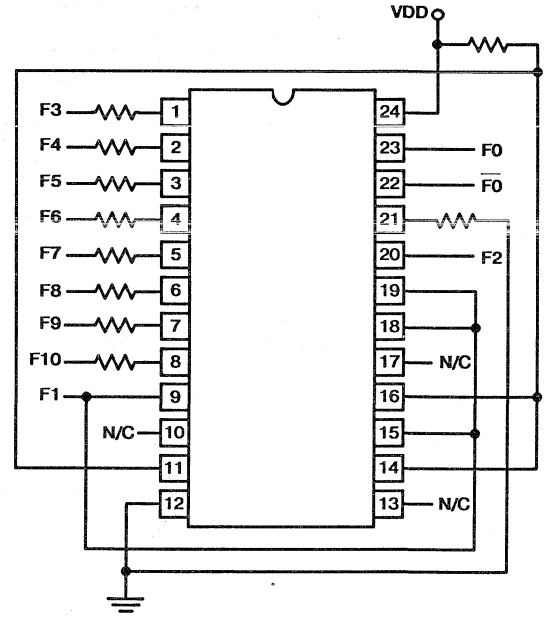
1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad(Si) ±10% from a Gammacell 220 cobalt 60 source or equivalent. The devices shall be powered in the configuration illustrated with V_{SUPPLY} + +5.5V.The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The sample devices shall be tested within one hour after irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.

Radiation Effects

1. TOTAL DOSE:
   No degradation of any parameters will be seen at 1 x 10^5 Rad(Si). Minimal (10%) increases in static supply current due to leakages will begin to appear between 1 x 10^5 Rad(Si) and 5 x 10^5 Rad(Si), increasing to 50% after exposure to 1 x 10^6 Rad(Si), although the device will remain functional within specifications.
2. DOSE RATE:
   The HS-82C54RH is manufactured on EPI material and is consequently latch-up free. Transient upset can be expected at dose rates higher than 1 x 10^9 Rad(Si)/sec.
3. SINGLE EVENT UPSET:
   The HS-82C54RH is manufactured on EPI material and is consequently latch-up free. Preliminary testing has shown the device has a LET threshold of 24MeVsmg/cm2.

Burn-In Circuits





STATIC CONFIGURATION

TA = 125°C Minimum
VDD = +6.0V ± 5%
IDD < 100µA
All Resistors 100kΩ ± 10%; 1/4W
Package: 24 Pin DIP
EQ. Package Code: 4E
Use crow bar circuit
Use 0.1F capacitor from VDD to ground each position

DYNAMIC CONFIGURATION

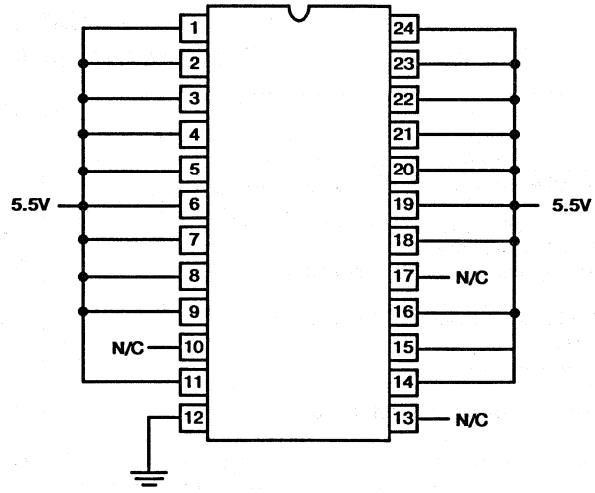
VDD = 6.0V ± 5% (Burn-In)
VDD = 5.0V ± 5% (Life Test)
TA = 125°C Minimum
IDD < 10mA
Resistors: 10kΩ ± 10%; 1/4W
Package: 24 Pin DIP
EQ. Package Code: 4E
-0.3V ≤ VIL ≤ 0.8V
VDD -1.0V ≤ VIH ≤ VDD
Inputs: Leakage: 500µA max
Levels: VIL = 0.8, VIH = 4.0

AC Specs
NOTE: F0 is complement of F0
F0 = 50kHz, ± 10%, 50% duty cycle

F1 = F0/2	F6 = F5/2
F2 = F1/2	F7 = F6/2
F3 = F2/2	F8 = F7/2
F4 = F3/2	F9 = F8/2
F5 = F4/2	F10 = F9/2

Use crow bar circuit
Use 01.µF Capacitor from VDD to ground at each position

Irradiation Circuit



V_{DD} = 5.5V ±10%, T_A = +25°C

HARRIS HS-82C55ARH

Radiation Hardened CMOS Programmable Peripheral Interface

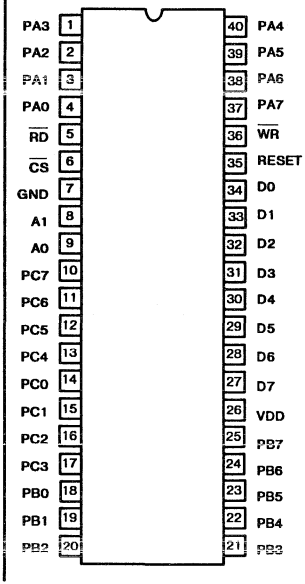
July 1990

Features

- Radiation Hardened
  - Total Dose ..... > 10^5 RAD(Si)
  - Transient Upset ..... > 10^8 RAD(Si)/sec
  - Latch Up Free EPI-CMOS
  - Functional after Total Dose..... 1 x 10^6 RAD(Si)
- Low Power Consumption ▸ IDDSB = 20μA
- Pin Compatible with NMOS 8255A and the Harris 82C55A
- High Speed, No "Wait State" Operation with 5MHz HS-80C86RH
- 24 Programmable I/O Pins
- Bus-Hold Circuitry on All I/O Ports Eliminates Pull-Up Resistors
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- Fully TTL Compatible
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- 2.5mA Drive Capability on All I/O Port Outputs
- Military Temperature Range ..... -55°C to +125°C

Pinout

DIP
TOP VIEW

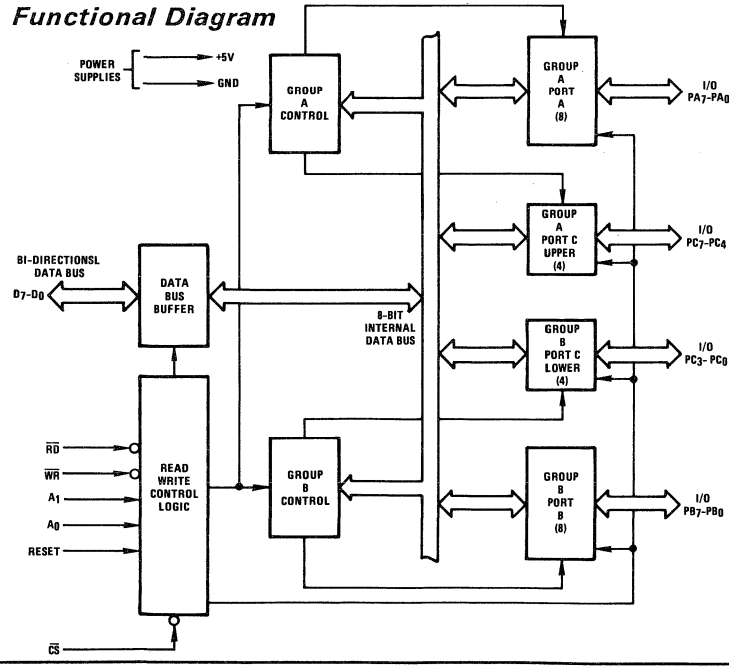


Description

The Harris HS-82C55ARH is a high performance, radiation hardened CMOS version of the industry standard 8255A and is manufactured using a hardened field, self-aligned silicon gate CMOS process. It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which are organized into two 8-bit and two 4-bit ports. Each port may be programmed to function as either an input or an output. Additionally, one of the 8-bit ports may be programmed for bi-directional operation, and the two 4-bit ports can be programmed to provide handshaking capabilities. The high performance, radiation hardness, and industry standard configuration of the HS-82C55ARH make it compatible with the HS-80C86RH radiation hardened microprocessor.

Static CMOS circuit design insures low operating power. Bus hold circuitry eliminates the need for pull-up resistors and provides TTL compatibility over the full temperature range. The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Functional Diagram



Pin Names

D7 - D0	Data Bus (Bi-Directional)
RESET	Reset Input
CS	Chip Select
RD	Read Input
WR	Write Input
A_0 - A_1	Port Address
PA_7 - PA_0	Port A (Bit)
PB_7 - PB_0	Port B (Bit)
PC_7 - PC_0	Port C (Bit)
V_{DD}	+5 Volts
GND	0 Volts

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NUMBERS	TYPE	DESCRIPTION
PA0-7	1-4, 37-40	I/O	**Port A:** General purpose I/O Port. Data direction and mode is determined by the contents of the Control Word.
PB0-7	18-25	I/O	**Port B:** General purpose I/O port. See Port A.
PC0-3	14-17	I/O	**Port C (Lower):** Combination I/O port and control port associated with Port B. See Port A.
PC4-7	10-13	I/O	**Port C (Upper):** Combination I/O Port and control port associated with Port A. See Port A.
D0-7	27-34	I/O	**Bi-Directional Data Bus:** Three-State data bus enabled as an input when $\overline{CS}$ and $\overline{WR}$ are low and as an output when $\overline{CS}$ and $\overline{RD}$ are low.
VDD	26	I	**VDD:** The +5V power supply pin. A 0.1μF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7	I	**Ground.**
$\overline{CS}$	6	I	**Chip Select:** A "low" on this input pin enables the communication between the HS-82C55ARH and the CPU.
$\overline{RD}$	5	I	**Read:** A "low" on this input pin enables the HS-82C55ARH to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the HS-82C55ARH.
$\overline{WR}$	36	I	**Write:** A "low" on this input pin enables the CPU to write data or control words into the HS-82C55ARH.
A0 and A1	8, 9	I	**Port Select 0 and Port Select 1:** These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the Least Significant Bits of the address bus (A0 and A1).
Reset	35	I	**Reset:** A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the HS-82C55ARH will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400μA.

TABLE 1.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus

TABLE 2.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control Word

TABLE 3.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	DISABLE FUNCTION
X	X	X	X	1	Data Bus → 3-State
X	X	1	1	0	Data Bus → 3-State

HS-82C55ARH Functional Description

The HS-82C55ARH is a programmable peripheral interface designed to allow microcomputer systems to control and interface with all types of peripheral devices. It has the ability to generate and respond to all asynchronous handshaking signals necessary to transfer data to and from peripheral devices, and it can also interrupt the processor when a peripheral needs servicing. These capabilities allow the HS-82C55ARH to be used in an unlimited number of applications including EXTERNAL SYSTEM CONTROL, ASYNCHRONOUS DATA TRANSFER, and SYSTEMS MONITORING.

Data Bus Buffer

This 3-state bi-directional 8-bit buffer is used to interface the HS-82C55ARH to the system data bus (See Figure 1). Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU writes a control word to the HS-82C55ARH. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the HS-82C55ARH.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group — Port A and Port C upper (C7-C4)

Control Group — Port B and Port C lower (C3-C0)

Ports A, B and C

The HS-82C55ARH contains three 8-bit ports (A, B and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the HS-82C55ARH.

Port A — One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A. See Figure 2A.

Port B — One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C — One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and can be used for the control signal outputs and status signal inputs in conjuction with Ports A and B. See Figure 2B.

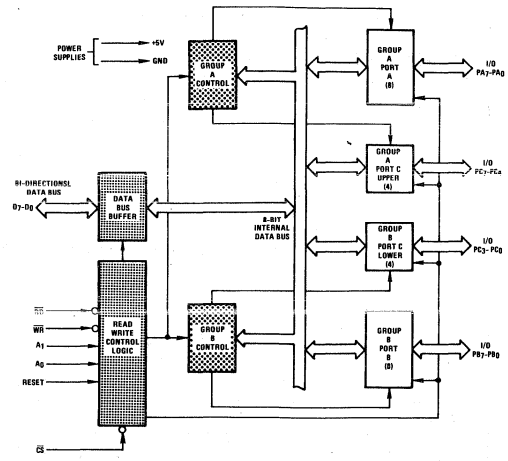


FIGURE 1. HS-82C55ARH BLOCK DIAGRAM DATA BUS BUFFER, READ/WRITE, GROUP A & B CONTROL LOGIC FUNCTIONS

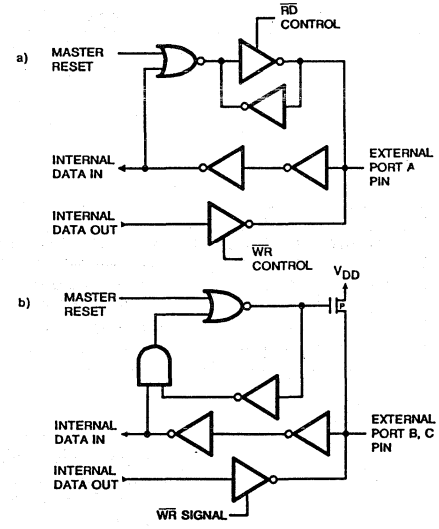


FIGURE 2. I/O PORT CONFIGURATION

HS-82C55ARH Operational Description

Control Word

The data direction and mode of Ports A, B and C are determined by the contents of the Control Word. See Figure 4. The Control Word can be both written and read as shown in Tables 1 and 2. During write operations, the function of the Control Word being written is determined by data bit D7. If D7 is high, the data on D0-D6 will be transferred into the Control Word Register. If D7 is low, the data on D0-D3 will set or reset one of the bits of Port C. See Figure 5. During Read Operations, the Control Word will always be in the format illustrated in Figure 4 with Bit D7 high to indicate Control Word Mode information.

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic Input/Output
Mode 1 — Strobed Input/Output
Mode 2 — Bi-Directional Bus

When the RESET input goes "high", all ports will be set to the input mode with all 24 port lines held at the logic "one" level by internal bus hold devices. After reset, the HS-82C55ARH can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown resistors in all-CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single HS-82C55ARH to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status register, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape recorder on an interrupt-driven basis.

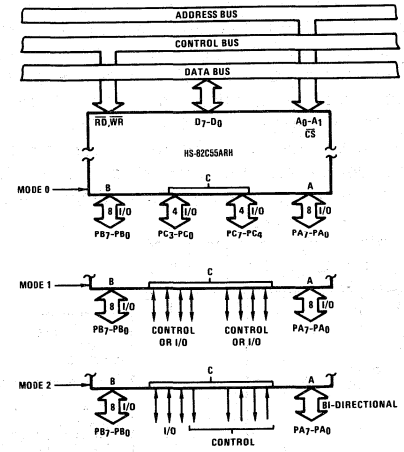


FIGURE 3. BASIC MODE DEFINITIONS AND BUS INTERFACE

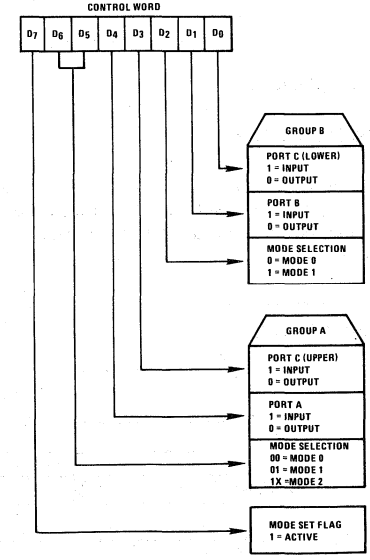


FIGURE 4. MODE SET CONTROL WORD FORMAT

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the HS-82C55ARH has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

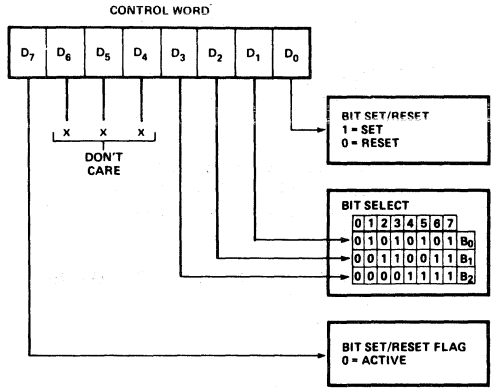


FIGURE 5. BIT SET/RESET CONTROL WORD FORMAT

Single Bit Set/Reset Feauture

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. See Figure 5. This feature reduces software requirements in control-based applications.

Interrupt Control Functions

When the HS-82C55ARH is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit Set/Reset function of Port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition:

(BIT-SET) — INTE is SET — Interrupt enable.

(BIT-RESET) — INTE is RESET — Interrupt disable.

NOTE: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

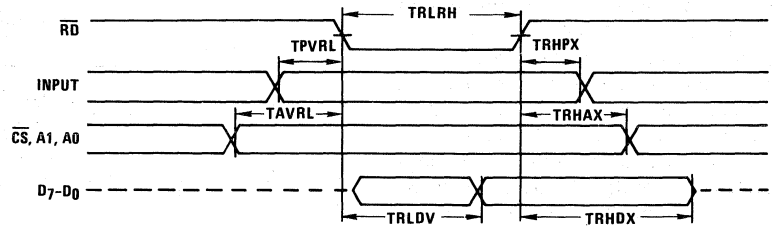
Mode O (Basic Input/Output)

This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

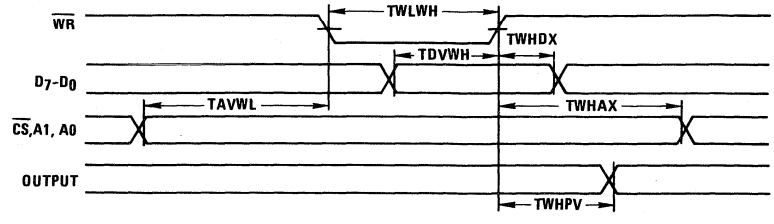
Mode O Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible

MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)

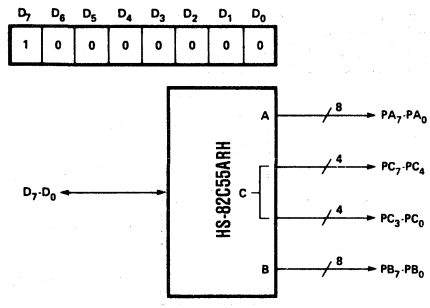


MODE 0 Port Definition

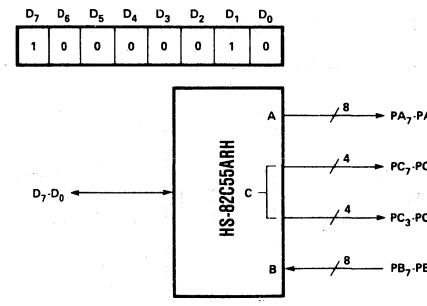
A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (UPPER)	NO.	PORT B	PORT C (LOWER)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

MODE 0 Configurations

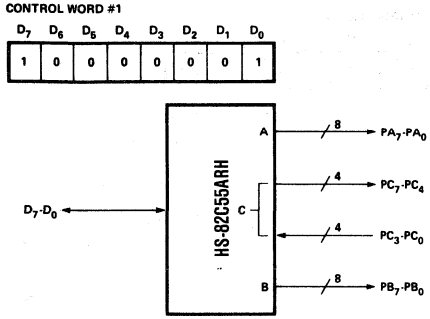
CONTROL WORD #0



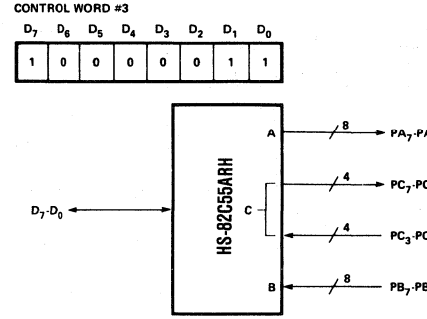
CONTROL WORD #2



CONTROL WORD #1

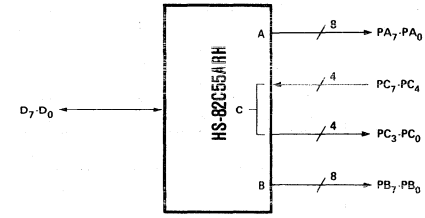


CONTROL WORD #3



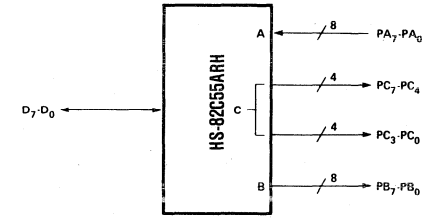
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



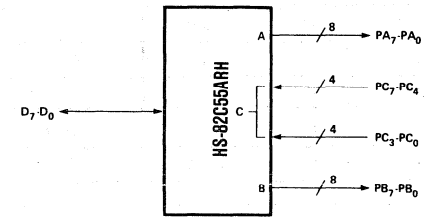
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



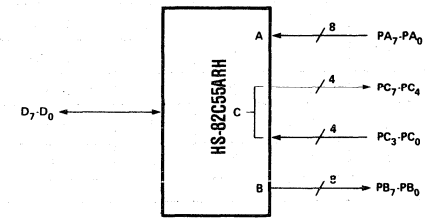
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



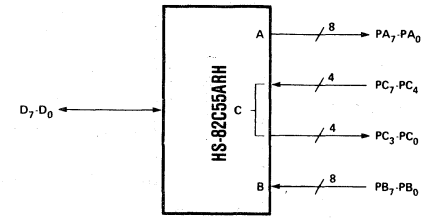
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



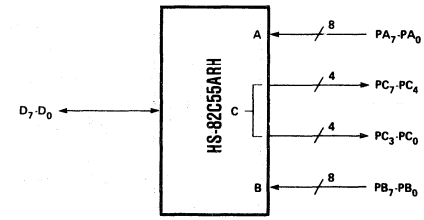
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



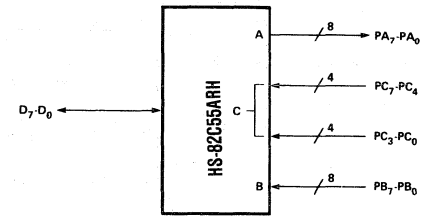
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



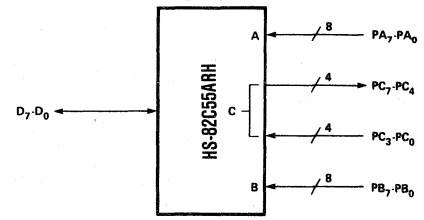
CONTROL WORD #7

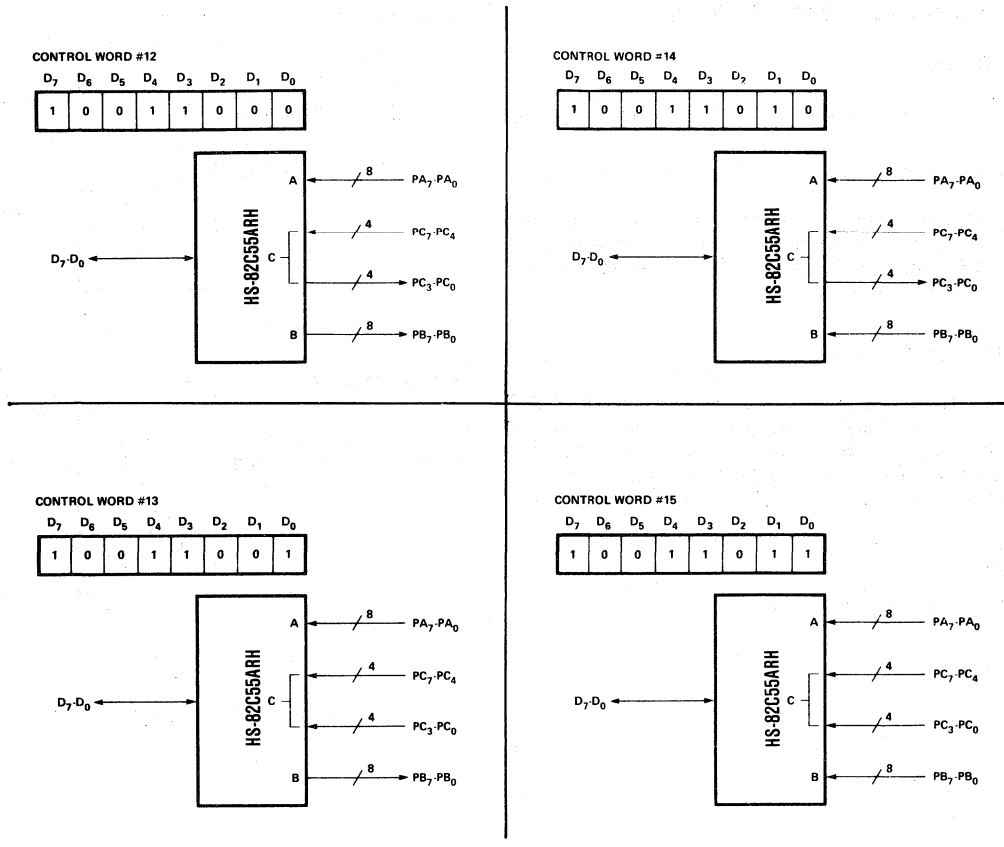
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1





Operating Modes

Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the rising edge of $\overline{STB}$ and reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by Bit Set/Reset of PC_4.

INTE B

Controlled by Bit Set/Reset of PC_2.

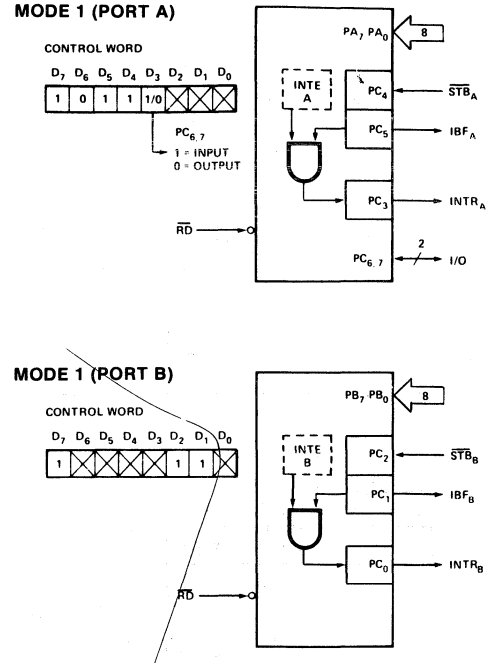


FIGURE 6. MODE 1 INPUT

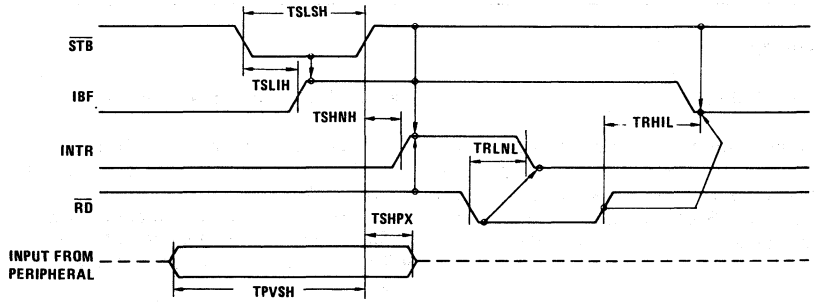


FIGURE 7. MODE 1 (STROBED INPUT)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. This does not mean valid data is sent out of the port at this time since $\overline{OBF}$ can go true before data is available. Data is guaranteed valid at the rising edge of $\overline{OBF}$. See Note 1. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input)

A "low" on this input informs the HS-82C55ARH that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data. See Note 1.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set by the rising edge of $\overline{ACK}$ and reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC_6.

INTE B

Controlled by Bit Set/Reset of PC_2.

NOTE: 1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device, generate an $\overline{ACK}$ from the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.

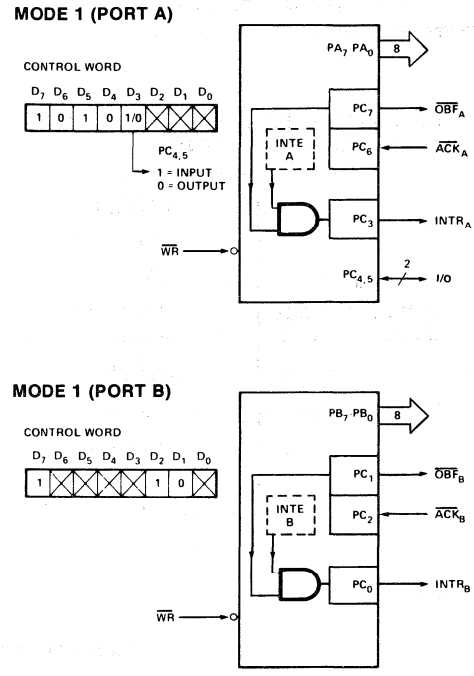


FIGURE 8. MODE 1 OUTPUT

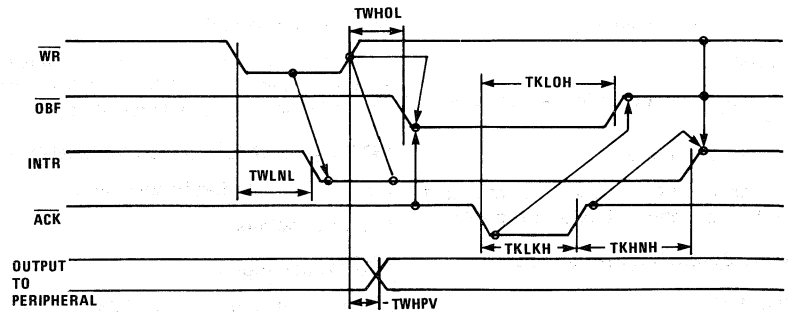


FIGURE 9. MODE 1 (STROBED OUTPUT)

Combinations of MODE 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

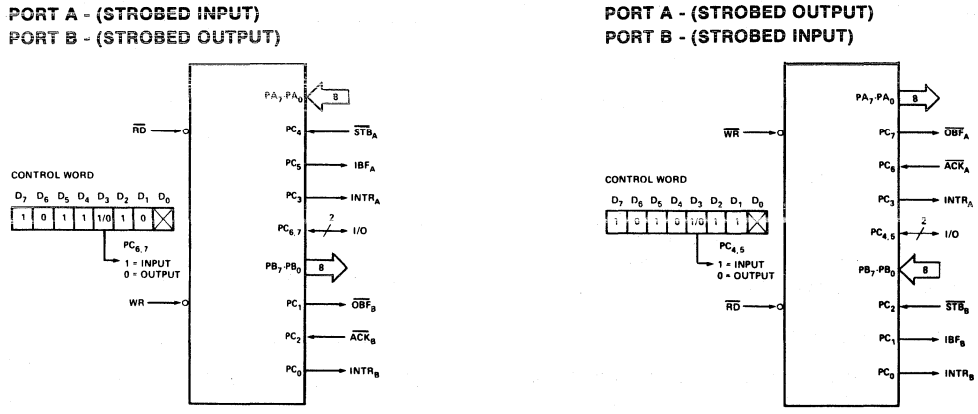


FIGURE 10. COMBINATIONS OF MODE 1

Operating Modes

MODE 2 (Strobed Bi-directional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline similar to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bi-directional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the CPU for both input or output operations. INTR will be set either by the rising edge of $\overline{ACK}$ (INTE1 = 1) or the rising edge of $\overline{STB}$ (INTE2 = 1). INTR will be reset by the falling edge of $\overline{WR}$ (if previously set by the rising edge or $\overline{ACK}$), the falling edge of $\overline{RD}$ (if previously set by the rising edge of $\overline{STB}$), or the falling edge of $\overline{WR}$ when immediately following a low $\overline{RD}$ pulse or the falling edge of $\overline{RD}$ when immediately following a low $\overline{WR}$ pulse (if previously set by the rising edges of both $\overline{ACK}$ and $\overline{STB}$).

Output Operations

$\overline{OBF}$ (Output Buffer Full)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge)

A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$)

Controlled by Bit Set/Reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF)

Controlled by Bit Set/Reset of PC_4.

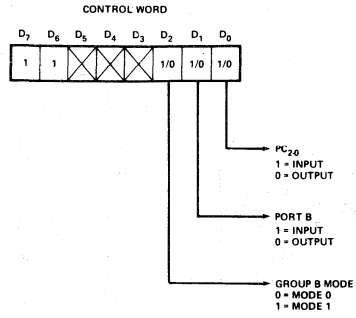


FIGURE 11. MODE CONTROL WORD

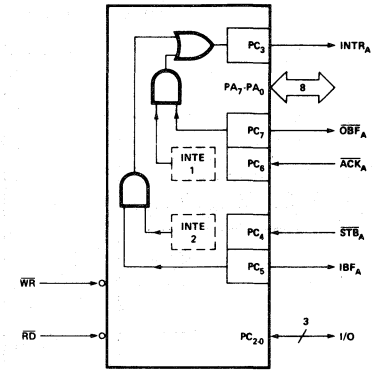


FIGURE 12. MODE 2 (BI-DIRECTIONAL)

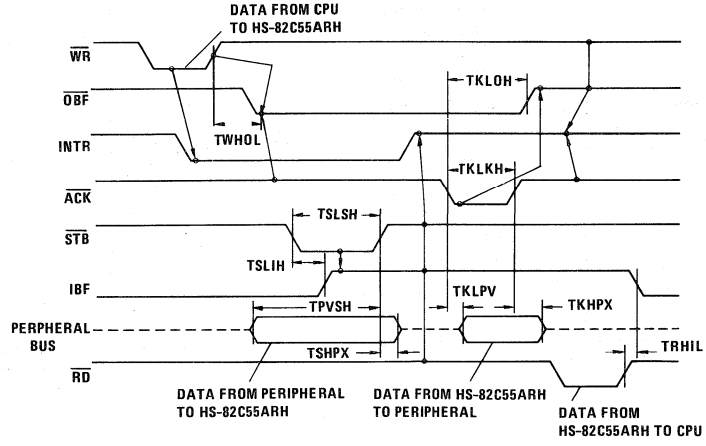


FIGURE 13. MODE 2 (BI-DIRECTIONAL)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.

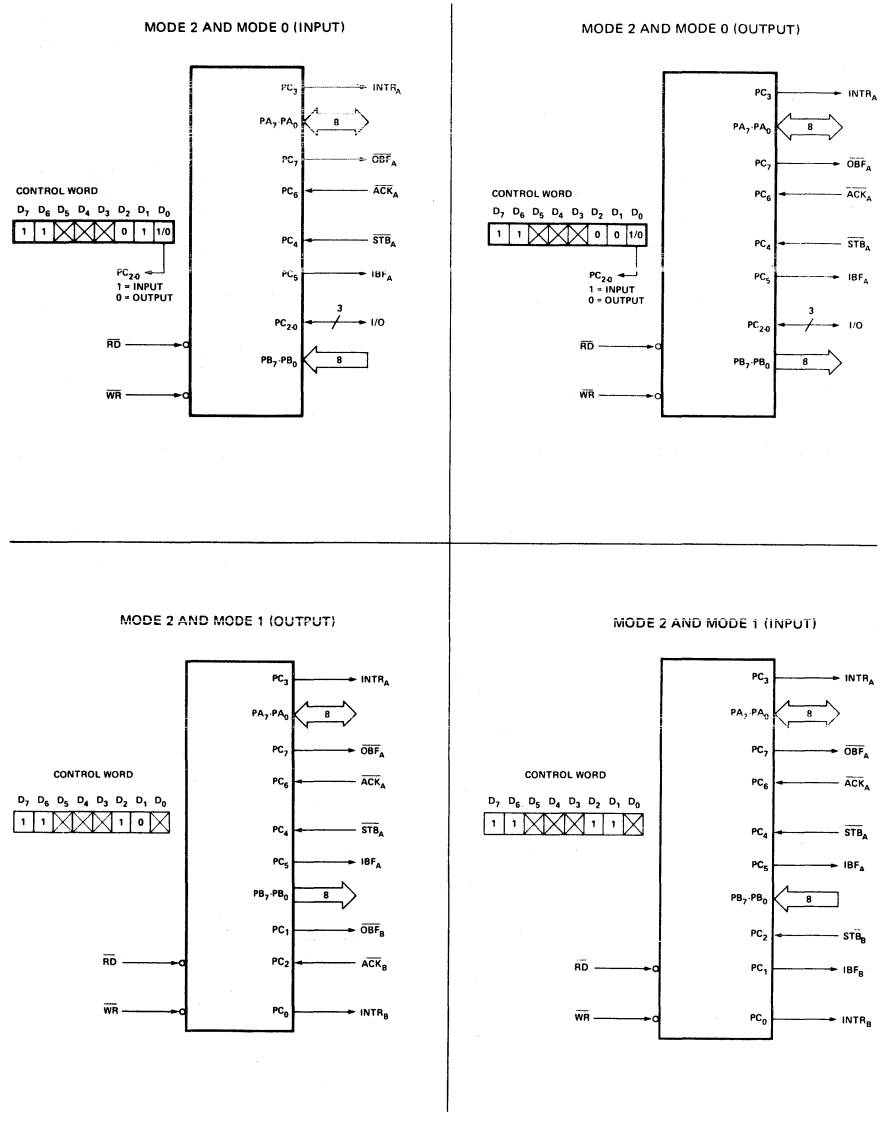


FIGURE 14. MODE 2 COMBINATIONS

Mode Definition Summary

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA_0	IN	OUT	IN	OUT	↔
PA_1	IN	OUT	IN	OUT	↔
PA_2	IN	OUT	IN	OUT	↔
PA_3	IN	OUT	IN	OUT	↔
PA_4	IN	OUT	IN	OUT	↔
PA_5	IN	OUT	IN	OUT	↔
PA_6	IN	OUT	IN	OUT	↔
PA_7	IN	OUT	IN	OUT	↔
PB_0	IN	OUT	IN	OUT	—
PB_1	IN	OUT	IN	OUT	—
PB_2	IN	OUT	IN	OUT	—
PB_3	IN	OUT	IN	OUT	—
PB_4	IN	OUT	IN	OUT	—
PB_5	IN	OUT	IN	OUT	—
PB_6	IN	OUT	IN	OUT	—
PB_7	IN	OUT	IN	OUT	—
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

MODE 0 OR MODE 1 ONLY

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC_2, PC_4 and PC_6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C"command, nor can the interrupt enable flags be accessed.

To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

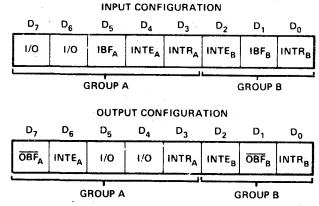


FIGURE 15. MODE 1 STATUS WORD FORMAT

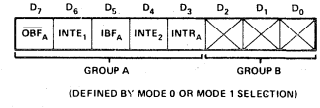


FIGURE 16. MODE 2 STATUS WORD FORMAT

INTERRUPT ENABLE FLAG	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC_2	$\overline{ACK}_B$ (Output Mode 1) or STB_B (Input Mode 1)
INTE A2	PC_4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
INTE A1	PC_6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the HS-82C55ARH to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the HS-82C55ARH is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND - 0.5V to VDD + 0.5V
Output Current (Port A, B, C) 3mA
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications

VDD = +5.0V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	VDD-1.5		V	Note 2
VIL	Logical Zero Input Voltage		0.8	V	Note 2
VOH	Logical One Output Voltage	3.0 VDD -0.4		V V	IOH = -2.5mA IOH = 100μA
VOL	Logical Zero Output Voltage		0.4	V	IOL = +2.5mA
IIL	Input Leakage Current	-1.0	1.0	μA	0V ≤ VIN ≤ VDD
IOZ	I/O Pin Leakage Current	-10.0	10.0	μA	0V ≤ VO ≤ VDD
IBHH	Bus Hold High Current	-60	-800	μA	VO = 3.0V Ports A, B, C
IBHL	Bus Hold Low Current	+60	+800	μA	VO = 1.0V Port A Only
IDAR	Darlington Drive Current	-2.0	Note 1	mA	Ports A, B, C Test Condition 3
IDDSB	Standby Power Supply Current		20	μA	VDD = 5.5V VIN = VDD or GND Outputs Open

Note 1. No internal current limiting exists on PORT OUTPUTS. A resistor must be added externally to limit the current.
Note 2. Each of the following groups is tested separately with all other inputs using VIH = 2.6V, VIL = 0.4V:
PA, PB, PC, D0-7, Controls (Pins 5, 6, 8, 9, 35, 36).

Capacitance

T_A = +25°C; VDD = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}*	Input Capacitance	10	pF	FREQ = 1MHz Unmeasured Pins Returned to GND
$C_{I/O}$*	I/O Capacitance	20	pF	

* Guaranteed and sampled, but not 100% tested.

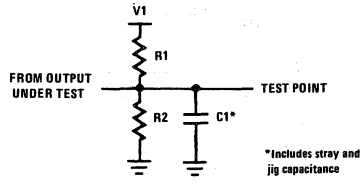
A.C. Electrical Specifications VDD = +5.0V ± 10%; GND = 0V; T_A = -55°C to +125°C

Bus Parameters

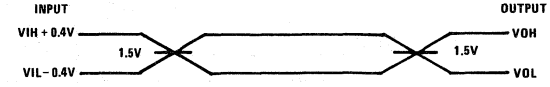
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ					
TAVRL	Address Stable Before $\overline{RD}$	0		ns	
TRHAX	Address Stable After $\overline{RD}$	0		ns	
TRLRH	$\overline{RD}$ Pulse Width	250		ns	
TRLDV	Data Valid From $\overline{RD}$		200	ns	1
TRHDX	Data Float After $\overline{RD}$	10	75*	ns	2
TRWHRWL	Time Between $\overline{RD}$s and/or $\overline{WR}$s	300		ns	
WRITE					
TAVWL	Address Stable Before $\overline{WR}$	0		ns	
TWHAX	Address Stable After $\overline{WR}$	20		ns	Ports A & B
		100		ns	Port C
TWLWH	$\overline{WR}$ Pulse Width	100		ns	
TDVWH	Data Valid to $\overline{WR}$ High	100		ns	
TWHDX	Data Valid After $\overline{WR}$ High	30		ns	Ports A & B
		100		ns	Port C
OTHER TIMINGS					
TWHPV	$\overline{WR}$ = 1 to Output		350	ns	1
TPVRL	Peripheral Data Before $\overline{RD}$	0		ns	
TRHPX	Peripheral Data After $\overline{RD}$	0		ns	
TKLKH	$\overline{ACK}$ Pulse Width	200		ns	
TSLSH	$\overline{STB}$ Pulse Width	100		ns	
TPVSH	Peripheral Data Before $\overline{STB}$ High	20		ns	
TSHPX	Peripheral Data After $\overline{STB}$ High	50		ns	
TKLPV	$\overline{ACK}$ = 0 to Output		175	ns	1
TKHPZ	$\overline{ACK}$ = 1 to Output Float	10	250*	ns	2
TWHOL	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0		150	ns	1
TKLOH	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1		150	ns	1
TSLIH	$\overline{STB}$ = 0 to IBF = 1		150	ns	1
TRHIL	$\overline{RD}$ = 1 to IBF = 0		150	ns	1
TRLNL	$\overline{RD}$ = 0 to INTR = 0		200	ns	1
TSHNH	$\overline{STB}$ = 1 to INTR = 1		150	ns	1
TKHNH	$\overline{ACK}$ = 1 to INTR = 1		150	ns	1
TWLNL	$\overline{WR}$ = 0 to INTR = 0		200	ns	1
TRSHRSL	RESET Pulse Width	500		ns	See Note 3

Note 3. Period of initial RESET pulse after power-on must be at least 50µsec. Subsequent RESET pulses may be 500ns minimum.
* Guaranteed and Sampled, not 100% tested

A.C. Test Circuit



A.C. Testing Input, Output Waveforms



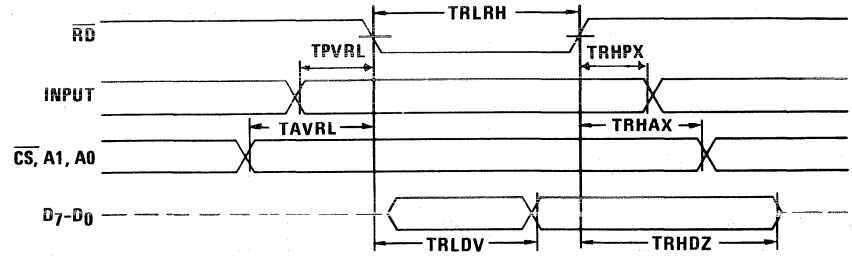
A.C. Testing: All parameters tested as per test circuits. Input rise and fall times are driven at 1ns/V.

TEST CONDITIONS DEFINITION TABLE

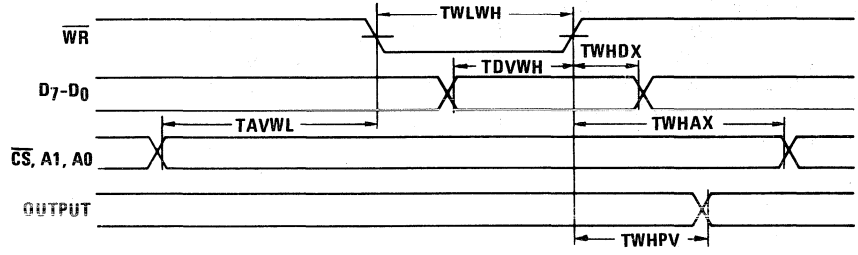
TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	Open	150pF
2	5.0V	2KΩ	1.7KΩ	50pF
3	1.5V	1.2KΩ	Open	Open

Waveforms

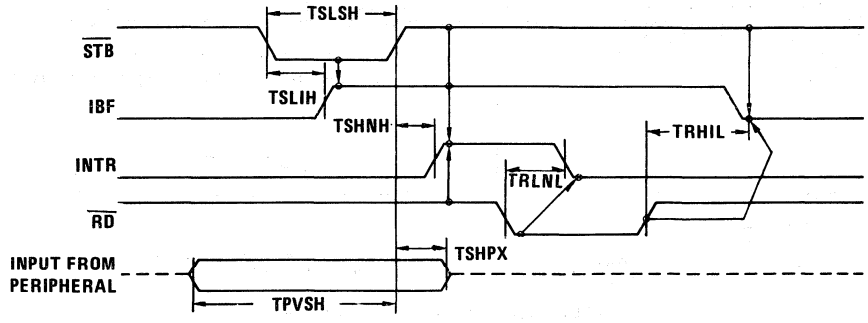
MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)

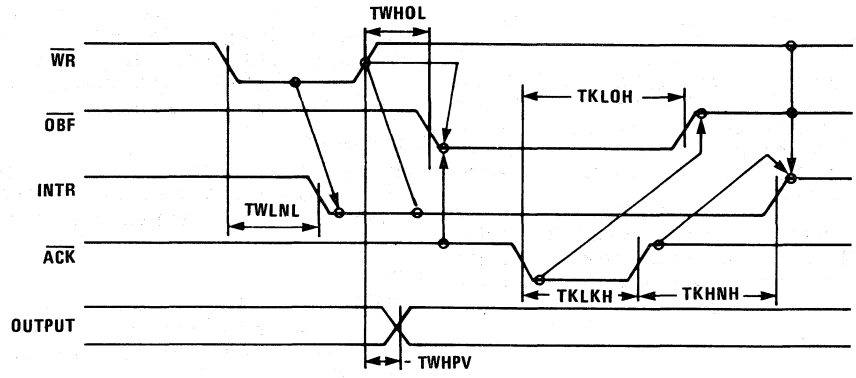


MODE 1 (STROBED INPUT)

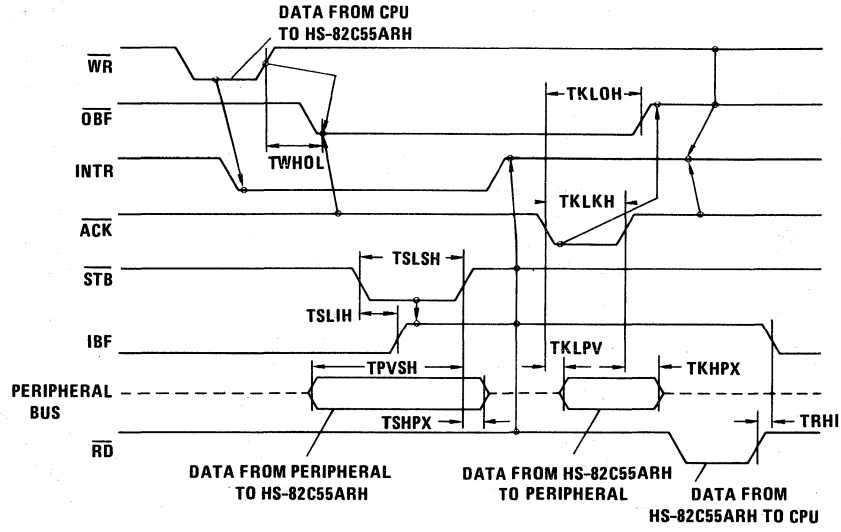


Waveforms

MODE 1 (STROBED OUTPUT)

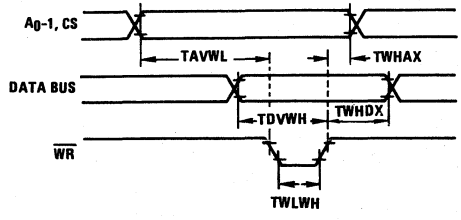


MODE 2 (BIDIRECTIONAL)

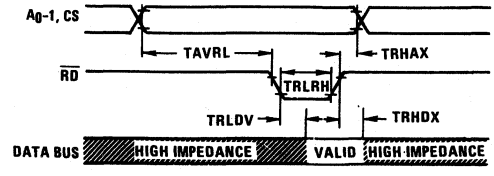


NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.

WRITE TIMING



READ TIMING



Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad(Si) ±10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = +5.5V. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The sample devices shall be tested within one hour after irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.

Radiation Effects

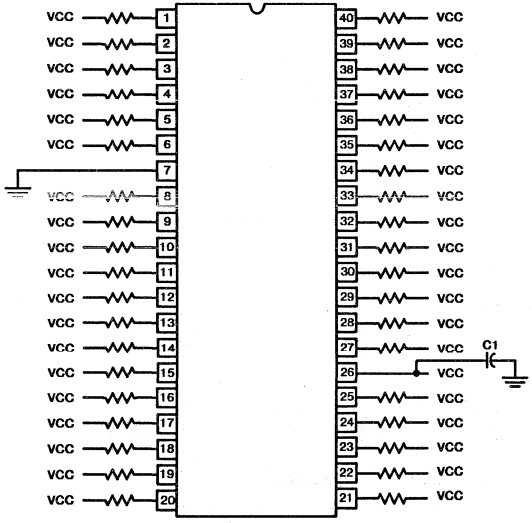
1. TOTAL DOSE:

   No degradation of any parameters will be seen at 1 x 10^5 Rad(Si). Minimal (10%) increases in **Static** supply current due to leakages will begin to appear between 1 x 10^5 Rad(Si) and 5 x 10^5 Rad(Si), increasing to 50% after exposure to 1 x 10^6 Rad(Si), although the device will remain functional within specifications.
2. DOSE RATE:

   The HS-82C55ARH is manufactured on EPI material and is consequently latch-up free. Transient upset can be expected at dose rates higher than 1 x 10^9 Rad(Si)/sec.
3. SINGLE EVENT UPSET:

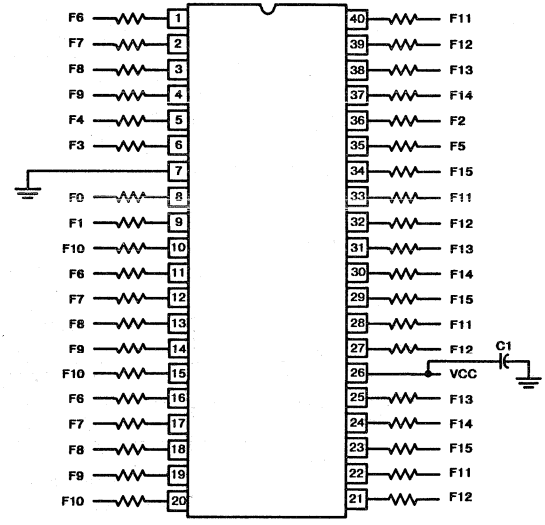
   The HS-82C55ARH is manufactured on EPI material and is consequently latch-up free. Preliminary testing has shown the device has a LET threshold of 24MeV/mg/cm2.

Burn-In Circuits



STATIC CONFIGURATION

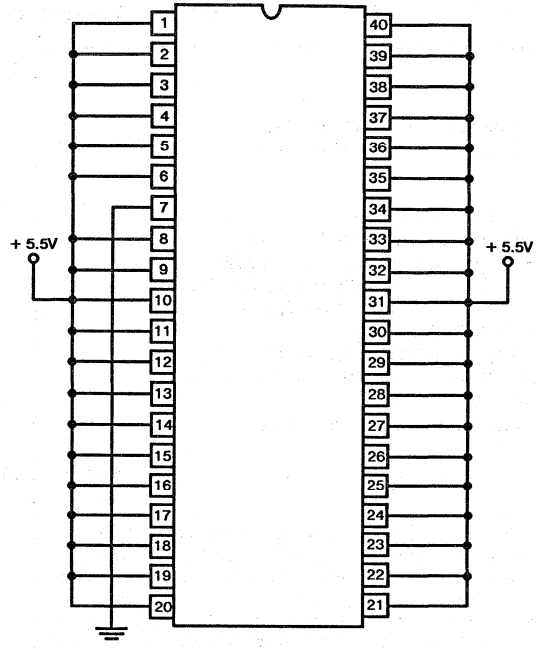
All resistors = 47kΩ; ± 5%; 1/4W (Min)
GND = Ground
VCC = 5.5V; ±10%
C1 = 0.1µF minimum



DYNAMIC CONFIGURATION

All resistors = 47kΩ; ± 5%; 1/4W (Min)
GND = Ground
VCC = 5.5V; ±10%
C1 = 0.1µF minimum

Irradiation Circuit



HS-82C55ARH CMOS PROGRAMMABLE
PERIPHERAL INTERFACE

HARRIS

HS-82C85RH

Radiation Hardened CMOS Static Clock Controller/Generator

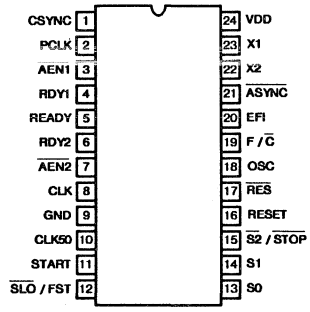
July 1990

Features

- Radiation Hardened
  - Total Dose ..... > 10^5 RAD(Si)
  - Transient Upset ... > 10^8 RAD(Si)/sec
  - Latch Up Free EPI-CMOS
  - Functional After Total Dose..... 1 x 10^6 RAD(Si)
- Very Low Power Consumption
- Pin Compatible with NMOS 8285 and Harris 82C85
- Generates System Clocks for Microprocessors and Peripherals
- Complete Control Over System Clock Operation for Very Low System Power
  - Stop-Oscillator
  - Stop-Clock
  - Low Frequency (Slo) Mode
  - Full Speed Operation
- DC to 15MHz Operation (DC to 5MHz System Clock)
- Generates Both 50% and 33% Duty Cycle Clocks (Synchronized)
- Uses Either Parallel Mode Crystal Circuit or External Frequency Source
- TTL/CMOS Compatible InputssOutputs
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- Military Temperature Range ..... -55°C to +125°C

Pinout

DIP
TOP VIEW

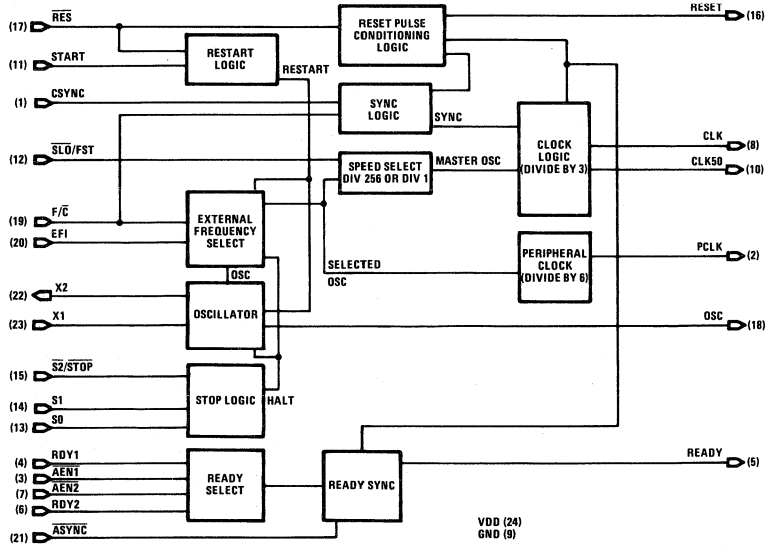


Description

The Harris HS-82C85RH is a high performance, radiation hardened CMOS Clock Controller/Generator designed to support systems utilizing radiation hardened static CMOS microprocessors such as the HS-80C86RH. The HS-82C85RH contains a crystal controlled oscillator, reset pulse conditioning, halt/restart logic, and divide-by-256 circuitry. These features provide the means to stop the system clock, stop the clock oscillator, or run the system at a low frequency (CLK/256), enhancing control of static system power dissipation and allowing system shut-down during periods of external stress.

Static CMOS circuit design insures low operating power and permits operation with an external frequency source from DC to 15MHz. Crystal controlled operation to 15MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors. All inputs (except X1, X2, and RES) are TTL compatible over all temperature and voltage ranges. Outputs are guaranteed compatible with both CMOS and TTL specifications. The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

PIN	PIN NUMBER	TYPE	DESCRIPTION
X1 X2	23 22	I O	CRYSTAL CONNECTIONS: X1 and X2 are the crystal oscillator connections. The crystal frequency must be three times the maximum desired processor clock frequency. X1 is the oscillator circuit input and X2 is the output of the oscillator circuit.
EFI	20	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input signal. This input signal should be a square wave with a frequency of three times the maximum desired CLK output frequency.
F/$\overline{C}$	19	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ selects either the crystal oscillator or the EFI input as the main frequency source. When F/$\overline{C}$ is LOW, the HS-82C85RH clocks are derived from the crystal oscillator circuit. When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input. F/$\overline{C}$ cannot be dynamically switched during normal operation.
START	11	I	A low-to-high transition on START will restart the CLK, CLK50 and PCLK outputs after the appropriate restart sequence is completed. When in the crystal mode (F/$\overline{C}$ LOW) with the oscillator stopped, the oscillator will be restarted when a Start command is received. The CLK, CLK50 and PCLK outputs will start after the oscillator input signal (X1) reaches the Schmitt trigger input threshold and an 8K internal counter reaches terminal count. If F/$\overline{C}$ is HIGH (EFI mode), CLK, CLK50 and PCLK will restart within 3 EFI cycles after START is recognized. The HS-82C85RH will restart in the same mode ($\overline{SLO}$/FST) in which it stopped. A high level on START disables the STOP mode.
S0 S1 $\overline{S2}$/$\overline{STOP}$	13 14 15	I I I	$\overline{S2}$/$\overline{STOP}$, S1, S0 are used to stop the HS-82C85RH clock outputs (CLK, CLK50, PCLK) and are sampled by the rising edge of CLK. CLK, CLK50 and PCLK are stopped by $\overline{S2}$/$\overline{STOP}$, S1, S0 being in the LHH state on the low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition. CLK and CLK50 stop in the high state. PCLK stops in it's current state (high or low). When in the crystal mode (F/$\overline{C}$) low and a STOP command is issued, the HS-82C85RH oscillator will stop along with the CLK, CLK50 and PCLK outputs. When in the EFI mode, only the CLK, CLK50 and PCLK outputs will be halted. The oscillator circuit if operational, will continue to run. The oscillator and/or clock is restarted by the START input signal going true (HIGH) or the reset input ($\overline{RES}$) going low.
$\overline{SLO}$/FST	12	I	$\overline{SLO}$/FST is a level-triggered input. When HIGH, the CLK and CLK50 outputs run at the maximum frequency (crystal or EFI frequency divided by 3). When LOW, CLK and CLK50 frequencies are equal to the crystal or EFI frequency divided by 768. $\overline{SLO}$/FST mode changes are internally synchronized to eliminate glitches on the CLK and CLK50. START and STOP control of the oscillator or EFI is available in either the SLOW or FAST frequency modes. The $\overline{SLO}$/FST input must be held LOW for at least 195 OSC/EFI clock cycles before it will be recognized. This eliminates unwanted frequency changes which could be caused by glitches or noise transients. The $\overline{SLO}$/FST input must be held HIGH for at least 6 OSC/EFI clock pulses to guarantee a transition to FAST mode operation.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the HS-80C86RH processor and other peripheral devices. When $\overline{SLO}$/FST is high, CLK has an output frequency which is equal to the crystal or EFI input frequency divided by three. When $\overline{SLO}$/FST is low, CLK has an output frequency which is equal to the crystal or EFI input frequency divide by 768. CLK has a 33% duty cycle.
CLK50	10	O	50% DUTY CYCLE CLOCK: CLK50 is an auxiliary clock with a 50% duty cycle and is synchronized to the falling edge of CLK. When $\overline{SLO}$/FST is high, CLK50 has an output frequency which is equal to the crystal or EFI input frequency frequency divided by 3. When $\overline{SLO}$/FST is low, CLK50 has an output frequency equal to the crystal or EFI input frequency divided by 768.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is equal to the crystal or EFI input frequency divided by six and has a 50% duty cycle. PCLK frequency is unaffected by the state of the $\overline{SLO}$/FST input.

Pin Description (Continued)

PIN	PIN NUMBER	TYPE	DESCRIPTION
OSC	18	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal oscillator circuit. OSC is unaffected by the state of the $\overline{SLO}$/FST input. When the HS-82C85RH is in the crystal mode (F/$\overline{C}$ low) and a STOP command is issued, the OSC output will stop in the HIGH state. When the HS-82C85RH is in the EFI mode (F/C HIGH), the oscillator (if operational) will continue to run when a STOP command is issued and OSC remains active.
$\overline{RES}$	17	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The HS-82C85RH provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration. $\overline{RES}$ starts crystal oscillator operation.
RESET	16	O	RESET: RESET is an active HIGH signal which is used to reset the HS-80C86RH processor. Its timing characteristics are determined by $\overline{RES}$. RESET is guaranteed to be HIGH for a minimum of 16 CLK pulses after the rising edge of $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple HS-82C85RHs to be synchronized to provide multiple in-phase clock signals. When CSYNC is HIGH, the internal counters are reset and force CLK, CLK50 and PCLK into a HIGH state. When CSYNC is LOW, the internal counters are allowed to count and the CLK, CLK50 and PCLK outputs are active. CSYNC must be externally synchronized to EFI.
$\overline{AEN1}$ $\overline{AEN2}$	3 7	I I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Buses.
RDY1 RDY2	4 6	I I	BUS READY: (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	21	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is LOW, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is used to inform the HS-80C86RH that it may conclude a pending data transfer.
GND	9	I	Ground
VDD	24	I	+5V power supply

Functional Description

The HS-82C85RH Static Clock Controller/Generator provides simple and complete control of static CMOS system operating modes. The HS-82C85RH can operate with either an external crystal or an external frequency source and can support full speed, slow, stop-clock and stop-oscillator operation. While it is directly compatible with the Harris HS-80C86RH CMOS 16-bit static microprocessor, the HS-82C85RH can also be used for general purpose system clock control.

Separate signals are provided on the HS-82C85RH for stop and start control of the crystal oscillator and clock outputs. A single control line determines fast (crystal/EFI frequency divided by 3) or slow (crystal/EFI frequency divided by 768) mode operation. A clock sychronization input is provided to allow the use of multiple HS-82C85RHs in the same system. The HS-82C85RH generates the proper HS-80C86RH reset pulse, and it also handles all data transfer timing by generating the HS-80C86RH ready signal.

Automatic maximum mode HS-80C86RH software HALT instruction decode logic is present to ease the design of software-based clock control systems and provides complete software control of STOP mode operation. Automatic minimum mode software HALT instruction decoding can be easily implemented with a single 74HC74 device. Restart logic insures valid clock start-up and complete synchronization of CLK, CLK50 and PCLK.

Static Operating Modes

The HS-82C85RH Static Clock Controller can be dynamically set to operate in any one of four modes at any one time: FAST, SLOW, STOP-CLOCK and STOP-OSCILLATOR. Each mode has distinct power and performance characteristics which can be matched to the needs of a particular system at a specific time (See Table 1).

Keep in mind that a single system may require all of these operating modes at one time or another during normal operation. A design need not be limited to a single operating mode or a specific combination of modes. The appropriate operating mode can be matched to the power-performance level needed at a specific time or in a particular circumstance.

Reset Logic

The HS-82C85RH reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the HS-82C85RH.

When in the crystal oscillator ($F/\overline{C}$ = LOW) or the EFI ($F/\overline{C}$ = HIGH) mode, a LOW state on the $\overline{RES}$ input will set the RESET output to the HIGH state. It will also restart the oscillator circuit if it is in the idle state. The RESET output is guaranteed to stay in the HIGH state for a minimum of 16 CLK cycles after a low-to-high transition of the $\overline{RES}$ input.

An oscillator restart count sequence will not be disturbed by RESET if this count is already in progress. After the restart counter expires, the RESET output will stay HIGH at least for 16 periods of CLK before going LOW. RESET can be kept high beyond this time by a continuing low input on the $\overline{RES}$ input.

If $F/\overline{C}$ is low (crystal oscillator mode), a low state on $\overline{RES}$ starts the crystal oscillator circuit. The stopped outputs remain inactive, until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK) start cleanly with the proper phase relationships.

This 8192 count requirement insures that the CLK, CLK50 and PCLK outputs will meet minimum clock requirements and will not be affected by unstable oscillator characteristics which may exist during the oscillator start-up sequence. This sequence is also followed when a START command is issued while the HS-82C85RH oscillator is stopped.

Oscillator/Clock Start Control

Once the oscillator is stopped (or committed to stop) or at power-on, the restart sequence is initiated by a HIGH state on START or LOW state on $\overline{RES}$. If $F/\overline{C}$ is HIGH, then restart occurs immediately after the START or $\overline{RES}$ input is synchronized internally. This insures that stopped outputs (CLK, PCLK, OSC and CLK50) start cleanly with the proper phase relationship.

If $F/\overline{C}$ is low (crystal oscillator mode), a HIGH state on the START input or a low state on $\overline{RES}$ causes the crystal oscillator to be restarted. The stopped outputs remain stopped, until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK) start cleanly with the proper phase relationships.

TABLE 1. STATIC SYSTEM OPERATING MODE CHARACTERISTICS

OPERATING MODE	DESCRIPTION	POWER LEVEL	PERFORMANCE
Stop — Oscillator	All system clocks and main clock oscillator are stopped	Maximum savings	Slowest response due to oscillator restart time
Stop — Clock	System CPU and peripherals clocks stop but main clock oscillator continues to run at rated frequency	Reduced system power	Fast restart — no oscillator restart time
Slow	System CPU clocks are slowed while peripheral clock and main clock oscillator run at rated frequency	Power dissipation slightly higher than Stop-Clock	Continuous operation at low frequency
Fast	All clocks and oscillators run at rated frequency	Highest power	Fastest response

Typically, any input signal which meets the START input timing requirements can be used to start the HS-82C85RH. In many cases, this would be the INT output from an HS-82C59ARH CMOS Priority Interrupt Controller (See Figure 1). This output, which is active high, can be connected to both the HS-82C85RH START pin and to the INTR input on the microprocessor.

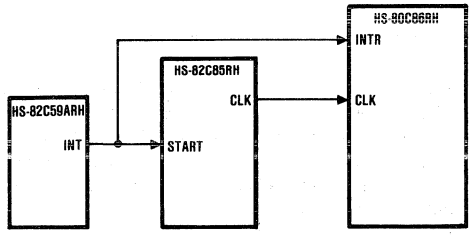


FIGURE 1. HS-82C85RH START CONTROL USING HS-82C59ARH INTERRUPT CONTROLLER

When the INT output becomes active (as a result of a "restart" IRQ or a system reset), the oscillator/clock circuit on the HS-82C85RH will restart. Upon completion of the appropriate restart sequence, the CLK signal to the CPU will become active. The CPU can then respond to the still-pending interrupt request.

Oscillator/Clock Stop Control

The S0, S1, and $\overline{S2}/\overline{STOP}$ control lines determine when the HS-82C85RH clock outputs or oscillator will stop. These three lines are designed to connect directly to the MAXimum mode HS-80C86RH status lines as shown in Figure 2.

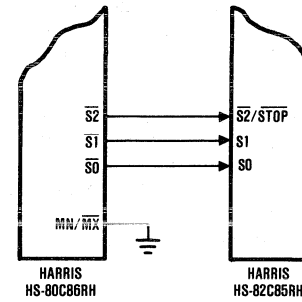


FIGURE 2. HS-82C85RH STOP CONTROL USING HS-80C86RH MAXIMUM MODE STATUS LINES

When used in this configuration, the HS-82C85RH will automatically recognize a software HALT command from the HS-80C86RH and stop the system clocks or oscillator. This allows complete software control of the STOP function.

If the HS-80C86RH is used in the MINimum mode, the HS-82C85RH can be controlled using the $\overline{S2}/\overline{STOP}$ input (with S0 and S1 held high). This can be done using the circuit shown in Figure 3. Since the HS-80C86RH, when executing a halt instruction in minimum mode, issues a

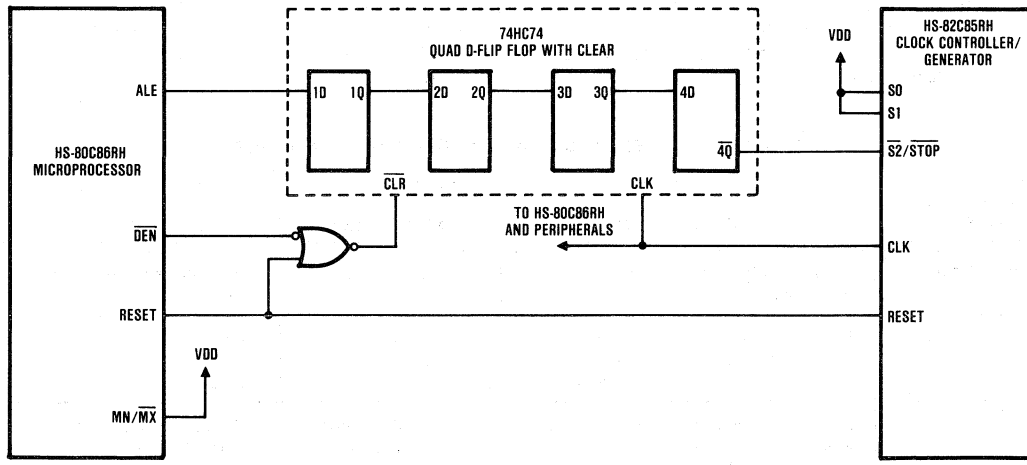


FIGURE 3. HS-82C85RH STOP CONTROL USING HS-80C86RH IN MINIMUM MODE

single ALE pulse with no corresponding bus signals ($\overline{DEN}$ remains high), the ALE pulse will be clocked through the 74HC74 and put the HS-82C85RH into stop mode.

The HS-82C85RH status inputs $\overline{S2}/\overline{STOP}$, S1, S0 are sampled on the rising edge of CLK. The oscillator (F/$\overline{C}$ LOW only) and clock outputs are stopped by $\overline{S2}/\overline{STOP}$, S1, S0 being in the LHH state on a low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition. CLK and CLK50 will stop in the logic HIGH state after two additional complete cycles of CLK. PCLK stops in its current state (HIGH or LOW). This is true for both SLOW and FAST mode operation.

Stop-Oscillator Mode

When the HS-82C85RH is stopped while in the crystal mode (F/C LOW), the oscillator, in addition to all system clock signals (CLK, CLK50 and PCLK), are stopped. CLK and CLK50 stop in the high state. PCLK stops in its current state (high or low).

With the oscillator stopped, HS-82C85RH power drops to its lowest level. All clocks and oscillators are stopped. All devices in the system which are driven by the HS-82C85RH go into the lowest power standby mode. The HS-82C85RH also goes into standby and requires a power supply current of less than 100 microamps.

Stop-Clock Mode

When the HS-82C85RH is in the EFI mode (F/C HIGH) and a STOP command is issued, all system clock signals (CLK, CLK50 and PCLK) are stopped. CLK and CLK50 stop in the high state. PCLK stops in its current state (high or low).

The HS-82C85RH can also provide its own EFI source simply by connecting the OSC output to the EFI input and pulling the F/C input HIGH. This puts the HS-82C85RH into the External Frequency Mode using its own oscillator as an external source signal (See Figure 4). In this configuration, when the HS-82C85RH is stopped in the EFI mode, the oscillator continues to run. Only the clocks to the CPU and peripherals (CLK, CLK50 and PCLK) are stopped.

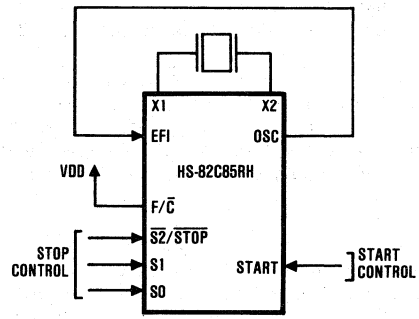


FIGURE 4. STOP-CLOCK MODE USING HS-82C85RH IN EFI MODE WITH OSCILLATOR AS FREQUENCY SOURCE

Clock Slow/Fast Operation

The $\overline{SLO}$/FST input determines whether the CLK and CLK50 outputs run at full speed (crystal or EFI frequency divided by 3) or at slow speed (crystal or EFI frequency divided by 768) (See Figure 5). When in the SLOW mode, HS-82C85RH stop-clock and stop-oscillator functions operate in the same manner as in the FAST mode, and the frequency of PCLK is unaffected.

The SLOW mode allows the CPU and the system to operate at a reduced rate which, in turn, reduces system power. For example, the operating power for the HS-80C86RH CPU is 10 mA/MHz of clock frequency. When the SLOW mode is used in a typical 5 MHz system, CLK and CLK50 run at approximately 20 kHz. At this reduced frequency, the average operating current of the CPU drops to 200 microamps. Adding the HS-80C86RH 500 microamps standby current brings the total current to 700 microamps.

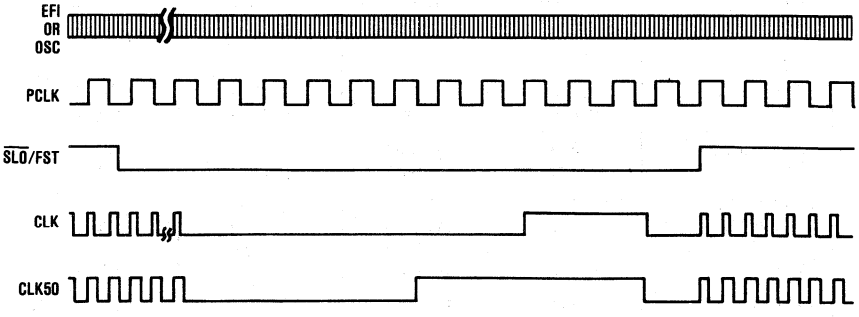


FIGURE 5. SLOW/FAST TIMING OVERVIEW

While the CPU and peripherals run slower and the HS-82C85RH CLK and CLK50 outputs switch at a reduced frequency, the main HS-82C85RH oscillator is still running at the maximum frequency (determined by the crystal or EFI input frequency.) Since CMOS power is directly related to operating frequency, HS-82C85RH power supply current will typically be reduced by 25-35%.

Internal logic requires that the $\overline{SLO}$/FST pin be held low for at least 195 oscillator or EFI clock pulses before the SLOW mode command is recognized. This requirement eliminates unwanted FAST-to-SLOW mode frequency changes which could be caused by glitches or noise spikes.

To guarantee FAST mode recognition, the $\overline{SLO}$/FST pin must be held high for at least 3 OSC or EFI pulses. The HS-82C85RH will begin FAST mode operation on the next PCLK edge after FAST command recognition. Proper CLK and CLK 50 phase relationships are maintained and minimum pulse width specifications are met.

FAST-to-SLOW or SLOW-to-FAST mode changes will occur on the next rising or falling edge of PCLK. It is important to remember that the transition time for operating frequency changes, which are dependent upon PCLK, will vary with the HS-82C85RH oscillator or EFI frequency.

Slow/Fast Mode Control

The HS-82C55ARH programmable peripheral interface can be used to provide slow/fast mode control by connecting one of the port pins directly to the $\overline{SLO}$/FST pin (See Figure 6). With the port pin configured as an output, software control of the $\overline{SLO}$/FST pin is provided by simply writing a logical one (FAST mode) or logical zero (SLOW Mode) to the corresponding port. PORT C is well-suited for this function due to its bit set and reset capabilities.

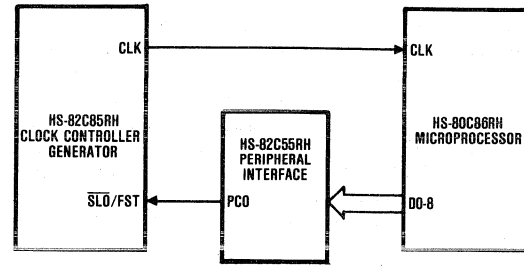


FIGURE 6. SLOW/FAST MODE CONTROL USING HS-82C55RH PERIPHERAL INTERFACE

Alternate Operating Modes

Using alternate modes of operation (slow, stop-clock, stop-oscillator) will reduce the average system operating power dissipation in a static CMOS system (See Table 2). This does not mean that system speed or throughput must be reduced. When used appropriately, the slow, stop-clock, stop-oscillator modes can make your design more power-efficient while maintaining maximum system performance.

Oscillator

The oscillator circuit of the HS-82C85RH is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived. The crystal frequency must be three times the required CPU clock. X1 and X2 are the two crystal input connections. The output of the oscillator is buffered and available at the OSC output (pin 18) for generation of other system timing signals.

TABLE 2. TYPICAL SYSTEM POWER SUPPLY CURRENT FOR STATIC CMOS OPERATING MODES

	FAST	SLOW	STOP-CLOCK	STOP-OSC
CPU Frequency	5 MHz	20 KHz	DC	DC
XTAL Frequency	15 MHz	15 MHz	15 MHz	DC
IDD				
HS-80C86RH	50 mA	2.5 mA	250 μA	250 μA
HS-82C85RH	24.7 mA	16.9 mA	14.1 mA	24.4 μA
HS-82C08RH	1.0 mA	10.0 μA	1.0 μA	1.0 μA
82C82	1.7 mA	6.5 μA	1.0 μA	1.0 μA
HS-82C52RH	151.2 μA	72.0 μA	1.0 μA	1.0 μA
HS-82C54RH	943.0 μA	915.0 μA	1.0 μA	1.0 μA
HS-82C55ARH	3.2 μA	1.2 μA	1.0 μA	1.0 μA
HS-82C59ARH	580.0 μA	520.0 μA	1.0 μA	1.0 μA
74HCXX + other	2.9 mA	110.0 μA	90.0 μA	90.0 μA
HS-65262RH	4.0 mA	50.0 μA	10.0 μA	10.0 μA
HS-6616RH	6.3 mA	52.5 μA	12.0 μA	12.0 μA

All measurements taken at room temperature, VDD = +5.0 volts. Power supply current levels will be dependent upon system configuration and frequency of operation.

For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1=C2) are recommended. Capacitors C1 and C2 are chosen such that their combined capacitance matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

The crystal/capacitor configuration and the formula used to determine the capacitor values are shown in Figure 7. Crystal Specifications are shown in Table 3. For additional information on crystal operation, see Harris publication Tech Brief 47.

$$CT = \frac{C1 \cdot C2}{C1 + C2} \quad \text{(Including stray capacitance)}$$

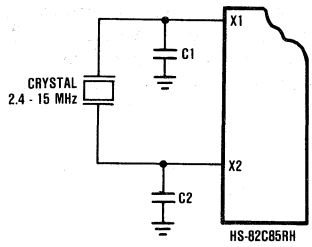


FIGURE 7. HS-82C85RH CRYSTAL CONNECTION

TABLE 3. CRYSTAL SPECIFICATIONS

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	2.4 to 15 MHz
Type of Operation	Parallel Resonant, Fund. Mode
Load Capacitance	20 or 32 pF
R_{SERIES} (Max)	56Ω (f = 15 MHz, CL = 32 pF)
	105Ω (f = 15 MHz, CL = 20 pF)

Frequency Source Selection

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the source frequency for clock generation. If the EFI input is selected as the source, the oscillator section (OSC output) can be used independently for another clock source. If a crystal is not used, then crystal input X1 (pin 23) must be tied to VDD or GND and X2 (pin 22) should be left open. If the EFI mode is not used, then EFI (pin 20) should be tied to VDD or GND.

Clock Generator

The clock generator consists of two synchronous divide-by-three counters with special clear inputs that inhibit the counting. One counter generates a 33% duty cycle waveform (CLK) and the other generates a 50% duty cycle waveform (CLK50). These two counters are negative-edge synchronized, with the low-going transitions of both waveforms occurring on the same oscillator transition. The CLK and CLK50 output frequencies are one-third of the base input frequency when $\overline{SLO}$/FST is high and are equal to the base input frequency divided by 768 when $\overline{SLO}$/FST is low.

The CLK output is a 33% duty cycle clock signal designed to drive the HS-80C86RH microprocessor directly. CLK50 has a 50% duty cycle output synchronous with CLK, designed to drive coprocessors and peripherals requiring a 50% duty cycle clock.

PCLK is a peripheral clock signal with an output frequency equal to the oscillator or EFI frequency divided by 6. PCLK has a 50% duty cycle. PCLK is unaffected by $\overline{SLO}$/FST. When the HS-82C85RH is placed in the STOP mode, PCLK will remain in its current state (logic high or logic low) until a $\overline{RES}$ or START command restarts the HS-82C85RH clock circuitry. PCLK is negative-edge synchronized with CLK and CLK50.

Since PCLK continues to run at the same frequency regardless of the state of the $\overline{SLO}$/FST pin, it can be used by other devices in the system which need a fixed high frequency clock. For example, PCLK could be used to clock an HS-82C54RH programmable interval timer to produce a real-time clock for the system or as a baud rate generator to maintain serial data communications during SLOW mode operation.

Clock Synchronization

The clock synchronization (CSYNC) input allows the output clocks to be synchronized with an external event (such as another HS-82C85RH clock signal). CSYNC going active causes all clocks (CLK, CLK50 and PCLK) to stop in the HIGH state.

It is necessary to synchronize the CSYNC input to the EFI clock using two flip-flops as shown in Figure 8. Multiple external flip-flops are necessary to minimize the occurance of metastable (or indeterminate) states.

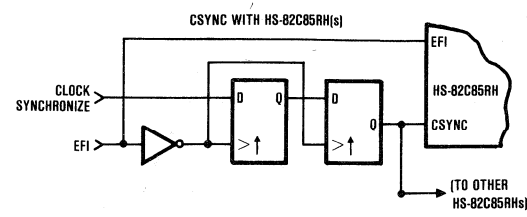


FIGURE 8. HS-82C85RH CSYNC SYNCHRONIZATION METHODS

Ready Synchronization

Two RDY inputs (RDY1, RDY2) are provided to accommodate two system buses. Each RDY input is qualified by its coresponding $\overline{AEN}$ input ($\overline{AEN1}$, $\overline{AEN2}$). Reception of a valid RDY signal causes the HS-82C85RH to output READY high, informing the HS-80C86RH that the pending data transfer may be concluded. (See HS-80C86RH data sheet system timing).

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY set up and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of RDY synchronization operation. When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active RDY input signals. Positive-going asynchronous RDY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time TR1VCH) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go HIGH.

Negative-going asynchronous RDY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the RDY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing (TR1VCL) on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first RDY flip-flop is bypassed in the RDY synchronization logic. RDY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time. $\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

Absolute Maximum Ratings

Supply Voltage ..... +7.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.5V to VDD +0.5V
Storage Temperature Range ..... -65°C to +150°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications

VDD = 5.0V 10%; TA = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	3.5		V	
VIHR	Reset Input High Voltage	3.5		V	
VIL	Logical Zero Input Voltage		0.8	V	
$V_{T^+} - V_{T^-}$	Reset Input Hysteresis	0.25		V	
VOH	Logical One Output Voltage	4.1		V	IOH = -5.0 mA for CLK or CLK50 outputs IOH = -2.5 mA for all other outputs
VOL	Logical Zero Output Voltage		0.4	V	IOL = +5.0 mA for all outputs
IIL	Input Leakage Current	-1.0	1.0	μA	0V < VIN > VDD except $\overline{\text{ASYNC}}$, X1, START, $\overline{\text{SLO}}$/FST, S0, S1, $\overline{\text{S2}}/\overline{\text{STOP}}$
IBHH	Bus-hold High Leakage Current	-10	-200	μA	VIN = 3.0V; $\overline{\text{ASYNC}}$, START, $\overline{\text{SLO}}$/FST, S0, S1, $\overline{\text{S2}}/\overline{\text{STOP}}$ inputs only
IDDSB	Standby Power Supply Current		100	μA	HS-82C85RH in HALT state with oscillator stopped
IDDOP	Operating Power Supply Current		80	mA	Crystal Frequency = 15MHz outputs open
IDDSLOW	Slow Mode Operating Current		1.5	mA/MHz	Outputs Open; $\overline{\text{SLO}}$/FST = 0; START = 1; Other inputs - VIN = VDD or GND

Capacitance

T_A = 25°C. VDD = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN*	Input Capacitance	5	pF	Frequency = 1MHz
COUT*	Output Capacitance	15	pF	Frequency = 1MHz

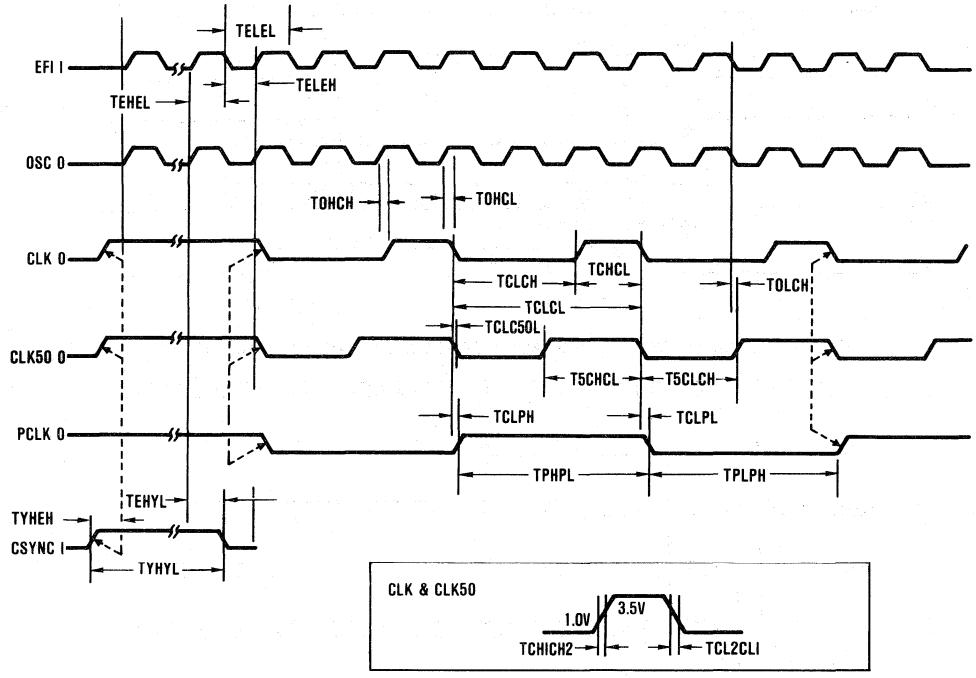
*Guaranteed But Not Tested

A.C. Electrical Specifications VDD = 4.5V, TA = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TIMING REQUIREMENTS					
TEHEL	External Frequency HIGH Time	25		ns	90%-90% V_{IN}
TELEH	External Frequency LOW Time	25		ns	10%-10% V_{IN}
TELEL	EFI or crystal period	65		ns	
TEFIDC	External Frequency input duty cycle	45	55	%	
Fx	Crystal Frequency	2.4	15	MHz	
TR1VCL	RDY1, RDY2 Active Setup to CLK	55		ns	$\overline{ASYNC}$ = HIGH
TR1VCH	RDY1, RDY2 Active Setup to CLK	55		ns	$\overline{ASYNC}$ = LOW
TR1VCL	RDY1, RDY2 Inactive Setup to CLK	55		ns	
TCLR1X	RDY1, RDY2 Hold to CLK	0		ns	
TAYVCL	$\overline{ASYNC}$ Setup to CLK	84		ns	
TCLAYX	$\overline{ASYNC}$ Hold to CLK	0		ns	
TA1VR1V	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	25		ns	
TCLA1X	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		ns	
TYHEH	CSYNC Setup to EFI	17		ns	
TEHYL	CSYNC Hold to EFI	17		ns	
TYHYL	CSYNC Pulse Width	2TELEL		ns	
TI1HCL	$\overline{RES}$ Setup to CLK	105		ns	See Note 2
TSVCH	S0, S1, $\overline{S2}$/$\overline{STOP}$ Setup to CLK	55		ns	
TCHSX	S0, S1, $\overline{S2}$/$\overline{STOP}$ Hold to CLK	55		ns	
TRSVCH	$\overline{RES}$, START Setup to CLK	105		ns	Note 2
TSHSL	$\overline{RES}$ (low) or START (high) pulse width	2/3 TCLCL		ns	
TSFPC	$\overline{SLO}$/FST setup to PCLK	TEHEL + 170		ns	Note 2
TSTART	$\overline{RES}$ or START valid to CLK low	2TELEL + 3		ns	
TSTOP	$\overline{STOP}$ command valid to CLK high	TCLCL +TCLCH	3TCHCH +55	ns	
TIMING RESPONSES					
TCLCL	CLK/CLK50 Cycle Period	200		ns	
TCHCL	CLK HIGH Time	(1/3 TCLCL)+ 3		ns	Figure 9
TCLCH	CLK LOW Time	(2/3 TCLCL)-15		ns	Figure 9
T5CHCL	CLK50 HIGH Time	(1/2 TCLCL)-7.5		ns	Figure 9
T5CLCH	CLK50 LOW Time	(1/2 TCLCL)-7.5		ns	Figure 9
TCH1CH2	CLK/CLK50 Rise Time*		15	ns	1.0V to 3.5V
TCL2CL1	CLK/CLK50 Fall Time*		15	ns	3.5V to 1.0V
TPHPL	PCLK HIGH Time	TCLCL-20		ns	
TPLPH	PCLK LOW Time	TCLCL-20		ns	
TRYLCL	Ready Inactive to CLK	-8		ns	Figure 10 & 11 See Note 4
TRYHCH	Ready Active to CLK	2/3(TCLCL)-15		ns	Figure 10 & 11 See Note 3
TCLIL	CLK to Reset Delay		65	ns	
TCLPH	CLK to PCLK HIGH Delay		40	ns	
TCLPL	CLK to PCLK LOW Delay		40	ns	
TOHCH	OSC to CLK HIGH Delay	-5	60	ns	
TOHCL	OSC to CLK LOW Delay	2	70	ns	
TOLCH	OSC LOW to CLK 50 HIGH Delay	-5	60	ns	
TOST	Start/Reset Valid to Clock LOW		3	ms	Typ. - See Note 8
TOLOH	Output Rise Time (except CLK)*		25	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time (except CLK)*		20	ns	From 2.0V to 0.8V
TRST	RESET output HIGH Time	16xTCLCL		ns	
TCLC50L	CLK LOW to CLK50 LOW Skew		10	ns	

*Guaranteed But Not Tested

NOTES:
1. Output signals switch between VOH and VOL unless otherwise specified.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3, TW states.
4. Applies only to T2 states.
5. All timing delays are measured at 1.5 volts unless otherwise noted.
6. Input signals must switch between VIL max - 0.4 and VIH min + 0.4 volts.
7. Timing measurements made with EFI duty cycle = 50%.
8. Oscillator start-up time depends on several factors including crystal frequency, crystal manufacturer, capacitive load, temperature, power supply voltage, etc. This parameter is given for information only.



NOTE: All Timing Measurements are Made At 1.5 Volts Unless Otherwise Noted

FIGURE 9. WAVEFORMS FOR CLOCKS

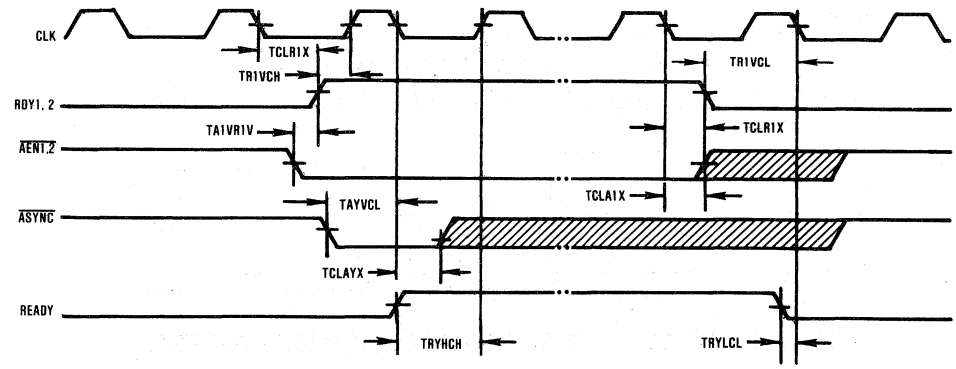


FIGURE 10. WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

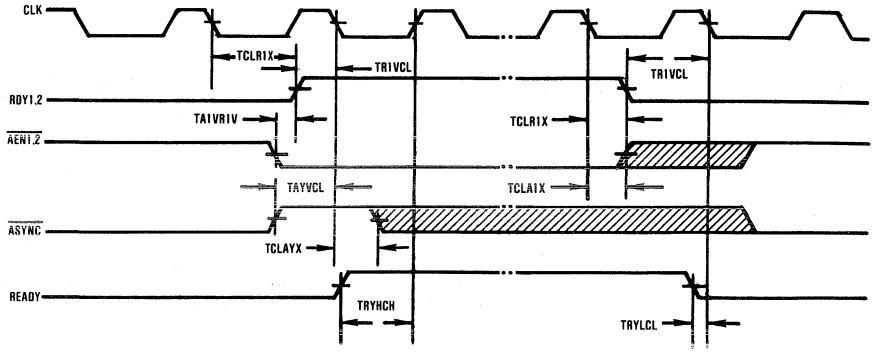


FIGURE 11. WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

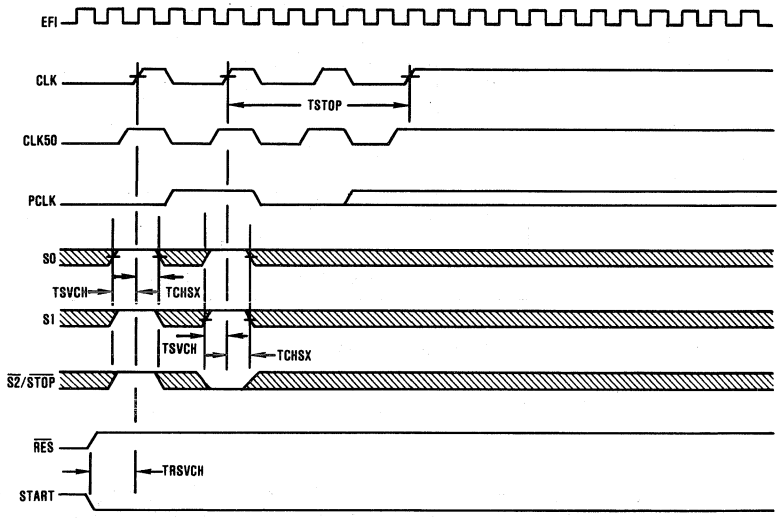


FIGURE 12. CLOCK STOP (F/$\overline{C}$ HIGH OR F/$\overline{C}$ LOW)

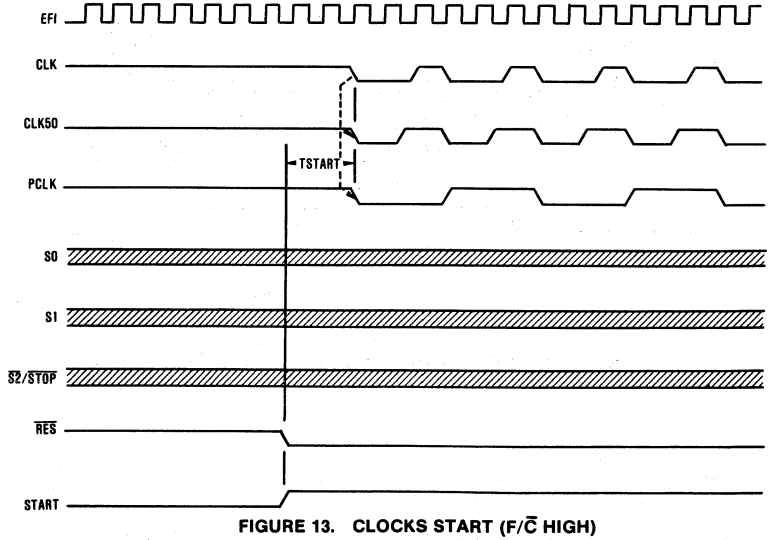


FIGURE 13. CLOCKS START (F/$\overline{C}$ HIGH)

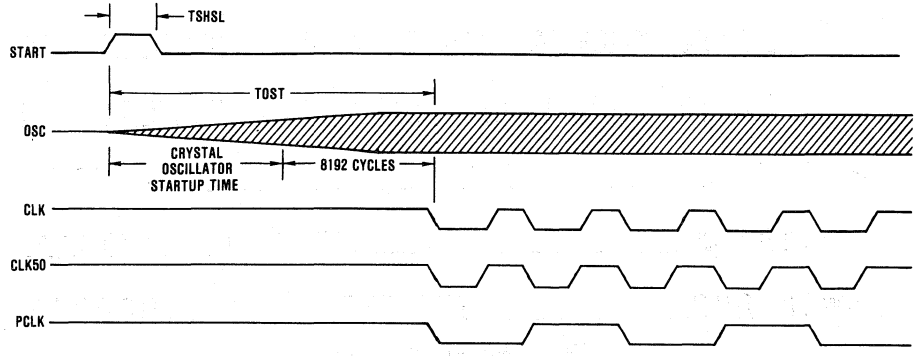


FIGURE 14. CLOCK START (F/$\overline{C}$ LOW)

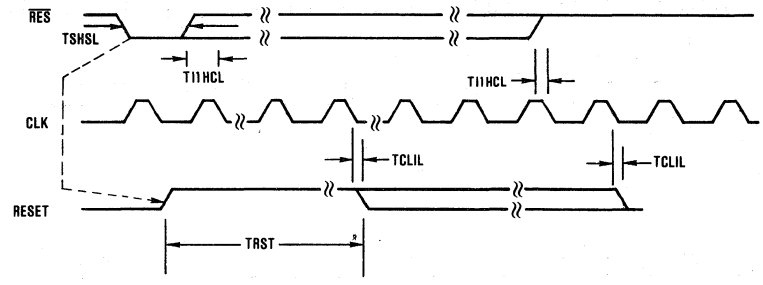


FIGURE 15. RESET TIMING (CLK RUNNING WITH F/$\overline{C}$ LOW — OSC MODE)
(CLK RUNNING — OR STOPPED WITH F/$\overline{C}$ HIGH EFI MODE)

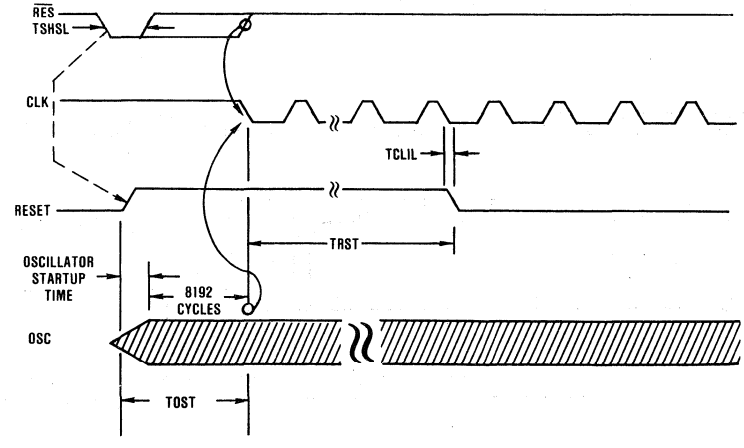


FIGURE 16. RESET TIMING OSCILLATOR STOPPED (F/$\overline{C}$ LOW)

NOTE 1: CLK, CLK50, PCLK Remain in the High State until $\overline{RES}$ goes high and 8192 valid oscillator cycles have been registered by the HS-82C85RH internal counter (TOST time period). After $\overline{RES}$ goes high and CLK, CLK50, PCLK become active, the RESET output will remain high for a minimum of 16 CLK Cycles (TRST).

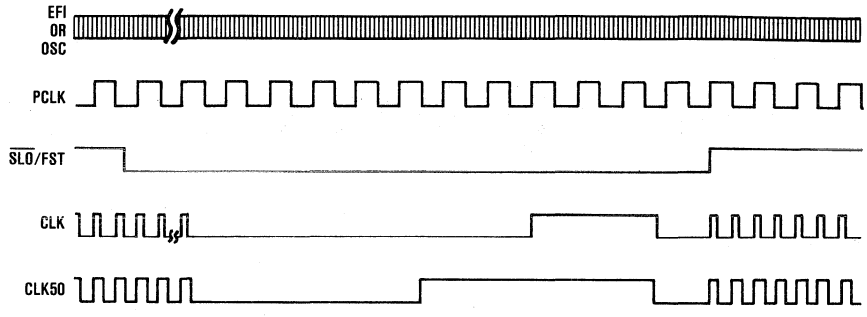


FIGURE 17A. SLO/FST TIMING OVERVIEW

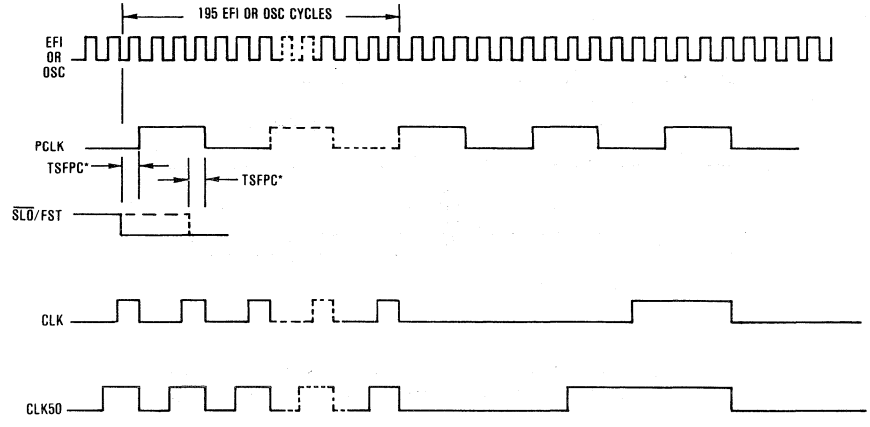
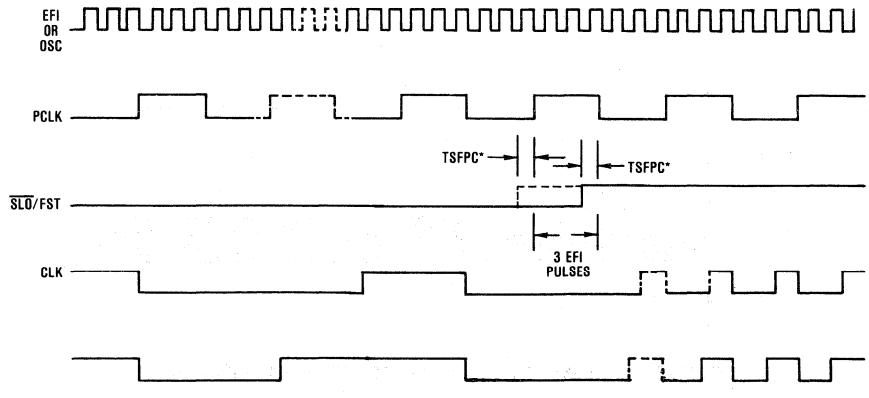


FIGURE 17B. FAST TO SLOW CLOCK MODE TRANSITION



*If TSFPC is not met on one edge of PLCK, SLO/FST will be recognized on the next edge of PCLK

FIGURE 17C. SLOW TO FAST CLOCK MODE TRANSITION

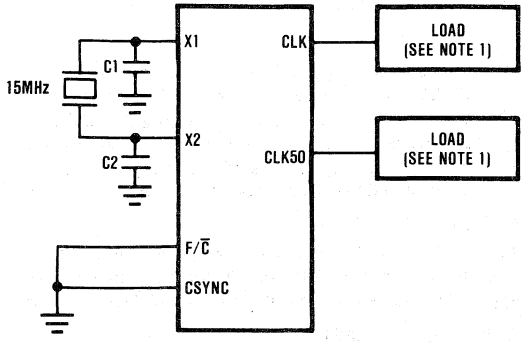


FIGURE 18. CLOCK HIGH AND LOW TIME (USING X1, X2)

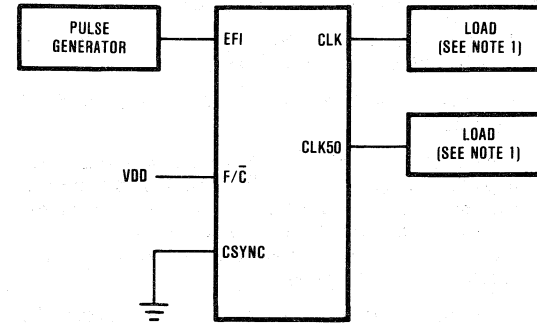


FIGURE 19. CLOCK HIGH AND LOW TIME (USING EFI)

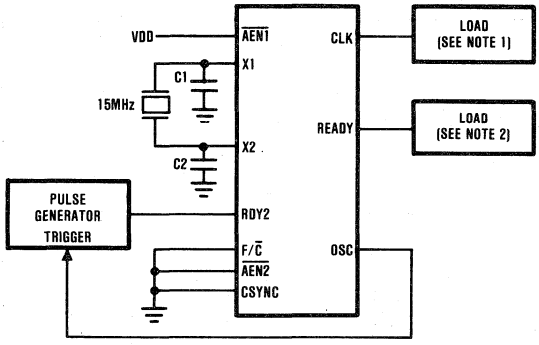


FIGURE 20. READY TO CLOCK (USING X1, X2)

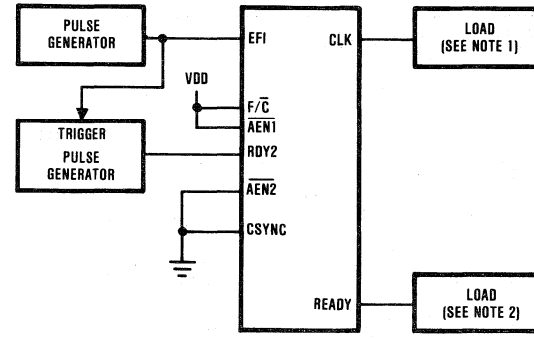


FIGURE 21. READY TO CLOCK (USING EFI)

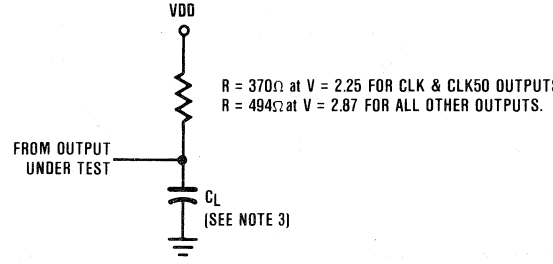


FIGURE 22. TEST LOAD MEASUREMENT CONDITIONS

NOTES:

1. C_L = 50pF
2. C_L = 50pF
3. C_L Includes probe and jig capacitance

Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad(Si) ±10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = +5.5V. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The sample devices shall be tested within one hour after irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.

Radiation Effects

1. TOTAL DOSE:

   No degradation of any parameters will be seen at 1 x 10^5 Rad(Si). Minimal (10%) increases in **static** supply current due to leakages will begin to appear between 1 x 10^5 Rad(Si) and 5 x 10^5 Rad(Si), increasing to 50% after exposure to 1 x 10^6 Rad(Si), although the device will remain functional within specifications.

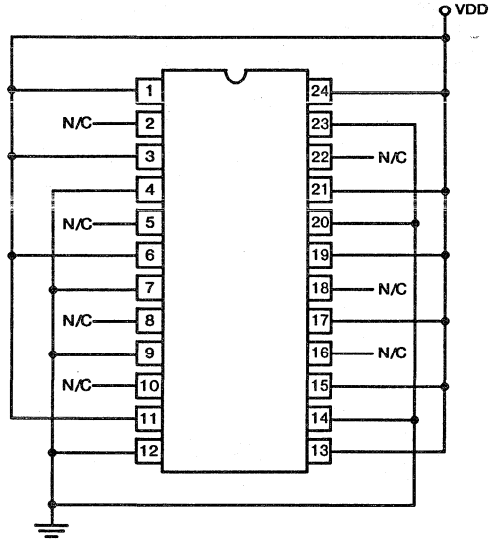
2. DOSE RATE:

   The HS-82C85RH is manufactured on EPI material and is consequently latch-up free. Transient upset can be expected at dose rates higher than 1 x 10^9 Rad(Si)/sec.

3. SINGLE EVENT UPSET:

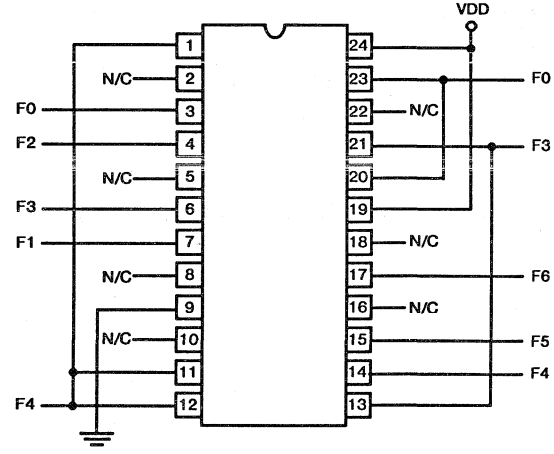
   The HS-82C85RH is manufactured on EPI material and is consequently latch-up free. Preliminary testing has shown the device has an LET threshold of 24 MeV/mg/cm^2.

Burn-In Circuits



STATIC CONFIGURATION

VDD = 6.0V ± 5%
IDD < 500µA
TA = 125°C Minimum
Package Code: SZ (24 Lead DIP)

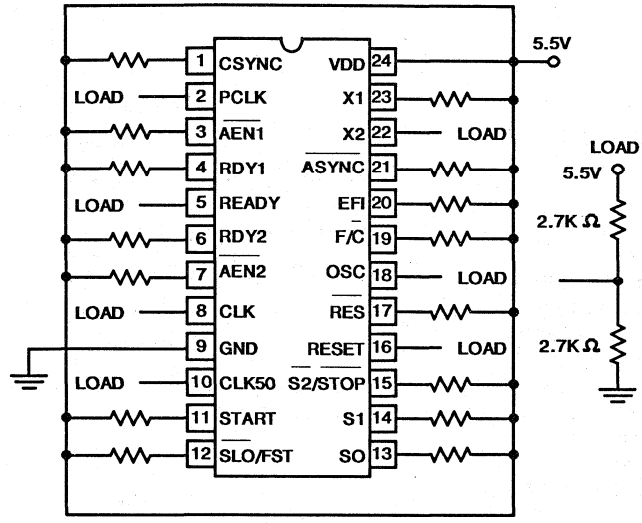


DYNAMIC CONFIGURATION

VDD = 6.0V ± 5% (Burn-In)
VDD = 5.0V ± 5% (Life Test)
IDD < 5µA
TA = 125°C Minimum
Package Code: SZ (24 Lead DIP)

F0 = 10kHz; 50% duty cycle
F1 = F0/2 F4 = F3/2
F2 = F1/2 F5 = F4/2
F3 = F2/2

Irradiation Circuit



R = 47kΩ
Pins Tied to VSS (0V): Pin 9
Pins With Loads: 2, 5, 8, 10, 16, 18, 22
Pins Tied to VDD (5.5V): 1, 3, 4, 6, 7, 11-15, 17, 19-21, 23, 24

HARRIS

HS-83C55RH

Radiation Hardened 16K-Bit CMOS ROM

July 1990

Features

- Radiation Hardened EPI-CMOS
  - Total Dose ..... 1×10^5 RAD(Si)
  - Transient Upset ..... $> 1 \times 10^8$ RAD(Si)/s (Ports and DDR)
  - Latch-Up Free ..... $> 1 \times 10^{12}$ RAD(Si)/s
- 2048 Words x 8 Bits ROM
- Electrically Equivalent to Sandia SA3002
- Pin Compatible with Intel 8355
- Bus Compatible with HS-80C85RH
- Single 5 Volt Power Supply
- Low Standby Current ..... 100mA Max
- Low Operating Current 2mA/MHz
- Completely Static Design
- Internal Address Latches
- Two General Purpose 8-Bit I/O Ports
- Multiplexed Address and Data Bus
- Self Aligned Junction Isolated (SAJI) Process
- Military Temperature Range..... -55°C to +125°C

Description

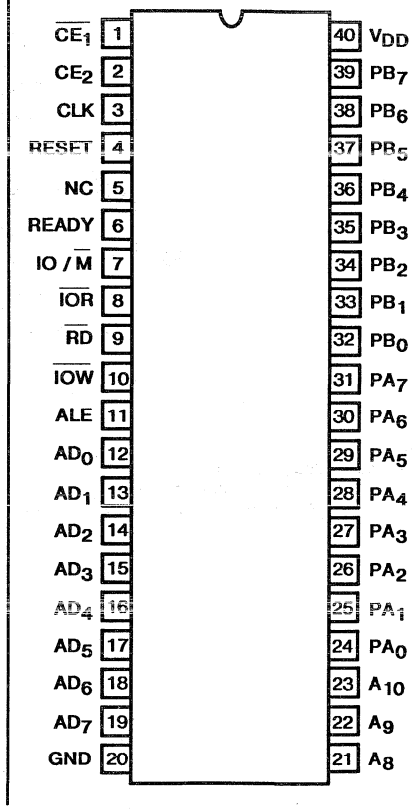
The HS-83C55RH is a radiation hardened ROM and I/O chip fabricated using the Harris radiation hardened Self-Aligned Junction Isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

The HS-83C55RH is intended for use with the HS-80C85RH radiation hardened microprocessor system.

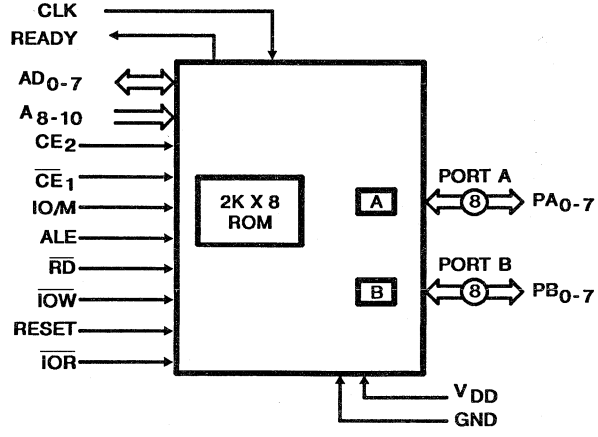
The ROM portion is designed as 16,384 mask programmable cells organized in a 2048 word x 8-bit format. A maximum post irradiation access time of 200ns allows the HS-83C55RH to be used with the HS-80C85RH CPU without any wait states. This ROM is designed for operation utilizing a single 5 volt power supply.

Pinout

TOP VIEW



Block Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Table 1. Pin Description

Symbol	Type	Name and Function
ALE	I	**Address Latch Enable:** When high, AD_{0-7}, $IO/\overline{M}$, A_{8-10}, CE_2, and $\overline{CE_1}$ enter the address latches. The signals (AD, $I/\overline{OM}$, A_{8-10}, CE_2, CE_1) are latched in at the trailing edge of ALE.*
AD_{0-7}	I	**Address/Data Bus (Bidirectional):** The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B is selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched chip enables are active, the output buffers present data on the bus.
A_{8-10}	I	**Address Bus:** High order bits of the ROM address. They do not affect I/O operations.
$\overline{CE_1}$ CE_2	I	**Chip Enable Inputs:** $\overline{CE_1}$ is active low and CE_2 is active high. The HS-83C55RH can be accessed only when *BOTH* Chip Enables are active at the time the ALE signal latches them in. If either Chip Enable input is not active, the AD_{0-7} and READY outputs will be in a high impedance state.
$IO/\overline{M}$	I	**I/O Memory:** If the latched $IO/\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low, the output data comes from the ROM.
$\overline{RD}$	I	**Read:** If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected ROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are 3-stated.
$\overline{IOW}$	I	**I/O Write:** If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of $IO/\overline{M}$ is ignored.
CLK	I	**Clock:** Used to force the READY into its high impedance state after it has been forced low by $\overline{CE_1}$ low, CE_2 high and ALE high.
READY	O	**READY:** A 3-state output controlled by $\overline{CE_1}$, CE_2, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK.
PA_{0-7}	I/O	**Port A:** General purpose I/O pins. Their input/output direction is determined by the contents of the Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0, AD_1. Read operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 and AD_1 low, *or* $IO/\overline{M}$ high, RD low, active chip enables, and AD_0 and AD_1, LOW.
PB_{0-7}	I/O	**Port B:** This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0 and a 0 from AD_1.
RESET	I	**Reset:** An input high causes all pins in Port A and B to assume input mode. (Clear DDR Register.)
$\overline{IOR}$	I	**I/O Read:** When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination $IO/\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC}.
V_{DD}	I	**Voltage:** +5 volt
GND	I	**Ground:** Ground Reference.

* ALE must be clocked once after power up.

Functional Description

ROM Section

The HS-83C55RH contains an 8-bit address latch which allows it to interface directly to the HS-80C85RH Microprocessor without additional hardware.

The ROM section of the chip is addressed by an 11-bit address and the Chip Enables. The address and levels on the Chip Enable pins are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and $IO/\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the ROM location addressed by the latched address are put out through AD_{0-7} output buffers.

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers (DDR) in the HS-83C55RH determine the input/output status of each pin in the corresponding ports. A "0" in a particular bit position of a DDR signifies that the corresponding I/O port bit is in the input mode. A "1" in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the HS-83C55RH are bit-by-bit programmable as inputs or outputs. The table summarizes port and DDR designation. DDR's cannot be read.

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD_{0-7} is written into the I/O port selected by the latched value of AD_{0-1}. During this operation all I/O bits of selected port are affected, regardless of their I/O mode and the state of $IO/\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high (glitch free output). A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with $IO/\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

To clarify the function of the I/O ports and Data Direction Registers, Figure 1 shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the output latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

Figure 1 also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

System Interface with HS-80C85RH

A system using the HS-83C55RH can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE_2 and $\overline{CE_1}$. By using a combination of unused address lines A_{11-15} and the Chip Enable inputs, the system can use up to 5 each HS-83C55RHs without requiring a CE decoder. See Figure 3.

If a memory mapped I/O approach is used the HS-83C55RH will be selected by the combination of both the Chip Enables and IO/M using AD_{8-15} address lines. See Figure 2.

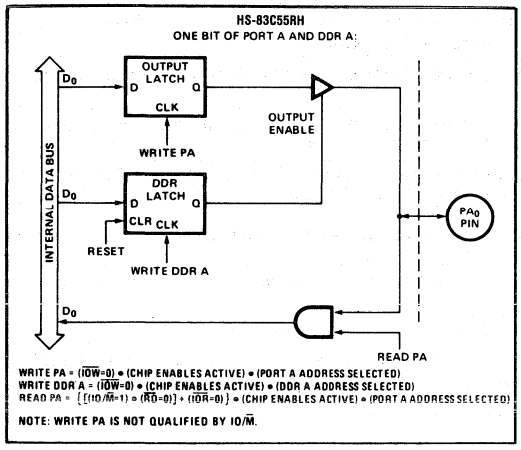


FIGURE 1. HS-83C55RH ONE BIT OF PORT A AND DDR A

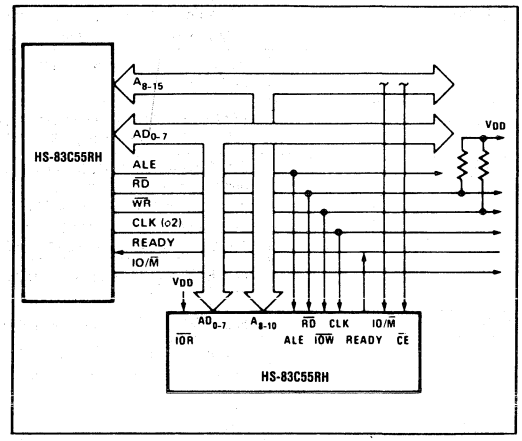
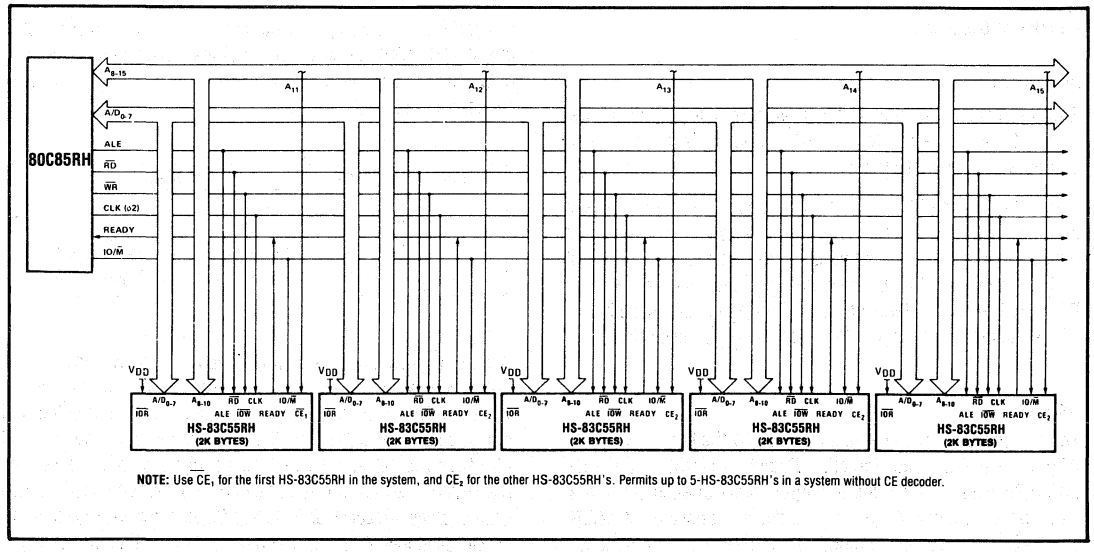


FIGURE 2. HS-83C55RH IN HS-80C85RH SYSTEM (MEMORY-MAPPED I/O)



NOTE: Use $\overline{CE_1}$ for the first HS-83C55RH in the system, and CE_2 for the other HS-83C55RH's. Permits up to 5-HS-83C55RH's in a system without CE decoder.

FIGURE 3. HS-83C55RH IN HS-80C85RH SYSTEM (STANDARD I/O)

Absolute Maximum Ratings*

Supply Voltage ..... + 7.0V.HS
Input or Output Voltage Applied ..... (GND-0.3V) to (V_{DD} + 0.3V)
Storage Temperature ..... -65°C to +150°C

Operating Range

Operating Supply Voltage ..... 4.75V to +5.25V
Operating Temperature ..... -55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

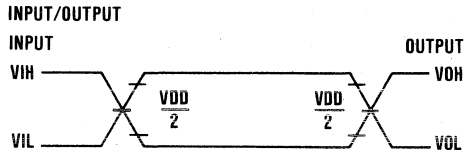
Electrical Specifications

	SYMBOL	PARAMETER	(Note 1) RADIATION, TEMPERATURE AND V_{DD} = OP. RANGE MIN	MAX	UNITS	TEST CONDITIONS
DC	V_{IL}	Input Low Voltage		0.8	V	V_{DD} = 4.75V
	V_{IH}	Input High Voltage	VDD -0.5		V	V_{DD} = 4.75V
	V_{OL}	Output Low Voltage		0.5	V	I_{OL} = 2mA, V_{DD} = 5.25V
	V_{OH}	Output High Voltage	V_{DD} -0.5		V	I_{OH} = -2mA, V_{DD} = 4.75V
	I_I	Input Leakage		±1.0	µA	V_{IN} = 0 or 5.25V, V_{DD} = 5.25V
	I_{DDSB}	Standby Current		100	µA	V_{DD} = 5.25 V
	I_{DDOP}	Operating Current Note 2		5	mA/MHz	V_{DD} = 5.25V, f = 1MHz
	IOZ	Output Leakage Current	-10	+10	µA	VO = V_{DD} or Gnd V_{DD} = 5.25V
AC	t_{CYC}	CLK Cycle Period	500		ns	Note 3
	t_1	CLK Pulse Width	40		ns	
	t_2	CLK Pulse Width	70		ns	
	t_r, t_f	CLK Rise and Fall Time		100	ns	
	t_{AL}	Address to Latch Set-Up Time	60		ns	
	t_{LA}	Address Hold Time After Latch	60		ns	
	t_{LC}	Latch to READ/WRITE Control	140		ns	
	t_{RD}	Valid Out Delay From READ Control*		140	ns	
	t_{AD}	Address Stable to Data Out Valid**		340	ns	
	t_{LL}	Latch Enable Width	120		ns	
	t_{RDF}	Data Bus Float After READ	0	110	ns	
	t_{CL}	READ/WRITE Control of Latch Enable	40		ns	
	t_{CC}	READ/WRITE Control Width	200		ns	
	t_{DW}	Data In to Write Setup Time	150		ns	
	t_{WD}	Data In Hold Time After WRITE	10		ns	
	t_{WP}	WRITE to Port Output		300	ns	
	t_{PR}	Port Input Setup Time	50		ns	
	t_{RP}	Port Input Hold Time	50		ns	
	t_{RYH}	READY HOLD Time	0	160	ns	
	t_{ARY}	ADDRESS CE to READY		160	ns	
	t_{RV}	Recovery Time Between Controls	300		ns	
	t_{RDE}	READ Control to Data Bus Enable	10		ns	

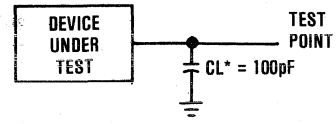
* Or T_{AD} - (T_{AL} + T_{LC}), whichever is greater. ** Defines ALE to Data Out Valid in conjunction with T_{AL}.

NOTES:
1. All devices guaranteed at worst case limits and over radiation.
2. Operating supply current (I_{DDOP}) is proportional to operating frequency.
3. Output timings are tested with purely capacitive load. Read and record data not available. (C_L = 170pF.)

A.C. Testing Input, Output Waveform



A.C. Testing Load Circuit (Note 3)



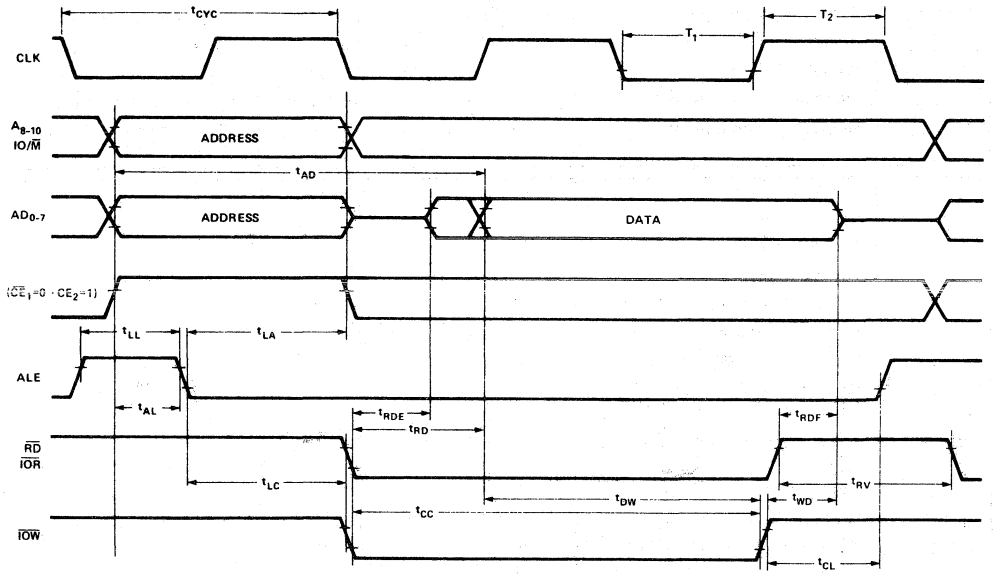
A.C. TESTING: All input signals must switch between V_{IL} max and V_{IH} min, t_r and t_f must be less than or equal to 15ns.

*C_L includes stray and jig capacitance.

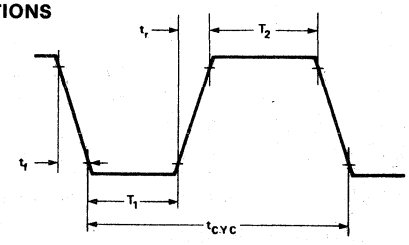
NOTES:
1. All devices guaranteed at worst case limits and over radiation.
2. Operating supply current (I_{DDOP}) is proportional to operating frequency.
3. Output timings are measured with purely capacitive load.
4. Devices screened to more rigorous electrical specifications are available. Contact your nearest Harris representative for details.

Waveforms

ROM READ AND I/O READ AND WRITE

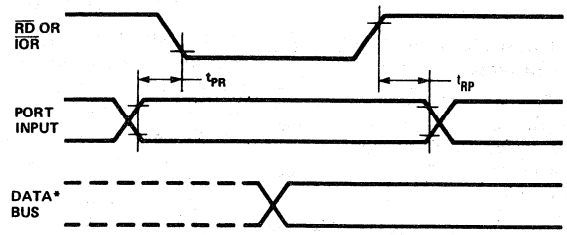


83C55RH CLOCK SPECIFICATIONS

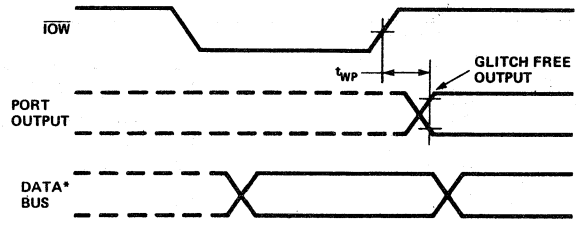


Waveforms

INPUT MODE

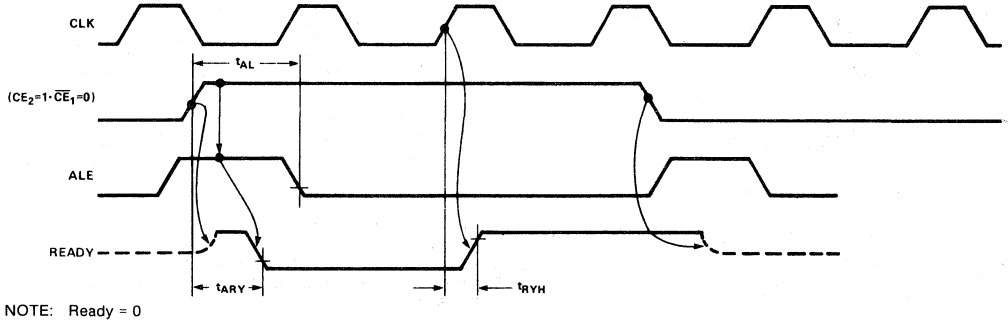


OUTPUT MODE



*DATA BUS TIMING IS SHOWN IN FIGURE 4.

WAIT STATE



NOTE: Ready = 0

Radiation Screening Procedure

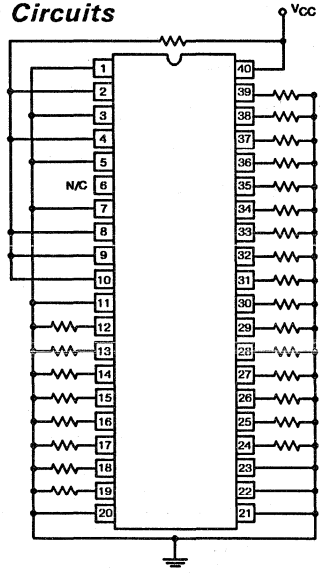
1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested to the customer's specification for proper operation.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad-Si (±10%) from a Gamma-cell 220 Cobalt 60 source or equivalent. The samples shall be biased at V_{DD} with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The lot will be accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-83C55RH has been designed to survive in a radiation environment and to meet the electrical characteristcs. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1×10^5 Rad-Si. Transient radiation tests have shown the following results:

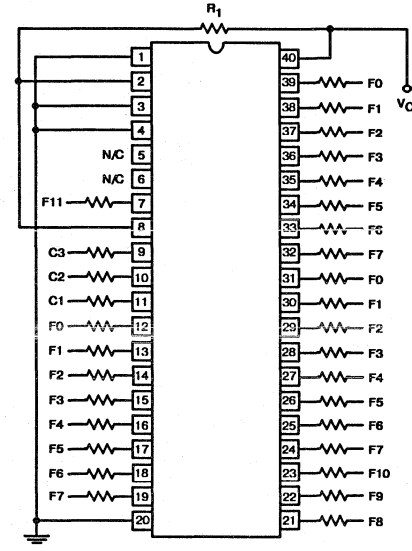
- Latch-up free to doses $\geq 1 \times 10^{12}$ rads/sec.
- Upset (loss of stored data) $\geq 10^8$ rads/sec.

Burn-In Circuits



STATIC CONFIGURATION

16K ROM, V_{CC} = 10V ± 10%
T_A Min = 125°C; All Resistors Are 10kΩ ± 10%, 1.4 Watt
Package: 40 Pin DIP; Package Code VB,
Part is Static Sensitive. Voltage Must Be Ramped.



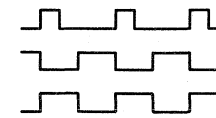
DYNAMIC CONFIGURATION

16K ROM, VCC = 10V ± 10%, T_A = 125°C; C2 = C3
R1 = 100kΩ ± 10%, 1/4 Watt. All Resistors are 10kΩ ± 10%, 1/4 Watt,
Unless Otherwise Noted. No Connection to Pins 5, 6
Package: 40 Pin DIP; Package Code VB, Part is Static Sensitive.
Voltage Must Be Ramped. 16K ROM.

NAME	FREQUENCY	DUTY CYCLE
C1	200kHz	20%
C2	200kHz	50%
C3	200kHz	50%

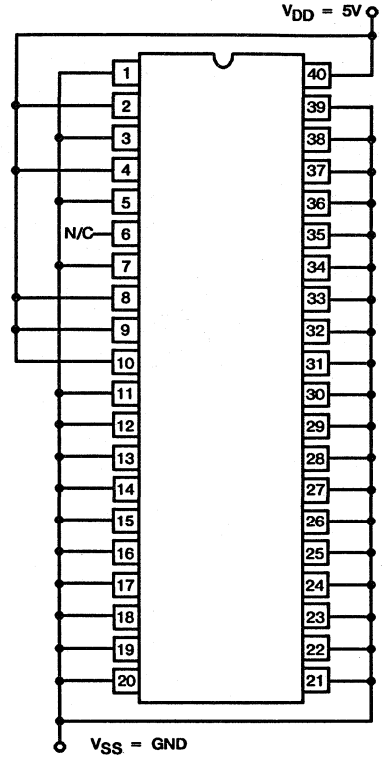
V_{IH} = 4.5V, V_{IL} = 0.8V

NAME	FREQUENCY	DUTY CYCLE
F0	100kHz	50%
F1	F0/2	50%
⋮	⋮	⋮
F11	F10/2	50%



Frequencies Fn Defined By: Fn = F(n-1)/2 Where F0 = 100kHz
e.g. F1 = 50kHz, F2 = 25kHz, . . . All Fn's have 50% Duty Cycle.
Note C3 = C2, Part is Static Sensitive.

Irradiation Circuit



RAD-HARD 10

COMMUNICATION CIRCUITS

HARRIS

HS-15530RH

Radiation Hardened CMOS Manchester Encoder-Decoder

July 1990

Features

- Functional Total Dose ..... 1×10^5 RAD(Si)
- Latch-Up Free to ..... 5×10^{11} RAD(Si)/s
- Support of MIL-STD-1553
- Low Operating Power ..... 50mW @ 5 Volts
- 1.0 Megabit/Sec Data Rate
- Sync Identification and Lock-in
- Clock Recovery
- Manchester II Encode, Decode
- Separate Encode and Decode
- Military Temperature Range..... -55°C to +125°C

Description

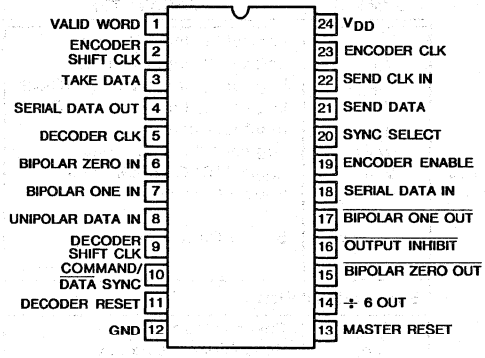
The Harris HS-15530 is a high performance, radiation resistant, CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset functions.

This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage while residing in a radiation environment. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

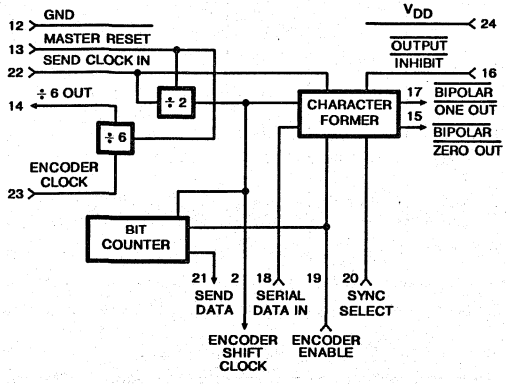
Pinout

DIP
TOP VIEW

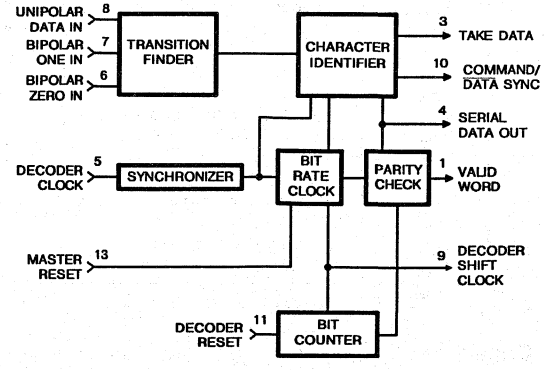


Block Diagrams

ENCODER



DECODER



10 COMMUNICATION CIRCUITS

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0 Volts
Input, Output or I/O Voltage Applied..... GND -0.3V to V_{DD} +0.3V
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range..... -55°C to +125°C

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications V_{DD} = +5.0V ± 10%, T_A = Operating Temperature Range

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	3.75			V	
	V_{IL}	Logical "0" Input Voltage			0.7	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{DD} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	I_I	Input Leakage	-1.0		+1.0	µA	$0V \leq V_{IN} \leq V_{DD}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA, V_{DD} = 4.5V
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA, V_{DD} = 4.5V
	I_{DDSB}	Supply Current Standby		0.5	2.0	mA	V_{IN} = 5.0V, V_{DD} = 5.5V Outputs Open
	I_{DDOP}	Supply Current Operating*		8.0	10.0	mA	V_{DD} = 5.5V, f = 1MHz
		(*Guaranteed and sampled but not 100% tested)					
	ENCODER TIMING						
A.C.	F_{EC}	Encoder Clock Frequency	0		13	MHz	C_L = 50pF
	F_{ESC}	Send Clock Frequency	0		2.16	MHz	
	T_{ECR}	Encoder Clock Rise Time			8	ns	
	T_{ECF}	Encoder Clock Fall Time			8	ns	
	F_{ED}	Data Rate	0		1.08	MHz	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{E1}	Shift Clock Delay			125	ns	
	T_{E2}	Serial Data Setup	75			ns	
	T_{E3}	Serial Data Hold	75			ns	
	T_{E4}	Enable Setup	90			ns	
	T_{E5}	Enable Pulse Width	100			ns	
	T_{E6}	Sync Setup	**55**			ns	
	T_{E7}	Sync Pulse Width	150			ns	
	T_{E8}	Send Data Delay	-10		50	ns	
	T_{E9}	Bipolar Ouput Delay			130	ns	
	DECODER TIMING						
A.C.	F_{DC}	Decoder Clock Frequency	0		13	MHz	C_L = 50pF
	T_{DCR}	Decoder Clock Rise Time			8	ns	
	T_{DCF}	Decoder Clock Fall Time			8	ns	
	F_{DD}	Data Rate	0		1.08	MHz	
	T_{DR}	Decoder Reset Pulse Width	150			ns	
	T_{DRS}	Decoder Reset Setup Time	75			ns	
	T_{MR}	Master Reset Pulse	150			ns	
	T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	(Note 1)
	T_{D2}	Sync Transition Span		$18T_{DC}$		ns	(Note 1)
	T_{D3}	One Zero Overlap			T_{DC} -10	ns	(Note 1)
	T_{D4}	Short Data Transition Span		$6T_{DC}$		ns	(Note 1)
	T_{D5}	Long Data Transition Span		$12T_{DC}$		ns	(Note 1)
	T_{D6}	Sync Delay (ON)		40	110	ns	
	T_{D7}	Take Data Delay (ON)		50	110	ns	
	T_{D8}	Serial Data Out Delay		80	80	ns	
	T_{D9}	Sync Delay (OFF)		90	110	ns	
	T_{D10}	Take Data Delay (OFF)		110	110	ns	
	T_{D11}	Valid Word Delay		90	110	ns	

NOTE 1. T_{DC} = Decoder Clock Period = $\frac{1}{FDC}$

Capacitance T_A = 25°C; V_{DD} = GND = 0V; V_{IN} = +5V or GND Guaranteed But Not 100% tested.

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5.0	pF	
C_O	Output Capacitance	8.0	pF	

Pin Description

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
2	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of Encoder Shift Clock.
3	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits.
4	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
5	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder, input a frequency equal to 12X the data rate.
6	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the Unipolar input is used.
8	I	UNIPOLAR DATA IN	Decoder	With pin 6 high and pin 7 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
9	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	I	GROUND	Both	Ground Supply pin.
13	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both Encoder and Decoder, and resets the ÷ 6 circuit.
14	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	$\overline{\text{BIPOLAR ZERO OUT}}$	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	$\overline{\text{OUTPUT INHIBIT}}$	Encoder	A low on this pin forces pin 15 and 17 high, the inactive states.
17	O	$\overline{\text{BIPOLAR ONE OUT}}$	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
20	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
21	O	SEND DATA	Encoder	An active high output which enables the external source of serial data.
22	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
23	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to the data rate X12 is usually input here.
24	I	VDD	Both	VDD is the +5V power supply pin. A 0.1μF decoupling capacitor from VDD (pin 24) to GROUND (pin 12) is recommended.

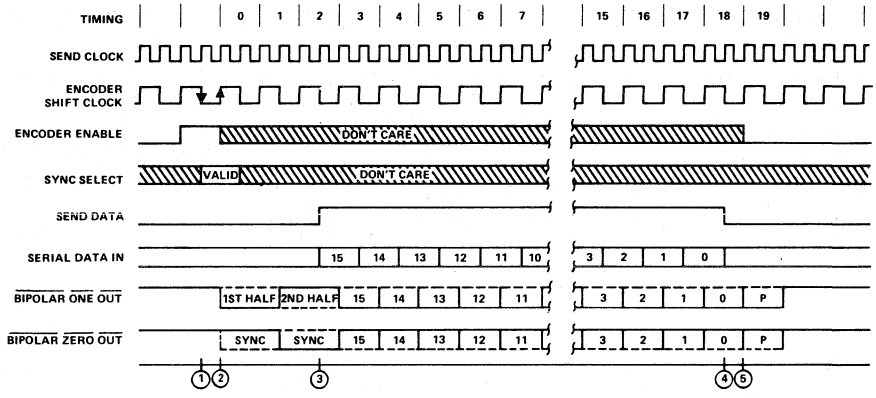
I = Input O = Output

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a command sync or a low will produce a data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③. During these sixten periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK so it can be sampled on the low-to-high transition ③ - ④. After the sync and Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ as shown to prevent a consecutive word from being encoded. At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



Decoder Operation

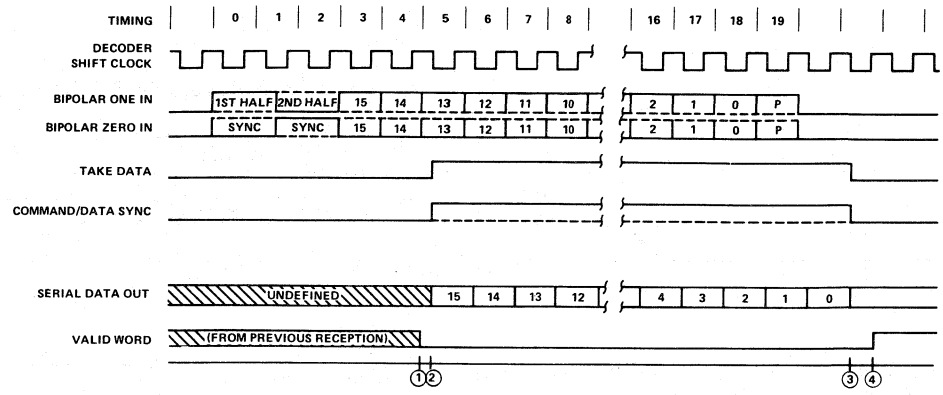
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ONE OUT}}$ of an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixten DECODER SHIFT CLOCK periods ③, otherwise it will remain low. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

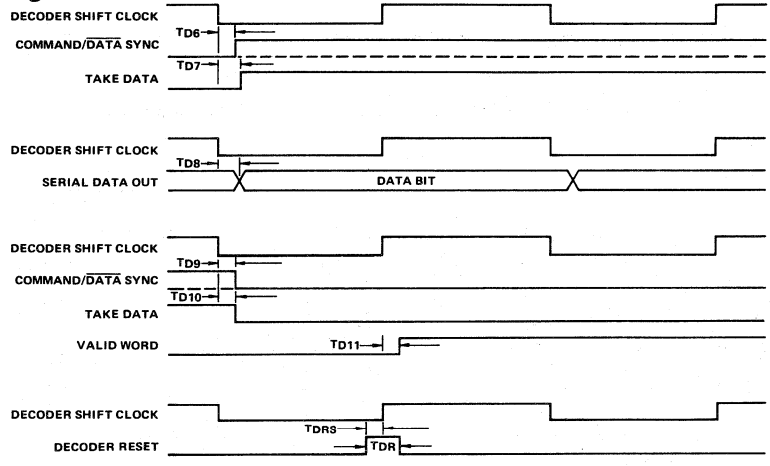
After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

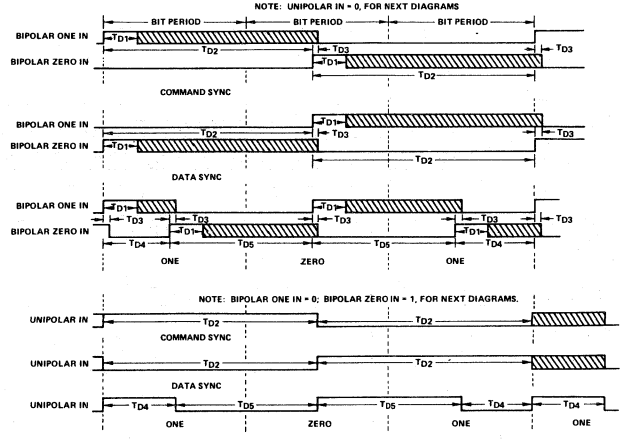
Decoder Operation (Continued)



Decoder Timing

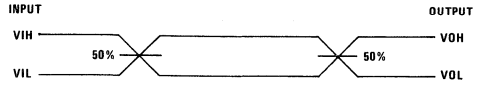


CONTROL SIGNALS



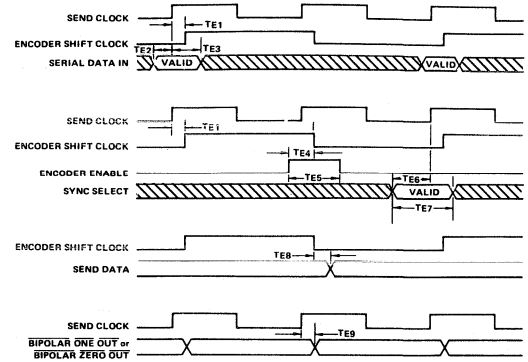
MANCHESTER INPUTS

A. C. Testing Input, Output Waveform



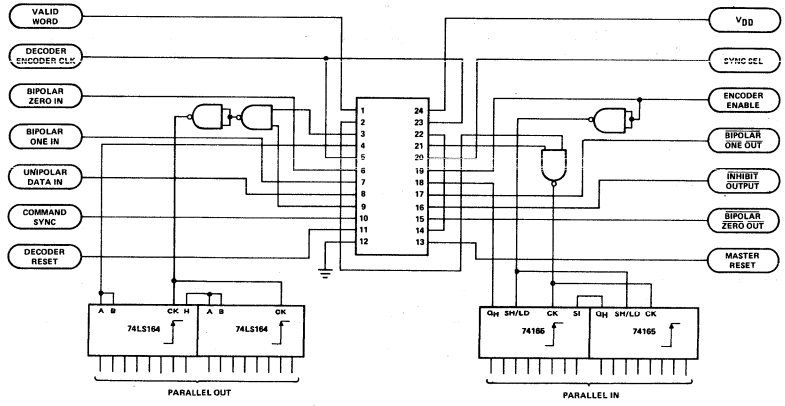
A. C. Testing: All input signals must switch between VIL and VIH. Input rise and fall times are driven at 1nsec per volt.

Encoder Timing

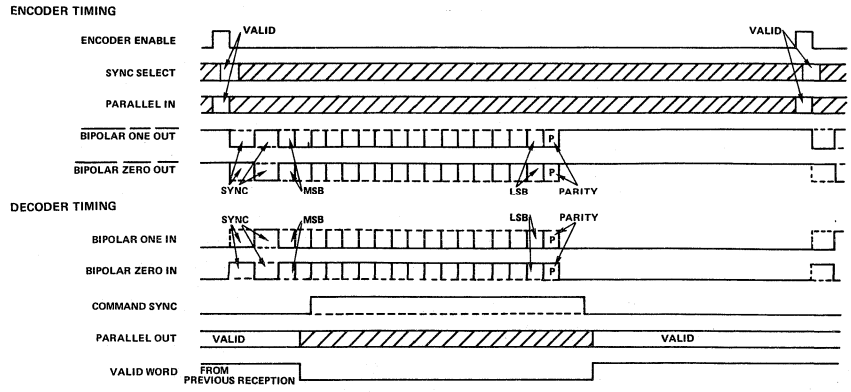


Applications

How to Make Our MTU Look Like a Manchester Encoded UART



Typical Timing Diagram for a Manchester Encoded UART



MIL-STD-1553

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HS-15530RH supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words. Terminals respond with Status Words. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20μsec. The word formats are shown in Figure 4. The special abbreviations are as follows:

P Parity, which is defined to be odd, taken across all 17 bits.

R/T Receive on logical zero, transmit on ONE.

ME Message Error if logical 1.

TF Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

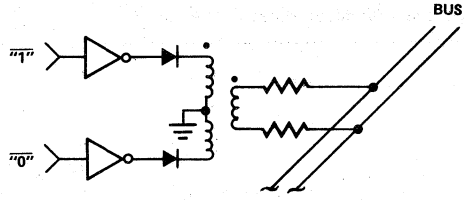


FIGURE 1. SIMPLIFIED MIL-STD-1553 DRIVER

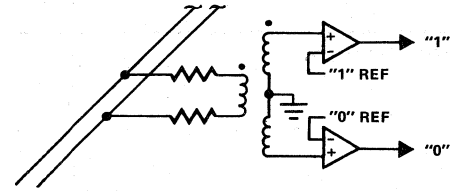


FIGURE 2. SIMPLIFIED MIL-STD-1553 RECEIVER

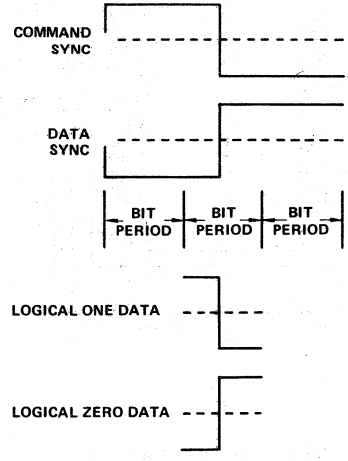


FIGURE 3. MIL-STD-1553 CHARACTER FORMATS

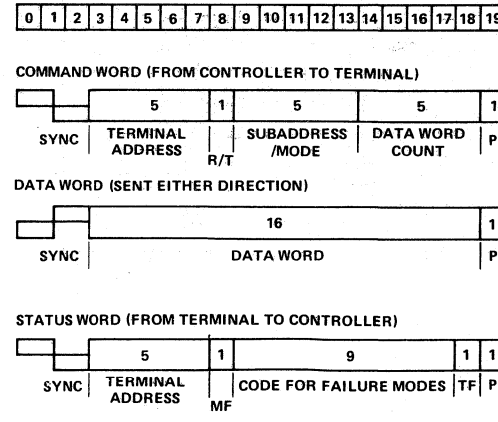


FIGURE 4. MIL-STD-1553 WORD FORMATS

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HS-15530RH.

Radiation Screening Procedure

1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad(Si) ±10% from a Gamma-cell 220 cobalt 60 source or equivalent. The samples shall be biased at 5V with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. I_{DDSB} at V_{DD} = 5V will be measured and recorded for each device within one hour (±15 minutes) after irradiation. The lot will be accepted only if the average of these measure values is ≤ 5mA.

Radiation Effects

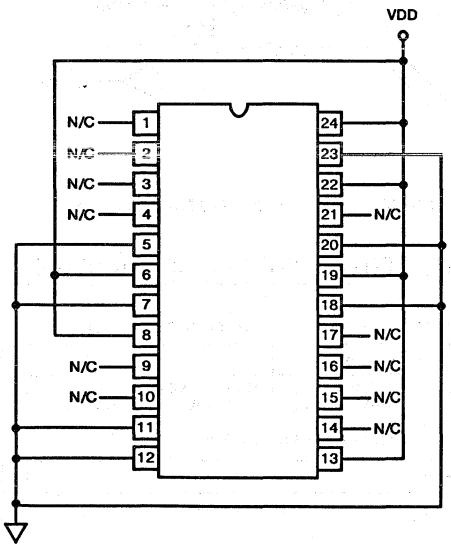
The HS-15530RH is processed with the same mask set as is used for the Harris equivalent commercial part. Latchup free operation is achieved by the use of epitaxial starting material, and improved total dose hardness is obtained with special processing cycles. These process techniques can, in principle, be applied to any standard Harris CMOS product.

The primary failure mode under exposure to ionizing radiation is an increase in static leakage current (IDDSB). Functional failure due to the increased leakage currents will typically occur for dose levels in excess of 5 x 10^5 RadSi. AC and DC parameters other than IDD will change less than 10p for total dose levels under 5 x 10^5 Rad-Si. The excess leakage currents will anneal at room temperature and are typically reduced by a factor of 3-10 within 24 hours after irradiation.

On a production basis, Harris is able to perform screens only for a total dose hardness. Transient radiation tests, however, have shown the following results:

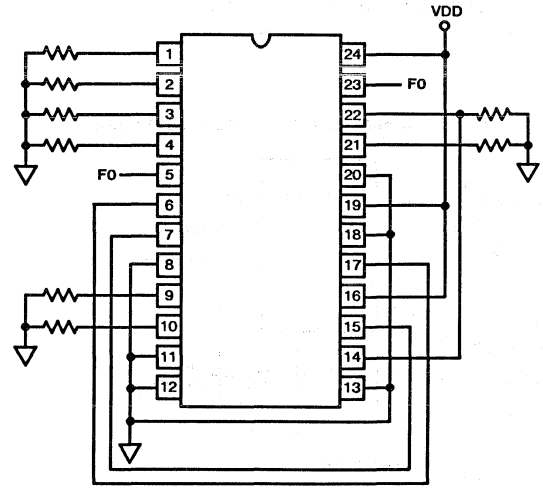
- Latchup free doses ≥ 5 x 10^{11} rads/sec.
- Upset (loss of stored data) ≥ 10^8 rads/sec.

Burn-In Circuits



STATIC CONFIGURATION

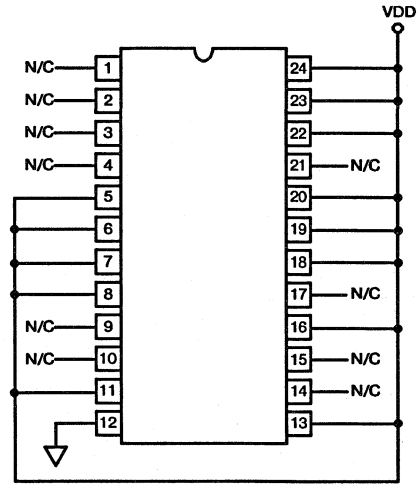
V_{DD} = 5.0V
I_{DD} < 2mA
T_A min = +125°C



DYNAMIC CONFIGURATION

V_{DD} = 5.0V
I_{DD} < 10mA
T_A min = +125°C
All resistors 1.8kΩ 1/4 watt
F_0 = 200KHz Square Wave; 50% Duty Cycle
V_{IL} = 0.5V
V_{IH} = 4.5V

Irradiation Circuit



RAD-HARD 11

MEMORIES

HARRIS

HS-6504RH

Radiation Hardened 4096 x 1 CMOS RAM

July 1990

Features

- Total Dose ..... 1×10^5 RAD (Si)
- Data Upset ..... $> 10^8$ RAD (Si)/s
- Latch-Up Free To ..... $> 1 \times 10^{12}$ RAD (Si)/s
- Low Power Standby ..... 1100µW Max
- Low Power Operation ..... 38.5mW/MHz Max
- Fast Access Time..... 150ns Typ
- Extremely Low Speed Power Product
- Single Event Upset Immune Option
- TTL Compatible Output
- Three-State Outputs
- Standard JEDEC Pinout
- 18 Pin Package for High Density
- On-Chip Address Register
- Military Temperature Range..... -55°C to +125°C

Description

The HS-6504RH is a synchronous 4096 x 1 static CMOS RAM fabricated using the radiation hardened guard band, self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices. On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

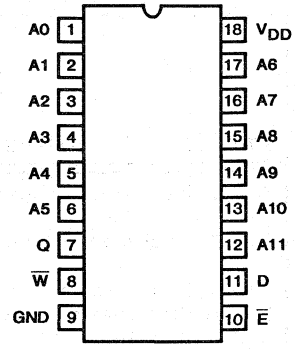
The HS-6504RH is a fully static RAM and may be maintained in any state for an indefinite period of time. A single event upset immune version of the HS-6504RRH is also offered. See page 11-5.

JAN

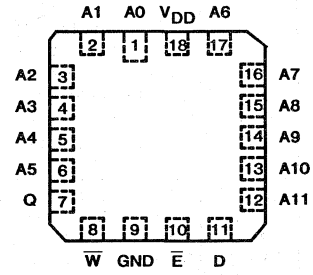
On January 28, 1987, Harris received JAN line certification as a Rad-Hard Class S fabrication facility for the HS-6504RH. Specifications can be found in JAN 38510/245 under device type 03.

Pinouts

CERAMIC DIP
TOP VIEW

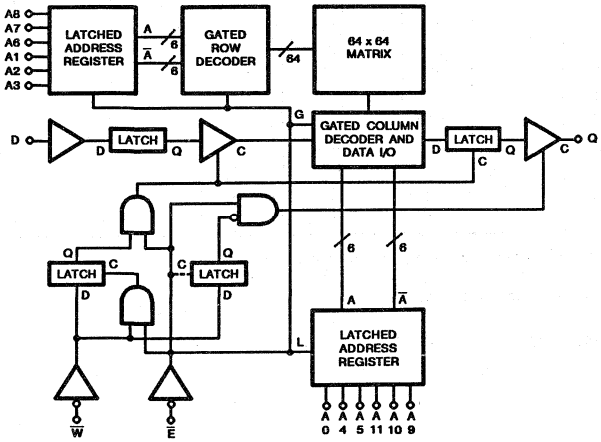


LCC/FLATPACK
TOP VIEW



A - Address Input D - Data Input
E - Chip Enable Q - Data Output
W - Write Enable

Functional Diagram



All lines Active High - Positive Logic
Three-State Buffers: C High → Output Active
Latches: C Low → Q = 0
Q Latches on Rising Edge of C

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage -(VDD-GND) ..... -0.3 to +7.0V
Input or Output Voltage Applied ..... GND -0.3V to VDD +0.3V
Storage Temperature ..... -65°C to +150°C

Operating Range

Operating Supply Voltage ..... 4.5V to 5.5V
Operating Temperature ..... -55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications ⑤

	SYMBOL	PARAMETER	TEMP & VDD = OPERATING RANGE ① MIN	TEMP & VDD = OPERATING RANGE ① MAX	TEMP = 25°C VDD = 5.0V TYPICAL PRE-RAD	TEMP = 25°C VDD = 5.0V TYPICAL POST 100K RADS	UNITS	TEST CONDITIONS
DC	IDDSB	Standby Supply Current		200	6	6	μA	IO = 0 VI = GND or VDD
	IDDOP	Operating Supply Current ②		7	4		mA	f = 1MHz, IO = 0 VI = VDD or GND
	IDDDR	Data Retention Current		100	4	4	μA	
	VDDDR	Data Retention Voltage		3.0	2.6	1.8	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	0.0	μA	GND≤VI≤ VDD
	IOZ	Output Leakage Current	-10	+10	±0.2	±0.2	μA	GND≤VO≤ VDD
	VIL	Input Low Voltage	-0.3	0.8	1.3	1.1	V	
	VIH	Input High Voltage All Except E and R/W	VDD -2.0	VDD +0.3	2.5	2.2	V	
	VIH	Input High Voltage E and R/W	VDD -1.5	VDD +0.3				
	VOL	Output Low Voltage		0.4	0.2	0.15	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		4.7	4.1	V	IOH = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	5.0	pF	VI = VDD or GND
	CO	Output Capacitance ③		10.0	6.0	6.0	pF	VO = VDD or GND f = 1MHz
AC	TELQV	Chip Enable Access Time		200	150	120	ns	④
	TAVQV	Address Access Time		210	150	120	ns	
	TELQX	Chip Enable/Output Enable Time ③		50	40	30	ns	
	TEHQZ	Chip Enable/Output Disable ③		50	40	30	ns	
	TELEH	Chip Enable Time	200		150	120	ns	
	TEHEL	Chip Disable Time	50		30	40	ns	
	TAVEL	Address Set-up Time	10		-10	0	ns	
	TELAX	Address Hold Time	40		20	30	ns	
	TWLWH	Write Enable Pulse Width	50		30	40	ns	
	TWLEH	Write Enable Set-up Time	200		140	160	ns	
	TWLEL	Early Write Pulse Set-up	0		-20	-10	ns	
	TWHEL	Read Mode Write Enable Set-up	0		-20	-10	ns	
	TELWH	Write Enable Hold Time	50		30	40	ns	
	TDVWL	Data Set-up Time	10		-10	0	ns	
	TDVEL	Early Write Data Set-up	0		-20	-10	ns	
	TWLDX	Data Hold Time	40		20	30	ns	
	TELDX	Early Write Data Hold	40		20	30	ns	
	TQVWL	Data Valid to Write Time	0		-20	-10	ns	
	TELEL	Read or Write Cycle Time	250		175	160	ns	

NOTES:
1. All devices guaranteed at worst case limits. Room temp., 5 volt data provided for information and not guaranteed. Post Rad Data at TD = 1 x 10^5
2. Operating Supply Current (IDDOP) is proportional to Operating Frequency.
3. Guaranteed — not tested.
4. AC test Conditions: Inputs: $T_{RISE} = T_{FALL} \leq 20$nsec; Outputs: 1 TTL Load and 50pF. All timing measurements at 1/2 VDD.
5. Pre-Radiation and Post-Radiation limits.

Absolute Maximum Ratings

Supply Voltage -(VDD-GND) ..... -0.3 to +7.0V
Input or Output Voltage Applied ..... GND -0.3V to VDD +0.3V
Storage Temperature ..... -65°C to +150°C

Operating Range

Operating Supply Voltage ..... 4.5V to 5.5V
Operating Temperature ..... -20°C to +80°C

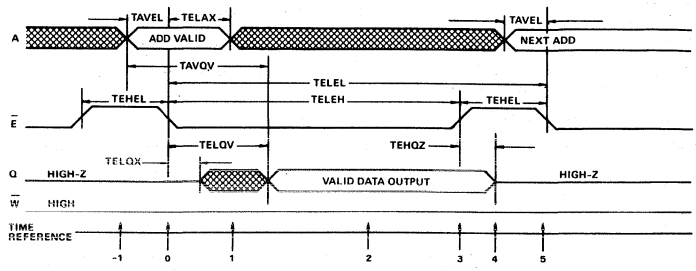
CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications ⑤

	SYMBOL	PARAMETER	TEMP & VDD = OPERATING RANGE ① MIN	TEMP & VDD = OPERATING RANGE ① MAX	TEMP = 25°C VDD = 5.0V TYPICAL PRE-RAD	TEMP = 25°C VDD = 5.0V TYPICAL POST 100K RADS	UNITS	TEST CONDITIONS
DC	IDDSB	Standby Supply Current		200	6	6	μA	IO = 0 VI = GND or VDD
	IDDOP	Operating Supply Current ②		7	4		mA	f = 1MHz, IO = 0 VI = VDD or GND
	IDDDR	Data Retention Current		100	4	4	μA	
	VDDDR	Data Retention Voltage ⑦		3.0	2.6	1.8	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	0.0	μA	GND≤VI≤ VDD
	IOZ	Output Leakage Current	-10	+10	±0.2	±0.2	μA	GND≤VO≤ VDD
	VIL	Input Low Voltage	-0.3	0.8	1.3	1.1	V	
	VIH	Input High Voltage All Except E and R/W	VDD -2.0	VDD +0.3	2.5	2.2	V	
	VIH	Input High Voltage E and R/W	VDD -1.5	VDD +0.3				
	VOL	Output Low Voltage		0.4	0.2	0.15	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		4.7	4.1	V	IOH = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	5.0	pF	VI = VDD or GND
	CO	Output Capacitance ③		10.0	6.0	6.0	pF	VO = VDD or GND f = 1MHz
AC	TELQV	Chip Enable Access Time		200	150	120	ns	④
	TAVQV	Address Access Time		210	150	120	ns	
	TELQX	Chip Enable/Output Enable Time ③		50	40	30	ns	
	TEHQZ	Chip Enable/Output Disable ③		50	40	30	ns	
	TELEH	Chip Enable Time	200		150	120	ns	
	TEHEL	Chip Disable Time	50		30	40	ns	
	TAVEL	Address Set-up Time	10		-10	0	ns	
	TELAX	Address Hold Time	40		20	30	ns	
	TWLWH	Write Enable Pulse Width	50		30	40	ns	
	TWLEH	Write Enable Set-up Time	200		140	160	ns	
	TWLEL	Early Write Pulse Set-up	0		-20	-10	ns	
	TWHEL	Read Mode Write Enable Set-up	0		-20	-10	ns	
	TELWH	Write Enable Hold Time	50		30	40	ns	
	TDVWL	Data Set-up Time	10		-10	0	ns	
	TDVEL	Early Write Data Set-up	0		-20	-10	ns	
	TWLDX	Data Hold Time	40		20	30	ns	
	TELDX	Early Write Data Hold	40		20	30	ns	
	TQVWL	Data Valid to Write Time	0		-20	-10	ns	
	TELEL	Read or Write Cycle Time	250		175	160	ns	

NOTES:
1. All devices guaranteed at worst case limits. Room temp., 5 volt data provided for information and not guaranteed. Post Rad Data at TD = 1 x 10^5
2. Operating Supply Current (IDDOP) is proportional to Operating Frequency.
3. Guaranteed — not tested.
4. AC test Conditions: Inputs: $T_{RISE} = T_{FALL} \leq 20$nsec; Outputs: 1 TTL Load and 50pF. All timing measurements at 1/2 VDD.
5. Pre-Radiation and Post-Radiation limits.

Read Cycle

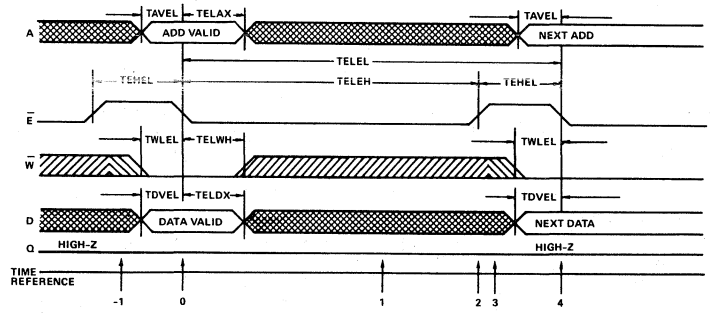


TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↑	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↑	X	X	X	Z	Write Completed
3	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
4	↓	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

NOTE: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Radiation Screening Procedure

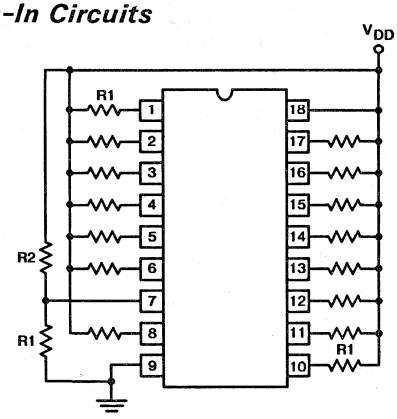
1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested to the customer's specification for proper operation.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad-Si (±10%) from a Gamma-cell 220 Cobalt 60 source or equivalent. The samples shall be biased at V_{DD} with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The wafers are accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact their local representative for details.

Radiation Effects

The HS-6504RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

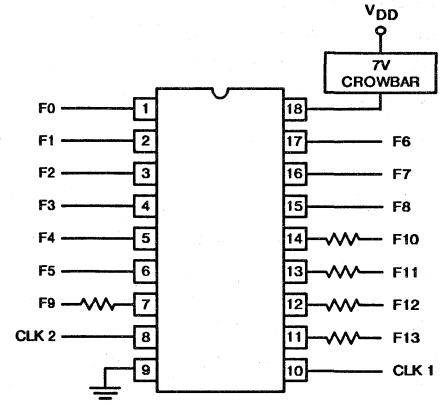
- Latch-up free to doses ≥ 1 x 10^{12} RAD/sec.
- Upset (loss of stored data) ≥ 10^8 RAD/sec.

Burn-In Circuits

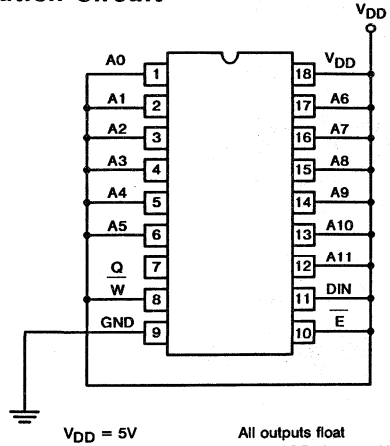


STATIC CONFIGURATION

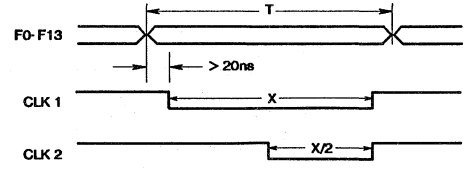
V_{DD} = 6.0V ± 0.5V R2 = 1.5K
R1 = 1K Minimum Ambient Temperature = +125°C



Irradiation Circuit



V_{DD} = 5V All outputs float
GND = 0V MONITOR: I_{DD} at 5V
All Inputs = 5V



DYNAMIC CONFIGURATION

V_{DD} = 6.0V ± 0.5V All Resistors = 27KΩ
Minimum Ambient Temperature = 125°C
V_{DD} must be applied before or at the same time as input signals
X > 700ns T = 5µs
F0 = 100kHz
F1 = F0/2
F2 = F0/4
F3 = F0/8 • • • F13 = F0/8192

HARRIS

HS-6508RH

July 1990

Radiation Hardened 1024 x 1 CMOS RAM

Features

- Functional Total Dose ..... 2×10^4 RAD (Si)
- Latch-Up Free To ..... $> 5.0 \times 10^{11}$ RAD (Si)/s
- Data Upset ..... $> 10^8$ RAD (Si)/s
- Low Standby Power ..... 550µW Max.
- Low Operating Power ..... 25mW/MHz Max.
- Fast Access Time ..... 300ns Max.
- TTL Compatible Outputs
- High Output Drive - 2 TTL Loads
- High Noise Immunity
- On-Chip Address Register
- Three-State Outputs
- 16 Pin Package for High Density
- Military Temperature Range ..... -55°C to +125°C

Description

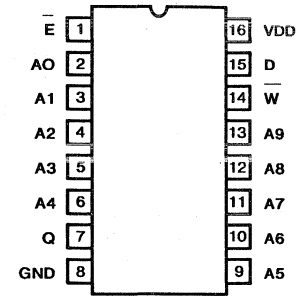
The Harris HS-6508RH is a 1024 by 1 static CMOS RAM fabricated using the Harris radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional CMOS devices.

On-Chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6508RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

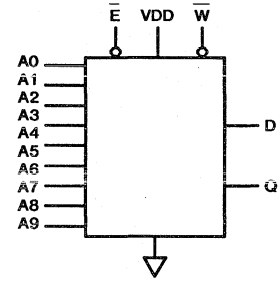
Pinout

TOP VIEW

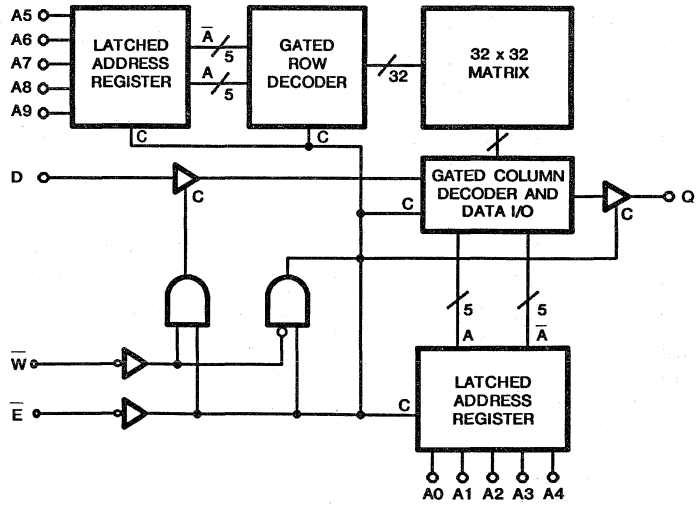


A - Address Input
D - Data Input
E - Chip Enable
Q - Data Output
W - Write Enable

Logic Symbol



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage -VDD .....-0.3V to 7.0V
Input or Output Voltage Applied.....GND -0.3V to VDD +0.3V
Storage Temperature.....-65°C to +150°C

Operating Range

Operating Supply Voltage -VDD .....4.5V to 5.5V
Operating Temperature.....-55°C to +125°C

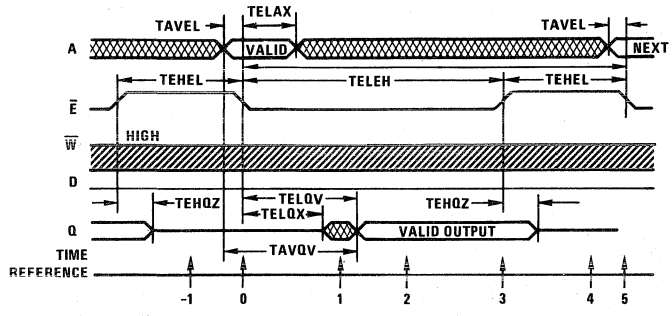
CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications ⑤

SYMBOL	PARAMETER	TEMP. & VDD = OPERATING RANGE		TEMP. = 25°C ① VDD = 5.0V			UNITS	TEST CONDITIONS
		MIN	MAX	MIN	TYP	MAX		
IDDSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VDD or GND
IDDOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VDD or GND
II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VDD
IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VDD
VIL	Input Low Voltage	-0.3	0.8	-0.3		1.5	V	
VIH	Input High Voltage	VDD-2.0	VDD+0.3	2.5	3.5	5.3	V	
VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -3mA
CI	Input Capacitance ③		6		4	6	pF	VI = VDD or GND f = 1MHz
CO	Output Capacitance ③		10		6	10	pF	VO = VDD or GND f = 1MHz
TELQV	Chip Enable Access Time		300		160	250	ns	④
TAVQV	Address Access Time		310		160	260	ns	④
TELQX	Chip Enable Output Enable Time ③		200		60	170	ns	④
TWLQZ	Write Enable Output Disable Time ③		200		60	170	ns	④
TEHQZ	Chip Enable Output Disable Time ③		200		60	170	ns	④
TELEH	Chip Enable Pulse Negative Width	300		250	160		ns	④
TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
TAVEL	Address Setup Time	10		10	0		ns	④
TELAX	Address Hold Time	70		50	40		ns	④
TDVWH	Data Setup Time	130		100	80		ns	④
TWHDX	Data Hold Time	0		0	0		ns	④
TWLEH	Chip Enable Write Pulse Setup Time	160		130	100		ns	④
TELWH	Chip Enable Write Pulse Hold Time	160		130	100		ns	④
TWLWH	Write Enable Pulse Width	160		130	100		ns	④
TELEL	Read or Write Cycle Time	450		380	250		ns	④

NOTES:
① All devices guaranteed at worst case limits. Room temperature, 5 volt data provided for information and not guaranteed.
② Operating Supply Current (IDDOP) is proportional to Operating Frequency. Example: Typical IDDOP = 1.5mA/MHz.
③ Guaranteed — not tested.
④ AC Test Conditions: Inputs — TRISE = TFALL ≤ 20ns; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VDD.
⑤ Pre-Radiation characteristics. See Radiation Effects for post radiation characteristics.

Read Cycle

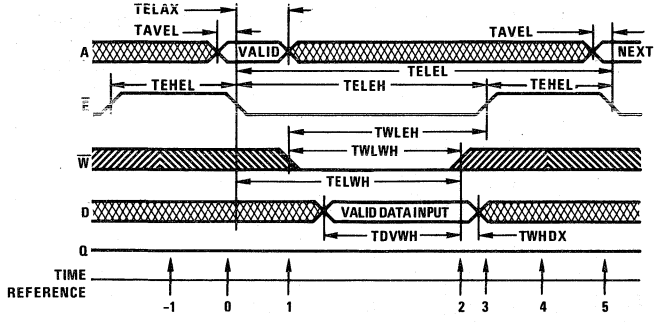


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	H	V	X	Z	Cycle Begins, Addresses Are Latched
1	L	H	X	X	X	Outputs Enabled
2	L	H	X	X	V	Output Valid
3	↑	H	X	X	V	Read Accomplished
4	H	X	X	X	Z	Prepare For Next Cycle (Same as -1)
5	↓	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the HA-6508RH Read Cycle the address information is latched into the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	X	V	X	Z	Cycle Begins, Addresses Are Latched
1	L	↓	X	X	Z	Write Period Begins
2	L	↑	X	V	Z	Data Is Written
3	↑	H	X	X	Z	Write Completed
4	H	X	X	X	Z	Prepare For Next Cycle (Same as -1)
5	↓	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on-chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the W line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times, within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

Radiation Screening Procedure

1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 2 x 10^4 Rad Si (±10%) from a Gammacell 220 Cobalt 60 sources or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. IDDSB at VDD = 5 volts will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the average of these measured values is < 10mA.

Radiation Effects

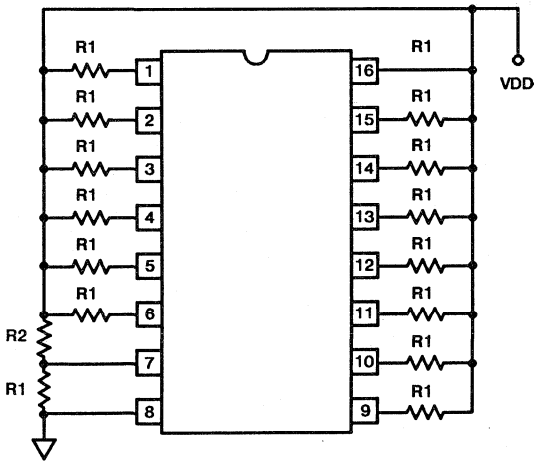
The HS-6508RH is a radiation hardened memory processed with the same mask set as is used for HARRIS' equivalent commercial part. Latchup free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. These process techniques can, in principle, be applied to any standard HARRIS CMOS product.

The primary failure mode under exposure to ionizing radiation is an increase in static leakage current (IDDSB). Functional failure due to the increased leakage currents will typically occur for dose levels in excess of 5 x 10^4 Rad-Si. The excess leakage currents will anneal at room temperature and are typically reduced by a factor of 3-10 within 24 hours after irradiation.

On a production basis, HARRIS is able to perform screens only for total dose hardness. Transient radiation tests, however, have shown the following results:

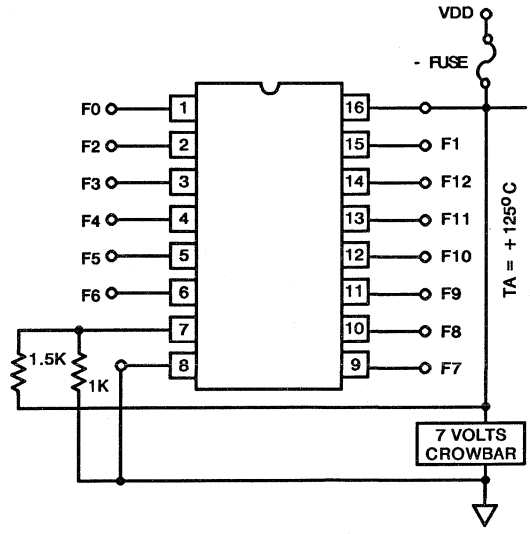
- Latchup free to doses ≥ 5 x 10^{11} RAD/sec.
- Upset (loss of stored data) typically > 10^8 RAD/sec.

Burn-In Circuits



STATIC CONFIGURATION

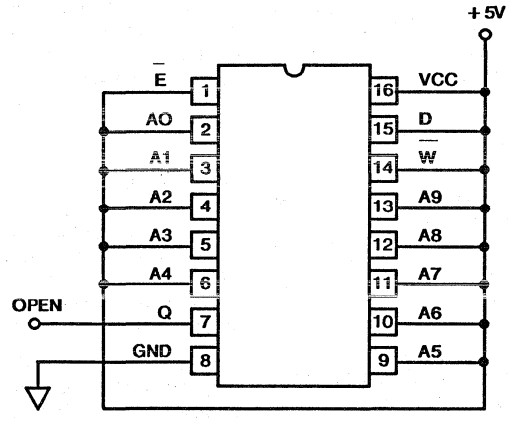
Minimum Ambient Temperature = +125°C
VDD = 6.0V ± 0.5V
R1 = 1K
R2 = 1.5K



DYNAMIC CONFIGURATION

All resistors are ± 20% 1/4W
Use standard crowbar circuit with + 7V zener diode
Driver 12 stage CMOS or equivalent
VDD = 6.0V ± 0.5V
F0 = 100kHz
F1 = F0/2
F2 = F0/4
F3 = F0/8
•
•
•
F12 = F0/4096

Irradiation Circuit



VDD = 5.0V
GND = 0V
All inputs = 5V
Q outputs float open

HARRIS

HS-6514RH

Radiation Hardened 1024 x 4 CMOS RAM

July 1990

Features

- Total Dose ..... 1×10^5 RAD (Si)
- Data Upset ..... $> 10^8$ RAD (Si)/s
- Latch-Up Free To ..... $> 1 \times 10^{12}$ RAD (Si)/s
- Low Power Standby ..... 1100µW Max
- Low Power Operation ..... 38.5mW/MHz Max
- Fast Access Time ..... 150ns Typ
- Single Event Upset Immune Option
- TTL Compatible Output
- Common Data I/O
- Three-State Outputs
- Standard JEDEC Pinouts
- 18 Pin Packages for High Density
- On-Chip Address Register
- Military Temperature Range ..... -55°C to +125°C

Description

The HS-6514RH is a synchronous 1024 x 4 static CMOS RAM fabricated using the Harris radiation hardened guard ring, self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

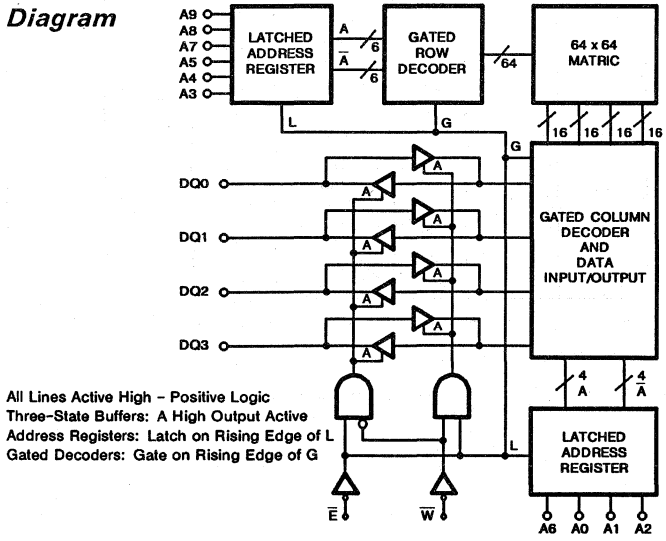
Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices. On-chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HS-6514RH is a fully static RAM and may be maintained in any state for an indefinite period of time. A single event upset immune version, the HS-6514RRH, is also available.

JAN

On January 28, 1987, Harris received JAN line certification as a Rad-Hard Class S fabrication facility for the HS-6514RH. Specifications can be found in JAN 38510/245 under device type 04.

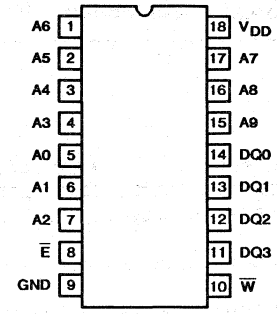
Functional Diagram



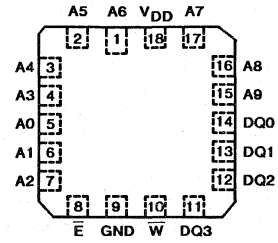
All Lines Active High - Positive Logic
Three-State Buffers: A High Output Active
Address Registers: Latch on Rising Edge of L
Gated Decoders: Gate on Rising Edge of G

Pinouts

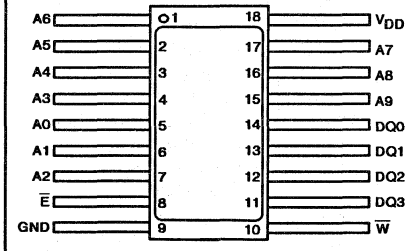
DIP
TOP VIEW



LCC
TOP VIEW



FLATPACK
TOP VIEW



A - Address Input
E - Chip Enable
W - Write Enable
DQ - Data In/Out

11 MEMORIES

Absolute Maximum Ratings

Supply Voltage -(VDD-GND) ..... -0.3 to +7.0V
Input or Output Voltage Applied..... GND -0.3V to VDD +0.3V
Storage Temperature.....-65°C to +150°C

Operating Range

Operating Supply Voltage.....4.5V to 5.5V
Operating Temperature .....-55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications ⑤

	SYMBOL	PARAMETER	TEMP & VDD OPERATING RANGE ① MIN	TEMP & VDD OPERATING RANGE ① MAX	TEMP = 25°C VDD = 5.0V TYPICAL PRE-RAD	TEMP = 25°C VDD = 5.0V TYPICAL POST 100K RADS	UNITS	TEST CONDITIONS
DC	IDDSB	Standby Supply Current		200	6	6	µA	IO = 0 VI = GND or VDD
	IDDOP	Operating Supply Current ②		7	4		mA	f = 1MHz, IO = 0 VI = VDD or GND
	IDDDR	Data Retention Current		100	4	4	µA	
	VDDDR	Data Retention Voltage		3.0	2.6	1.8	V	
	II	Input Leakage Current	-1.0	+1.0	0.0		µA	GND≤VI≤ VDD
	IIOZ	Input/Output Leakage Current	-10	+10	±0.2	±0.2	µA	GND≤VO≤ VDD
	VIL	Input Low Voltage	-0.3	0.8	1.3	1.1	V	
	VIH	Input High Voltage	VDD- 2.0	VDD +0.3	2.5	2.2	V	
	VOL	Output Low Voltage		0.4	0.2	0.15	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		4.7	4.1	V	IOH = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	5.0	pF	VI = VDD or GND
	CIO	Input/Output Capacitance ③		10.0	6.0	6.0	pF	VO = VDD or GND f = 1MHz
AC	TELQV	Chip Enable Access Time		225	150	120	ns	④
	TAVQV	Address Access Time		235	150	120	ns	
	TELQX	Chip Enable/Output Enable Time ③		75	50	40	ns	
	TWLQZ	Write Enable/Output Disable ③		75	50	40	ns	
	TEHQZ	Chip Enable/Output Disable ③		75	50	40	ns	
	TELEH	Chip Enable Time	225		150	180	ns	
	TEHEL	Chip Disable Time	75		40	50	ns	
	TAVEL	Address Set-up Time	10		-10	0	ns	
	TELAX	Address Hold Time	50		30	40	ns	
	TWLWH	Write Enable Pulse Width	225		150	180	ns	
	TWLEH	Write Enable Set-up Time	225		150	170	ns	
	TELWH	Write Enable Hold Time	225		150	170	ns	
	TDVWH	Data Set-up Time	190		140	160	ns	
	TWHDZ	Data Hold Time	50		10	20	ns	
	TWLEL	Early Output High-Z Time	0		-20	-10	ns	
	TEHWH	Late Output High-Z Time	0		-20	-10	ns	
	TELEL	Read or Write Cycle Time	300		200	190	ns	

NOTES:
1. All devices guaranteed at worst case limits. Room temp., 5 volt data provided for information and not guaranteed. Post Rad Data at TD = 1 x 10^5
2. Operating Supply Current (IDDOP) is proportional to Operating Frequency.
3. Guaranteed — not tested.
4. AC test Conditions: Inputs: $T_{RISE} = T_{FALL} \leq 20$nsec; Outputs: 1 TTL Load and 50pF. All timing measurements at ½ VDD.
5. Pre-Radiation and Post-Radiation limits.

Absolute Maximum Ratings

Supply Voltage -(VDD-GND) ..... -0.3 to +7.0V
Input or Output Voltage Applied ..... GND -0.3V to VDD +0.3V
Storage Temperature ..... -65°C to +150°C

Operating Range

Operating Supply Voltage ..... 4.5V to 5.5V
Operating Temperature ..... -20°C to +80°C

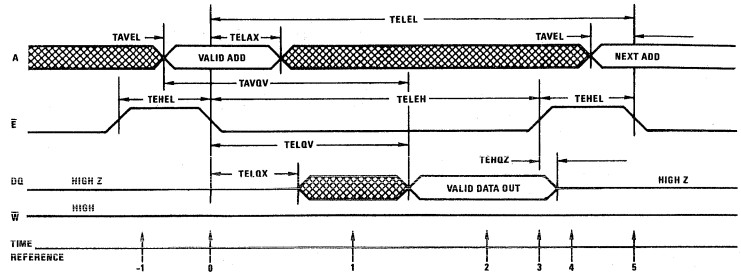
CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications ⑤

	SYMBOL	PARAMETER	TEMP & VDD OPERATING RANGE ① MIN	TEMP & VDD OPERATING RANGE ① MAX	TEMP = 25°C VDD = 5.0V TYPICAL PRE-RAD	TEMP = 25°C VDD = 5.0V TYPICAL POST 100K RADS	UNITS	TEST CONDITIONS
DC	IDDSB	Standby Supply Current		200	6	6	µA	IO = 0 VI = GND or VDD
	IDDOP	Operating Supply Current ②		7	4		mA	f = 1MHz, IO = 0 VI = VDD or GND
	IDDDR	Data Retention Current		100	4	4	µA	
	VDDDR	Data Retention Voltage ⑦		3.0	2.6	1.8	V	
	II	Input Leakage Current	-1.0	+1.0	0.0		µA	GND≤VI≤ VDD
	IIOZ	Input/Output Leakage Current	-10	+10	±0.2	±0.2	µA	GND≤VO≤ VDD
	VIL	Input Low Voltage	-0.3	0.8	1.3	1.1	V	
	VIH	Input High Voltage	VDD- 2.0	VDD +0.3	2.5	2.2	V	
	VOL	Output Low Voltage		0.4	0.2	0.15	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		4.7	4.1	V	IOH = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	5.0	pF	VI = VDD or GND
	CIO	Input/Output Capacitance ③		10.0	6.0	6.0	pF	VO = VDD or GND f = 1MHz
AC	TELQV	Chip Enable Access Time		225	150	120	ns	④
	TAVQV	Address Access Time		235	150	120	ns	
	TELQX	Chip Enable/Output Enable Time ③		75	50	40	ns	
	TWLQZ	Write Enable/Output Disable ③		75	50	40	ns	
	TEHQZ	Chip Enable/Output Disable ③		75	50	40	ns	
	TELEH	Chip Enable Time	225		150	180	ns	
	TEHEL	Chip Disable Time	75		40	50	ns	
	TAVEL	Address Set-up Time	10		-10	0	ns	
	TELAX	Address Hold Time	50		30	40	ns	
	TWLWH	Write Enable Pulse Width	225		150	180	ns	
	TWLEH	Write Enable Set-up Time	225		150	170	ns	
	TELWH	Write Enable Hold Time	225		150	170	ns	
	TDVWH	Data Set-up Time	190		140	160	ns	
	TWHDZ	Data Hold Time	50		10	20	ns	
	TWLEL	Early Output High-Z Time	0		-20	-10	ns	
	TEHWH	Late Output High-Z Time	0		-20	-10	ns	
	TELEL	Read or Write Cycle Time	300		200	190	ns	

NOTES:
1. All devices guaranteed at worst case limits. Room temp., 5 volt data provided for information and not guaranteed. Post Rad Data at TD = 1 x 10^5
2. Operating Supply Current (IDDOP) is proportional to Operating Frequency.
3. Guaranteed — not tested.
4. AC test Conditions: Inputs: $T_{RISE} = T_{FALL} \leq 20$nsec; Outputs: 1 TTL Load and 50pF. All timing measurements at ½ VDD.
5. Pre-Radiation and Post-Radiation limits.

Read Cycle

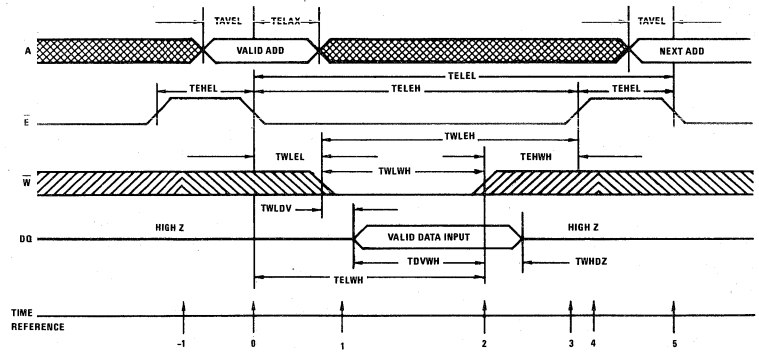


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT DQ	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↑	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	X	V	Z	Cycle Begins, Addresses are Latched
1	L	L	X	Z	Write Period Begins
2	L	↑	X	V	Data In is Written
3	↑	H	X	Z	Write Completed
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls.

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs will disable (three-state) after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rises.

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data output will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDZ become TDVEH and TEHDZ. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ & $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDV

If a series of consecutive write cycles are to be performed, W may be held low until all desired locations have been written (an extension of Case 2).

NOTE: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Radiation Screening Procedure

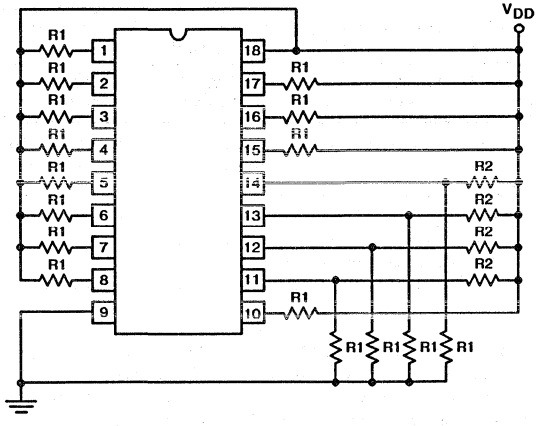
1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested to the customer's specification for proper operation.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad-Si (±10%) from a Gamma-cell 220 Cobalt 60 source or equivalent. The samples shall be biased at VDD with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The wafers are accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact their local representative for details.

Radiation Effects

The HS-6514RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

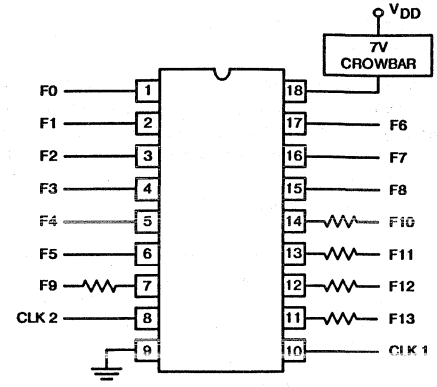
- Latch-up free to doses $\geq$ 1 x 10^{12} RAD/sec.
- Upset (loss of stored data) $\geq$ 10^8 RAD/sec.

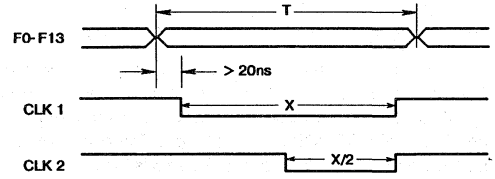
Burn-In Circuits



STATIC CONFIGURATION

V_{DD} = 6.0V ± 0.5V
R1 = 1K
R2 = 1.5K
Minimum Ambient Temperature = 125°C

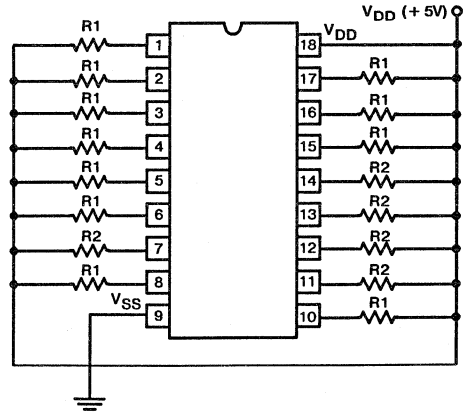




DYNAMIC CONFIGURATION

V_{DD} = 6.0V ± 0.5V
All Resistors = 27kΩ
Minimum Ambient Temperature = 125°C
V_{DD} must be applied before or at the same time as input signals
X > 700ns T = 5µs
F0 = 100kHz
F1 = F0/2
F2 = F0/4
F3 = F0/8 • • • F13 = F0/8192

Irradiation Circuit



V_{DD} = 5V
V_{SS} = 0V
All inputs = 5V
Monitor I_{DD} at V_{DD}
R1 = 47kΩ
R2 = 2.7kΩ

HARRIS

HS-6551RH

Radiation Hardened 256 x 4 CMOS RAM

July 1990

Features

- Functional Total Dose ..... 2×10^4 RAD (Si)
- Latch-up Free To..... $> 5.0 \times 10^{11}$ RAD (Si)/s
- Data Upset..... $> 10^8$ RAD (Si)/s
- Low Standby Power ..... 550µW Maximum
- Low Operating Power .....22mW/MHz Maximum
- Fast Access Time..... 300ns Maximum
  160ns Typical
- TTL Compatible Outputs
- High Output Drive 1TTL Load
- High Noise Immunity
- On Chip Address Register
- Three-State Outputs
- 22 Pin Package for High Density
- Military Temperature Range.....-55°C to +125°C

Description

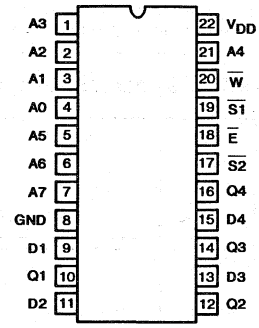
The HS-6551RH is a 256 by 4 static CMOS RAM fabricated using the Harris radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

On-chip latches are provided for addresses, and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6551RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

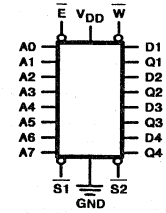
Pinout

TOP VIEW

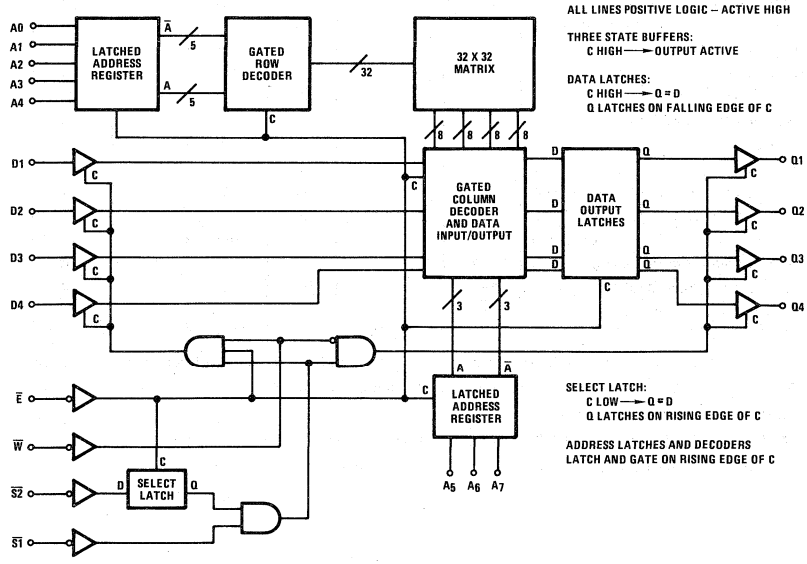


A - Address Input
E - Chip Enable
S - Chip Select
W - Write Enable
D - Data Input
Q - Data Output

Logic Symbol



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage -VDD ..... +7V
Applied Input or Output Voltage..... GND - 0.3V to VDD + 0.3V
Storage Temperature..... -65°C to +150°C

Operating Range

Operating Supply Voltage -VDD..... 4.5V to 5.5V

Operating Temperature..... -55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

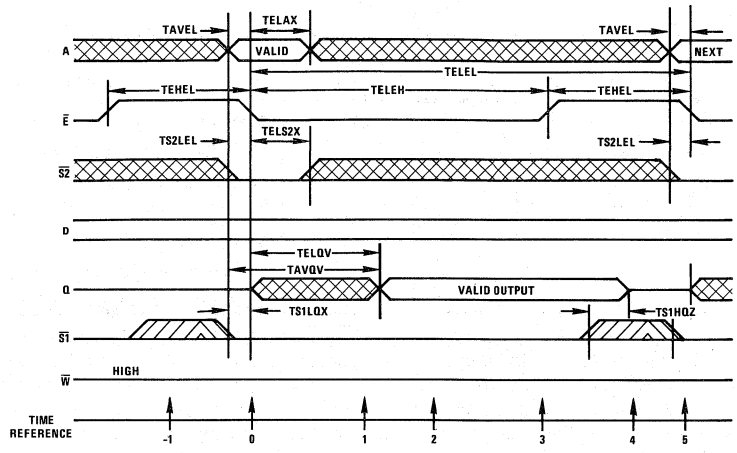
Electrical Specifications ⑤

	SYMBOL	PARAMETER	TEMP. & VDD = OPERATING ① RANGE MIN	TEMP. & VDD = OPERATING ① RANGE MAX	TEMP. = 25°C VDD = 5.0V MIN	TEMP. = 25°C VDD = 5.0V TYP	TEMP. = 25°C VDD = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	IDDSB	Standby Current		100		10	100	µA	IO = 0 VI = VDD or GND
	IDDOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VDD or GND
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VDD
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VDD
	VIL	Input Low Voltage	-0.3	0.8	-0.3	1.5	2.0	V	
	VIH	Input High Voltage	VDD -2.0	VDD +0.3	3.0	3.5	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.4	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -1.0mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VDD or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VI = VDD or GND f = 1MHz

A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		315		150	240	ns	④
	TS1LQX	Chip Select 1 Output Enable Time ③		150		60	120	ns	④
	TWLQZ	Write Enable Output Disable Time ③		150		60	120	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time ③		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		70	50		ns	④
	TAVEL	Address Setup Time	15		0	-10		ns	④
	TS2LEL	Chip Select 2 Setup Time	15		0	-10		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TELS2X	Chip Select 2 Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	180		150	120		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	315		180	200		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	300		180	200		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	195		150	120		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		150	120		ns	④
	TWLWH	Write Enable Pulse Width	180		150	120		ns	④
	TELEL	Read or Write Cycle Time	450		270	170		ns	④

NOTES:
① All devices tested at worst case limits. Room temperature 5 volt data provided for information — not guaranteed.
② Operating Supply Current (IDDOP) is proportional to Operating Frequency. Example: Typical IDDOP = 1.5mA/MHz.
③ Guaranteed — not tested.
④ AC Test Conditions: Inputs — TRISE = TFALL ≤ 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VDD.
⑤ Pre-radiation characteristics, see Radiation Effects for post-radiation characteristics.

Read Cycle



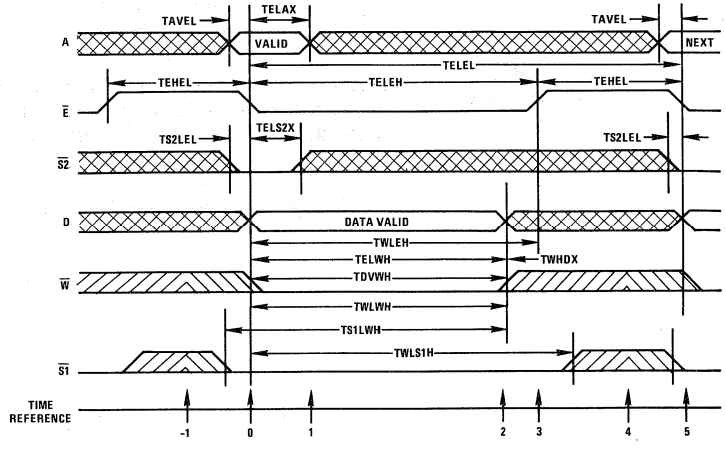
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTIONS
-1	H	H	X	X	X	X	Z	Memory Disable
0	↘	L	L	H	V	X	Z	Addresses and $\overline{S2}$ are Latched, Cycle Begins
1	L	L	X	H	X	X	X	Output Enabled But Undefined
2	L	L	X	H	X	X	V	Data Output Valid
3	↗	L	X	H	X	X	V	Outputs Latched, Valid Data
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The HS-6551RH Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on-chip registers providing that minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a higher order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV).

The HS-6551RH has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in the state until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTIONS
-1	H	H	X	X	X	X	Z	Memory Disable
0	↓	L	L	↓	V	X	Z	Cycle Begins, Addresses and $\overline{S2}$ are Latched
1	L	L	X	L	X	V	Z	Write Period Begins
2	L	L	X	↑	X	X	Z	Data in is Written
3	↑	L	X	H	X	X	Z	Write is Complete
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	L	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on-chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched low simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HS-6551RH may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

Radiation Screening Procedures

1. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 2×10^4 Rad Si (±10%) from a Gammacell 220 Cobalt 60 sources or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. IDDSB at VDD = 5 volts will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the average of these measured values is $\leq$ 10mA.

Radiation Effects

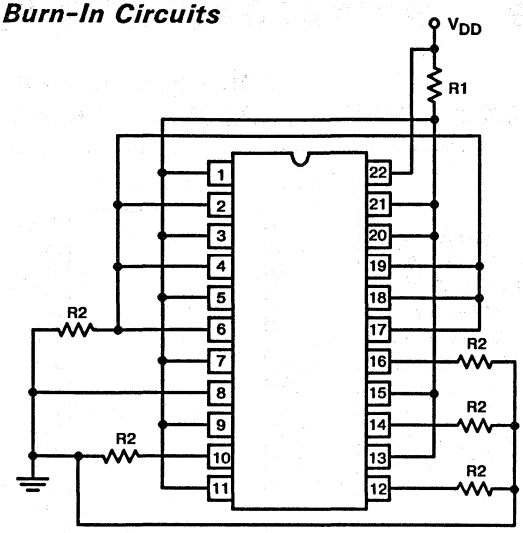
The HS-6551RH is a radiation hardened memory processed with the same mask set as is used for HARRIS' equivalent commercial part. Latchup free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. These process techniques can, in principle, be applied to any standard HARRIS CMOS product.

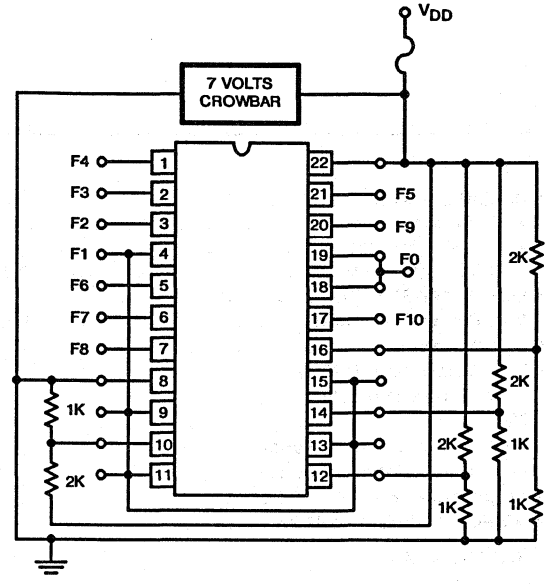
The primary failure mode under exposure to ionizing radiation is an increase in static leakage current (IDDSB). Functional failure due to the increased leakage currents will typically occur for dose levels in excess of 5×10^4 Rad-Si. The excess leakage currents will anneal at room temperature and are typically reduced by a factor of 3-10 within 24 hours after irradiation.

On a production basis, HARRIS is able to perform screens only for total dose hardness. Transient radiation tests, however, have shown the following results:

- Latchup free to doses $\geq 5 \times 10^{11}$ RAD/s.
- Upset (loss of stored data) typically $> 10^8$ RAD/s.

Burn-In Circuits





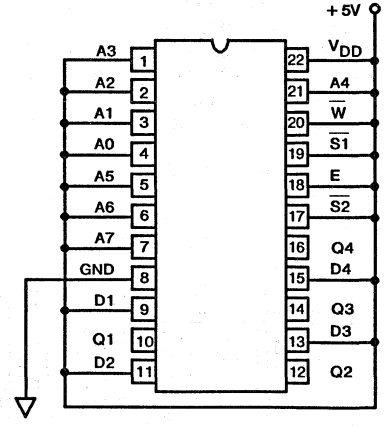
STATIC CONFIGURATION

Minimum Temp. 125°C
R_1 = 100K
R_2 = 10K
V_{DD} = 6.0V ± 0.5V
I_{DD} + 1.5mA

DYNAMIC CONFIGURATION

All resistors are ±20% 1/4W.
Use standard crowbar circuit with +7V zener diode.
Driver 10 stage CMOS or equivalent.
V_{DD} = 6.0V ± 0.5V
F0 = 100kHz
F1 = F0/2
F2 = F0/4 • • • F10 = F0/1024

Irradiation Circuit



V_{DD} = 5V
GND = 0V
All inputs = 5V
All Q outputs float open

HARRIS

HS-6564RH

July 1990

Radiation Hardened 8K x 8, 16K x 4 CMOS RAM Module

Features

- Radiation Hardened EPI CMOS
  - Total Dose ..... 1×10^5 RAD (Si)
  - Transient Upset ..... $> 1 \times 10^8$ RAD (Si)/s
  - Latch-Up Free to ..... $> 1 \times 10^{12}$ RAD (Si)/s
- Low Power Standby ..... 4.4mW Maximum
- Low Power Operation ..... 308mW/MHz Maximum
- Data Retention ..... 3.0V Minimum
- TTL Compatible In/Out
- Three State Outputs
- Fast Access Time..... 250ns Maximum
- Military Temperature Range..... -55°C to +125°C
- On Chip Address Registers
- Organizable 8K x 8 or 16K x 4
- 40 Pin DIP Pinout 2.000" x 0.900"

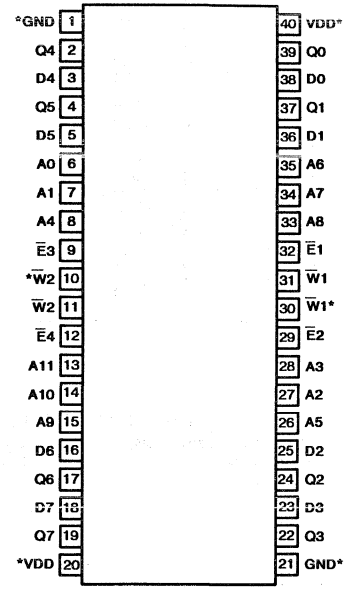
Description

The HS-6564RH is a radiation hardened 64K bit, synchronous CMOS RAM module. It consists of 16 HS-6504RH 4K x 1 radiation hardened CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The individual RAMs are fabricated using the Harris radiation hardened guard ring, self-aligned silicon gate technology. The HS-6564RH is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K x 1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are seperate for each block of RAM. This allows the user to organize the HS-6564RH RAM as either an 8K by 8 or a 16K by 4 array.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HS-6564RH is intended for use in radiation environments where a large amount of RAM is needed, and where power consumption and board space are prime concerns. On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile readswrite memory by using very small batteries mounted directly on the memory circuit board.

Pinout

TOP VIEW

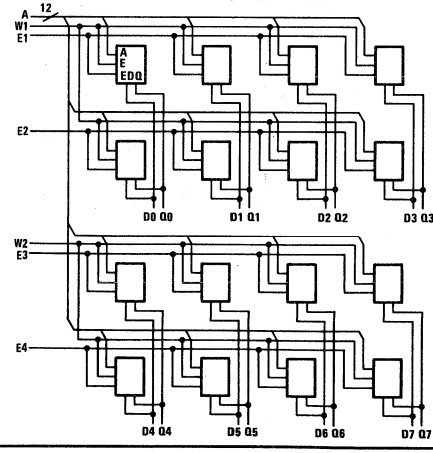


*NOTES:

Pins 20 and 40 (VDD) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect both VDD pins and both Ground pins to the board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31. For those users wishing to preserve board compatibility with possible future RAM arrays, we recommend connections to the write lines be made at pins 11 and 31, leaving pins 10 and 30 free for future expansion.

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings*

Supply Voltage - (VDD - GND) .....-0.3V to +7.0V
Input or Output Voltage Applied.....(GND -0.3V) to (VDD +0.3V)
Storage Temperature.....-65°C to +150°C

Operating Range

Operating Supply Voltage..... +4.5V to +5.5V
Operating Temperature.....-55°C to +125°C

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.

Electrical Specifications (Note 4)

			RAD. TEMP. & VDD = OPERATING RANGE (Note 1)		TYPICAL TEMP. = +25°C VDD = 5.0V			
	SYMBOL	PARAMETER	MIN	MAX	PRE RAD	POST RAD	UNITS	TEST CONDITIONS
D.C.	IDDSB	Standby Supply Current		1600	96	96	μA	IO = 0 VI = VDD or GND
	IDDOP1	Operating Supply Current (8K x 8) (Note 2)		56	32		mA	f = 1MHz, IO = 0 VI = VDD or GND
	IDDOP2	Operating Supply Current (16K x 4) (Note 2)		28	16		mA	f = 1MHz, IO = 0 VI = VDD or GND
	IDDDR	Data Retention Supply Current		1200	64	64	μA	IO = 0, VDD = 3.0 VI = VDD or GND
	VDDDR	Data Retention Supply Current	3.0		2.6	1.8	V	
	IIA	Address Input Leakage	-20	+20			μA	GND ≤ VI ≤ VDD
	IID1	Data Input Leakage (8K x 8)	-3	+3			μA	GND ≤ VI ≤ VDD
	IID2	Data Input Leakage (16K x 4)	-5	+5			μA	GND ≤ VI ≤ VDD
	IIE1	Enable Input Leakage (8K x 8)	-10	+10			μA	GND ≤ VI ≤ VDD
	IIE2	Enable Input Leakage (16K x 4)	-5	+5			μA	GND ≤ VI ≤ VDD
	IIW	Write Enable Input Leakage (Each)	-10	+10			μA	GND ≤ VI ≤ VDD
	IOZ1	Output Leakage (8K x 8)	-20	+20	±4	±4	μA	GND ≤ VO ≤ VDD
	IOZ2	Output Leakage (16K x 4)	-40	+40	±8	±8	μA	GND ≤ VO ≤ VDD
	VIL	Input Low Voltage		0.8	1.5	1.3	V	
	VIH1	Input High Level (Except $\overline{E}$ and $\overline{W}$)	VDD -1.5		2.7	2.5	V	
	VIH2	Input High Level ($\overline{E}$ and $\overline{W}$)	VDD -1.0		2.9	2.1	V	
	VOL	Output Low voltage		0.4	0.2	0.15	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.6	4.0	V	IO = -1.0mA
	CIA	Address Input Capacitance (Note 3)		200			pF	f = 1MHz VI = VDD or GND
	CID1	Data Input Capacitance (8K x 8) (Note 3)		50			pF	f = 1MHz VI = VDD or GND
	CID2	Data Input Capacitance (16K x 4) (Note 3)		100			pF	f = 1MHz VI = VDD or GND
	CIE1	Enable Input Capacitance (8K x 8) (Note 3)		160			pF	f = 1MHz VI = VDD or GND
	CIE2	Enable Input Capacitance (16K x 4) (Note 3)		80			pF	f = 1MHz, VI = VDD or GND
	CIW	Write Enable Input Capacitance (Each) (Note 3)		100			pF	f = 1MHz, VI = VDD or GND
	CO1	Output Capacitance (8K x 8) (Note 3)		50			pF	f = 1MHz VO = VDD or GND
	CO2	Output Capacitance (16K x 4) (Note 3)		100			pF	f = 1MHz, VO = VDD or GND

NOTES:

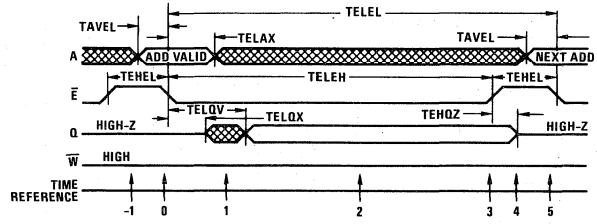
1. Each individual RAM in the leadless chip carrier is fully tested to worst case limits over temperature and voltage. The complete assembled HS-6564RH array is tested at room temperature only. The worst case parameters are guaranteed over the specified temperature and voltage ranges. Room temperature, 5 volt data is provided for information purposes and is not guaranteed.
2. Operating supply current is proportional to operating frequency. IDDOP is specified at an operating frequency of 1MHz, indicating repetitive accessing at a 1μs rate. Operating at slower rates will decrease IDDOP proportionally.
3. Guaranteed — not tested.
4. Pre-Radiation and Post Radiation limits.

Electrical Specifications

	SYMBOL	PARAMETER	RAD. TEMP. & VDD = OPER. RANGE MIN	RAD. TEMP. & VDD = OPER. RANGE MAX	TYPICAL TEMP. = +25°C VDD = 5.0V PRE RAD	TYPICAL TEMP. = +25°C VDD = 5.0V POST RAD	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access		350	200	215	ns	(Note 5)
	TAVQV	Address Access (TAVQV = TELQV + TAVEL)		400	220	240	ns	
	TELQX	Output Enable (Note 3)		75	50	55	ns	
	TEHQZ	Output Disable (Note 3)		75	50	55	ns	
	TELEL	Read or Write Cycle	480		250	275	ns	
	TELEH	Chip Enable Low	350		200	215	ns	
	TEHEL	Chip Enable High	130		50	60	ns	
	TAVEL	Address Setup	50		20	30	ns	
	TELAX	Address Hold	50		30	35	ns	
	TWLWH	Write Enable Low	150		50	55	ns	
	TWLEH	Write Enable Setup	250		175	175	ns	
	TWLEL	Early Write Setup	10		-5	0	ns	
	TELWX	Early Write Hold Time	100		40		ns	
	TDVWL	Data Setup	10		-5	0	ns	
	TDVEL	Early Write Data Setup	90		-5	0	ns	
	TWLDX	Data Hold	100		30	35	ns	
	TELDX	Early Write Data Hold	100		30	35	ns	
	TQVWL	Data Valid to Write (Read-Modify-Write)	100		0	0	ns	
	TELWH	Early Write Pulse Hold Time	250		50	55	ns	(Note 5)

NOTES: 5. AC Test Conditions: Inputs — $T_{RISE} = T_{FALL} \leq 20ns$. Timing measured at 1/2 VDD
Outputs — CLOAD = 50pF

Read Cycle

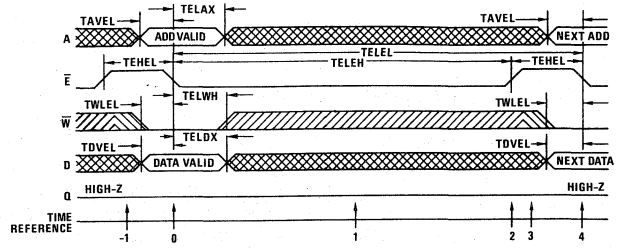


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	INPUTS W̄	INPUTS A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

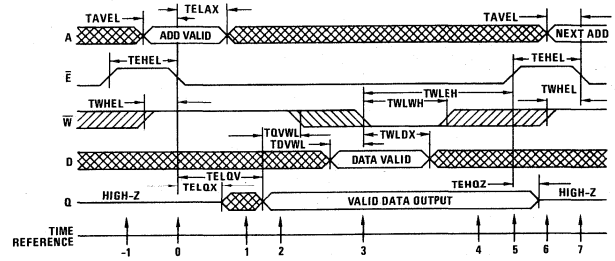


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↑	X	X	X	Z	Write Completed
3	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
4	↓	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of Ē (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of W̄ at the time Ē falls determines the state of the output buffer for the cycle. Since W̄ is low when Ē falls, the output buffer is latched into the high impedance state and will remain in that state until Ē returns high (T = 2). For this cycle, the data input is latched by Ē going low; therefore data set up and hold times should be referenced to Ē. When Ē (T = 2) returns to the high state, the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	X	Output Enabled
2	L	H	X	X	V	Output Valid, Read and Modify Time
3	L	↓	X	V	X	Write Begins, Data is Latched
4	L	H	X	X	V	Write in Progress Internally
5	↑	X	X	X	V	Write Completed
6	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
7	↓	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The read modify write cycle begins as all other cycles on the falling edge of Ē (T = 0). The W̄ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the W̄ (T = 3) the data present at the output and input are latched. The W̄ signal also latches itself on its low going edge. All input signals excluding Ē have been latched and have no further effect on the RAM. The rising edge of Ē (T = 5) completes the write portion of the cycle and unlatches all inputs and output. The output goes to a high impedance and the RAM is ready for the next cycle.

NOTES: In the above descriptions the numbers in parenthesis (T = n) refers to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Organization Guide

To Organize 8K x 8:

Connect: $\overline{E1}$ with $\overline{E3}$ (Pins 9 + 32)
$\overline{E2}$ with $\overline{E4}$ (Pins 12 + 29)
$\overline{W1}$ with $\overline{W2}$ (Pins 11 + 31)

To Organize 16K x 4:

Connect: Q0 with Q4 (Pins 2 + 39)
D0 with D4 (Pins 3 + 38)
Q1 with Q5 (Pins 4 + 37)
D1 with D5 (Pins 5 + 36)
D2 with D6 (Pins 16 + 25)
Q2 with Q6 (Pins 17 + 24)
D3 with D7 (Pins 18 + 23)
Q3 with Q7 (Pins 19 + 22)
Optional $\overline{W1}$ may be common with $\overline{W2}$ 11 (Pins 11 + 31)

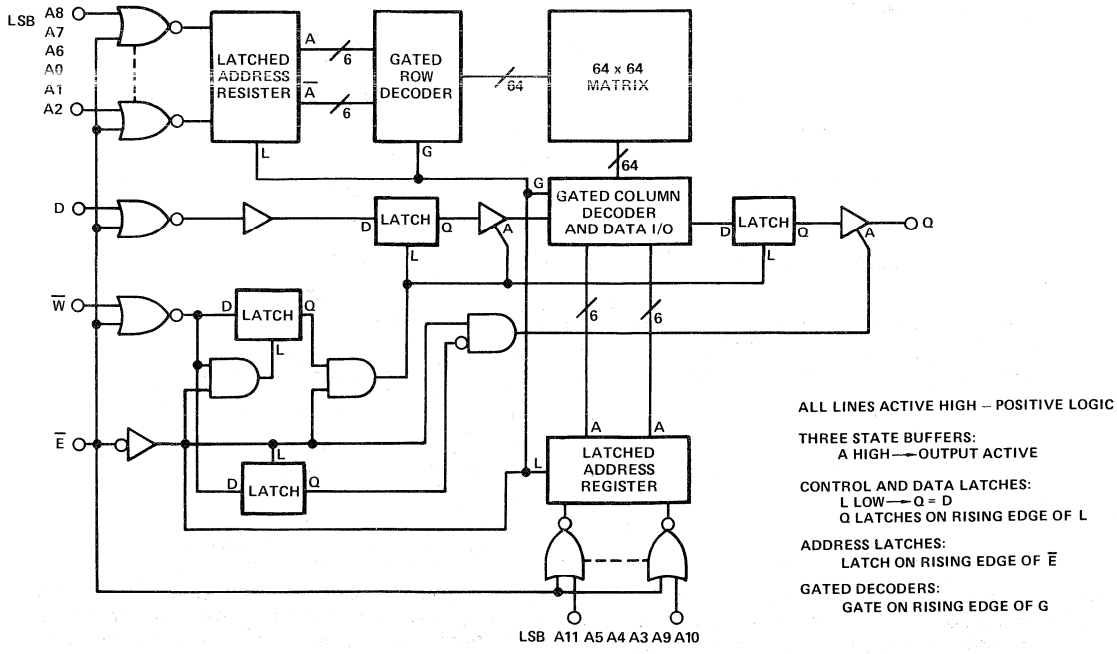
Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 8K x 8 mode, use the chip enables as if there were only two, $\overline{E1}$ and $\overline{E2}$. In the 16K x 4 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HS-6564RH have conductive lids. These lids are electrically floating, not connected to VDD or GND. The designer should be aware of the possiblity that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

HS-6504RH (One of Sixteen)



Board Size Tradeoffs

Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

The following table compares board space for 16 standard DIP 4K RAMs to the HS-6564RH RAM array. Both fine line, close tolerance layout and standard "easy" layout board sizes are shown in the comparison.

64K ARRAY OR 16 4K RAMs ON A PC BOARD vs. THE HS-6564RH

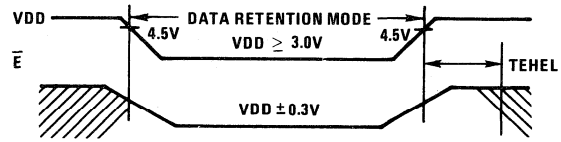
PACKAGE	CIRCUIT SUBSTRATE	SIZE
18 Pin DIP	Standard Two Sided PCB	12 to 15 square inch
18 Pin DIP	Fine Line or Multilayer PCB	9 to 11 square inch
18 Pin Leadless Carrier	Multilayer Alumina Substrate	3 to 5 square inch
HS-6564RH	Two Sided Mounting Mulitlayer Alumina Substrate	2 square inch

We urge you to contact your local Harris office or sales representative for pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Consider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data Retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention: within VDD +0.3V to VDD -0.3V.
2. All other inputs should be held either high (at CMOS VDD) or at ground to minimize IDDDR.
3. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VDD +0.3V and 70% of VDD during the power up and power down transitions.
4. The RAM can begin operation one TEHEL after VDD reaches the minimum operating voltage (4.5 volts).



Radiation Screening Procedure

1. Radiation screening is performed on discrete HS-6504RH devices. At least 20% of the yielding wafers contribute equally to a population of dice. From that population, a radiation test sample is selected. The sample has a size equivalent to 2 dice taken from 20% of the yielding wafers in a diffusion run.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad-Si (±10%) from a Gammacell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The samples will be tested to the data sheet limits within one hour after irradiation. The lot will be accepted only if all units, exclusive of nonradiation failures, meet the specified limits.
5. Radiation screening to a higher total dose is available. Customers should contact their Harris Representative for details.

Radiation Effects

The HS-6564RH is a radiation hardened memory module designed to survive in a radiation environment and to meet the electrical characteristcs of this data sheet. Latch-up free operation, achieved by the use of epitaxial starting material and improved total dose hardness, is obtained with special low temperature processing cycles.

On a production basis, Harris only performs screens for total dose hardness to a level of 1×10^5 Rad-Si. Transient radiation tests, however, have shown the following results:

- Latch-up free to doses $\geq 1 \times 10^{12}$ RAD/s.
- Upset (loss of stored data) $\geq 10^8$ RAD/s.

Burn-In/Irradiation Circuits

NOTE: Circuits are irradiated and burned-in as HS-6504RH discrete units. See HS-6504RH for appropriate irradiation bias circuits.

HARRIS

HS-65643RH

PRELIMINARY

July 1990

Radiation Hardened 64K x 1 SOS CMOS Static RAM

Features

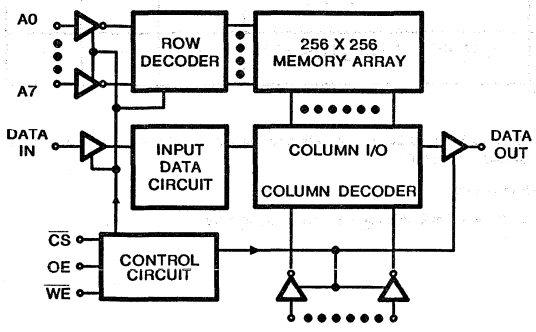
- 1.2 Micron Radiation Hardened SOS CMOS
  - Total Dose ..... 1×10^6 RAD (Si)
  - Transient Upset ..... 1×10^{11} RAD (Si)/s
  - Single Event Upset .... 1×10^{-12} Errors/bit-day
- Latch-up Free
- LET Threshold .....120 Mev/mg/cm^2
- Low Standby Supply Current ..... 2mA (Max)
- Low Operating Supply Current... 3mA/MHz (Max)
- Fast Access Time ..... 40ns (Max)
- High Output Drive Capability.....±8mA
- Gated Input Buffers
- Six Transistor Memory Cell
- Fully Static Design
- Aynchronous Operation
- CMOS Inputs
- 5V Single Power Supply
- Military Temperature Range ....-55°C to +125°C

Description

The Harris HS-65643RH is a fully asynchronous 64K x 1 radiation hardened static RAM. This RAM is fabricated using the Harris 1.2 micron silicon-on-sapphire CMOS technology. This technology gives exceptional hardness to all types of radiation, including neutron fluence, total ionizing dose, high intensity ionizing dose rates, and cosmic rays.

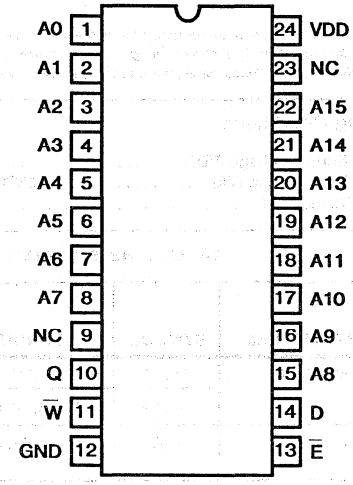
Low power operation is provided by a fully static design. Low standby power can be achieved without pull-up resistors, due to the gated input buffer design.

Functional Diagram

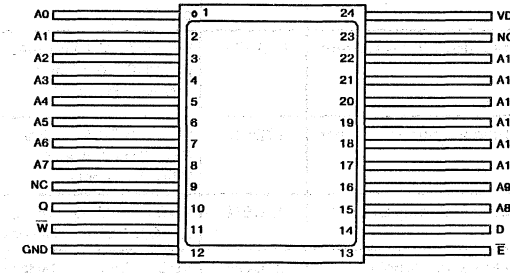


Pinouts

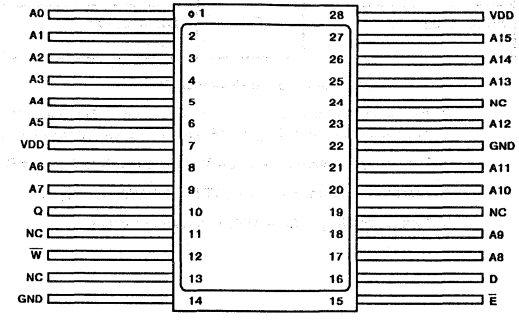
24 PIN CERAMIC DIP
TOP VIEW



24 PIN FLAT PACK
TOP VIEW



28 PIN FLAT PACK
TOP VIEW



11 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND -0.3V to VDD +0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering Ten Seconds)..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor..... 3mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance Junction-to-Case (θ_{jc})
Braze Seal DIP ..... TBD °C/W
Braze Seal Flat Pack ..... TBD °C/W
Thermal Impedance Junction-to-Ambient (θ_{ja})
Braze Seal DIP ..... TBD °C/W
Braze Seal Flat Pack ..... TBD °C/W
Maximum Package Power Dissipation at +125°C
Braze Seal DIP ..... TBD Watts
Braze Seal Flat Pack ..... TBD Watts
Gate Count ..... 101,000 Gates

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulitng in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance" are the only conditions recommended for satisfactory operation.

Operating Conditions

Operating Supply Voltage (VDD)..... 4.5V to 5.5V
Operating Temperature (TA) ..... -55°C to +125°C
Input Low Voltage (VIL)..... 0V to +0.8V
Input High Voltage (VIH) ..... VDD - 0.8V to VDD
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HS-65647 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

D.C. PARAMETERS	SYMBOL	CONDITIONS (1)	GROUP A SUBGROUPS	TEMPERATURE (°C)	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH 1	VDD = 4.5V, IO = -8.0ma	1, 2, 3	$-55 \le T_A \le +125$	2.4	-	V
	VOH 2	VDD = 4.5V, IO = -100µa			VDD -0.4		
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 8.0mA	1, 2, 3	$-55 \le T_A \le +125$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VDD = 5.5V, VI/O = GND or VDD, $\overline{E}$ = VDD - 0.8V	1, 2, 3	$-55 \le T_A \le +125$	-30	30	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	$-55 \le T_A \le +125$	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, $\overline{E}$ = VDD - 0.3V, and VIN = VDD or GND	1, 2, 3	$-55 \le T_A \le +125$	-	2	mA
						Pre-Rad = 500	µA
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, $\overline{E}$ = VDD - 0.8, and VIN = VDD or GND	1, 2, 3	$-55 \le T_A \le +125$	-	20	mA
Enable Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V, VIN = VDD or GND	1, 2, 3	$-55 \le T_A \le +125$	-	25	mA
Operating Supply Current	IDDOP	VDD = 5.5V, f = 1MHz (5) $\overline{E}$ = 0.8V, VIN = VDD or GND	1, 2, 3	$-55 \le T_A \le +125$	-	25	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, $\overline{E}$ = VDD - 0.3V	1, 2, 3	$-55 \le T_A \le +125$	-	TBD	µA
Functional Test	FT	VDD = 4.5V (4) and 5.5V	7, 8A, 8B	$-55 \le T_A \le +125$	-	-	-

NOTES: 1. All Voltages referenced to device GND.

2. A.C. measurements assume transition time $\le$ 5ns; input levels = 0.0V to VDD -0.8V, timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\ge$ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.

3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.

4. Tested as follows: f = 1MHz, VIH = 4.0V,VIL = 0.4V, IOH = -8.0mA, IOL = 8.0mA, VOH $\ge$ 1.5V and VOL $\le$ 1.5V.

5. Typical derating = 3mA/MHz increase in IDDOP.

TABLE 2. HS-65643RH A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Address Access Time	TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Chip Enable Access Time	TELQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Write Recovery Time	TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Address Hold Time	TEHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0		
Chip Enable to End-of-Write	TELWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
Address Valid to End-of-Write	TAVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TBD		
Chip Enable Pulse Width	TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TBD	-	
Address Setup Time	TAVWL TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Write to End-of-Write	TWLEH	VDD =4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20		
Write Enable Pulse Width	TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	ns
Data Setup Time	TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
	TDVEH				TBD		
Address Valid to End-of-Write	TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20		
Data Hold Time	TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
	TEHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TBD	-	ns

NOTES: 1. All voltages referenced to device GND.

2. A.C. measurements assume transition time $\leq$ 5ns; input levels = 0.0V to VDD - 0.8V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\geq$ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.

3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.

4. Tested as follows: f = 1MHz, VIH = 4.0V, VIL = 0.4V, IOH = -8.0mA, IOL = 8.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.

5. Typical derating = 3mA/MHz increase in IDDOP.

TABLE 3. HS-65643RH ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	10	pF
		VDD = Open, f = 1MHz All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	TBD	pF
I/O Capacitance	COUT	VDD = Open, f = 1MHz All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	12	pF
		VDD = Open, f = 1MHz All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	TBD	pF
Write Enable to Output in High Z	TWLQZ	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	10	ns
Write Enable High to Output ON	TWHQX	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Enable to Output ON	TELQX	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Enable to Output in High Z	TEHQZ	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	15	ns
Output Hold from Address Change	TAXQX	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	0	-	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

2. Applies to DIP device types only.

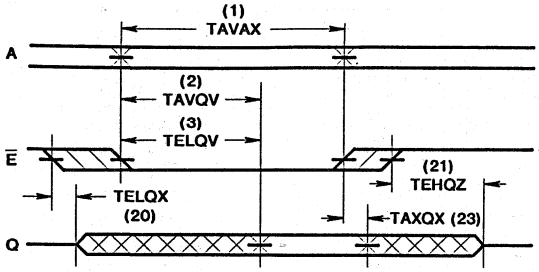
3. Applies to Flat Pack device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Groups C		Samples/5005	N/A	1, 7
Group D		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

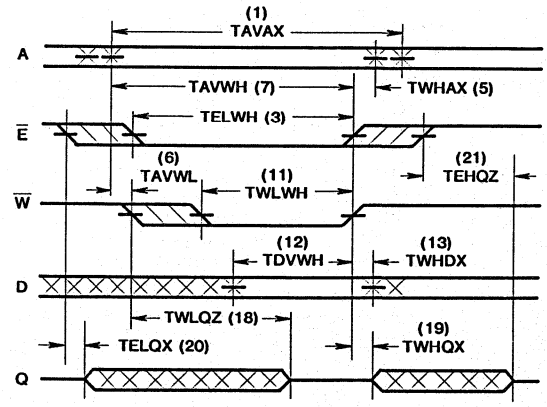
Timing Waveforms

READ CYCLE



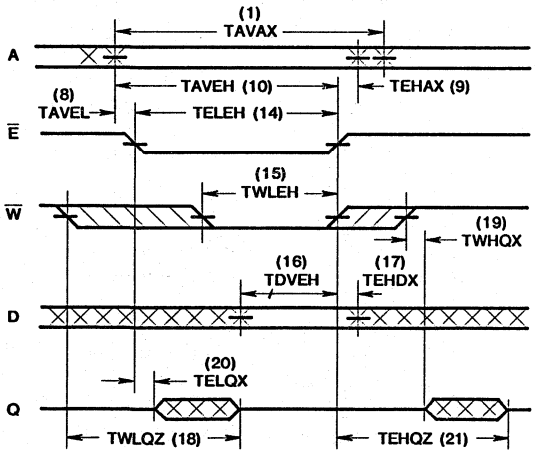
NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

WRITE CYCLE I: CONTROLLED BY $\overline{W}$ (LATE WRITE)



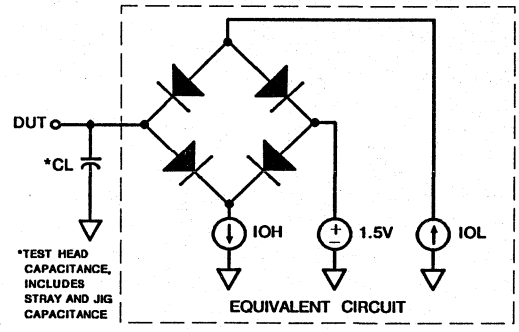
NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E}$ (EARLY WRITE)



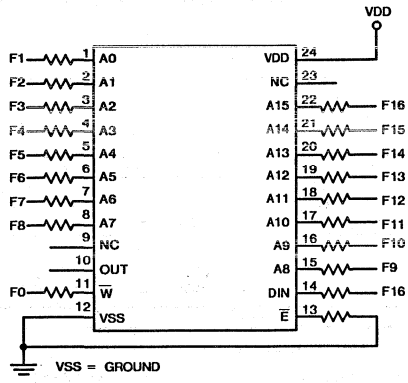
NOTE: In this mode, $\overline{W}$ rises after $\overline{E}$. If $\overline{W}$ falls before $\overline{E}$ by a time exceeding TWLQZ (Max) TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) - TWHQZ (Min), then Q will remain in the high impedance state throughout the cycle.

Test Circuit



Burn-In Circuits

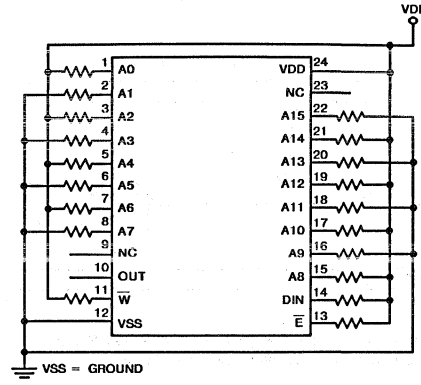
HS-65643RH (64K X 1 TSOS4 SRAM) 24 PIN FLAT PACK



DYNAMIC CONFIGURATION

NOTES:
Power Supply: VDD = 5.5V ±0.5V
Resistors = 10kΩ ±10%, > 0.25 Watt.
IDD < 20mA per Socket
Input Levels: VIH = VDD - 1.0V (±0.5V); VIL = 0.8V Max
F0 = 100kHz ± 10%, 50% Duty Cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2; ..... F16 = F15/2

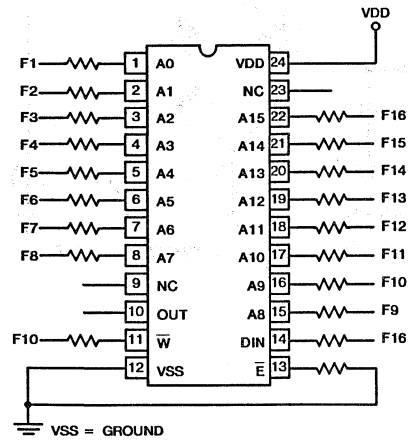
HS-65643RH (64K x 1 TSOS4 SRAM) 24 PIN FLAT PACK



STATIC CONFIGURATION

NOTES:
Power Supply: VDD = 5.5V ±0.5V
Resistors = 10kΩ ±10%, > 0.25 Watt
IDD < 5mA per Socket

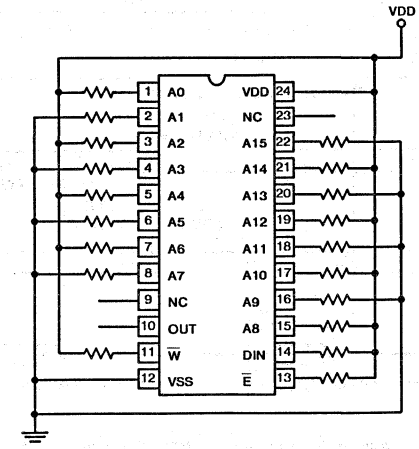
HS-65643RH (64K x 1 TSOS4 SRAM) 24 LEAD DIP



DYNAMIC CONFIGURATION

NOTES:
Power Supply: VDD = 5.5V ±0.5V
Resistors = 10kΩ ±10%, > 0.25 Watt
IDD < 20mA per Socket
Input Levels: VIH = VDD - 1.0V (±0.5V); VIL = 0.8V Max
F0 = 100kHz ± 10%, 50% Duty Cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2; ..... F16 = F15/2

HS-65643RH (64K x 1 TSOS4 SRAM) 24 LEAD DIP

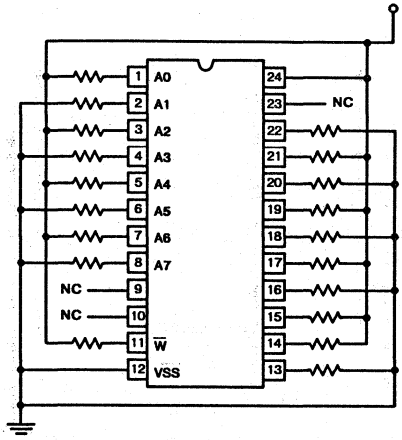


STATIC CONFIGURATION

NOTES:
Power Supply: VDD = 5.5V ±0.5V
All Resistors = 10kΩ ±10%, > 0.25 Watt
IDD < 5mA per Socket

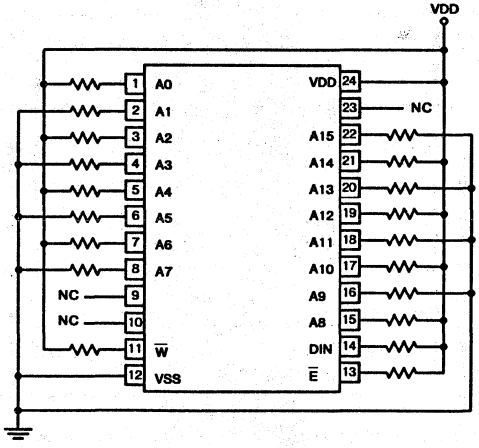
Irradiation Circuits

HS-65643RH (64K X 1 TSOS4 SRAM) 24 PIN LEAD DIP



NOTES:
Power Supply: VDD = 5.5V ±0.5V
Resistors = 10kΩ ±10%, > 0.25 Watt

HS-65643RH (64K X 1 TSOS4 SRAM) 24 PIN FLAT PACK



NOTES:
Power Supply: VDD = 5.5V ±0.5V
All Resistors = 10kΩ ±10%, > 0.25 Watt
IDD < 5mA per Socket

Metallization Topology

DIE DIMENSIONS:
297 x 310 mils x 21±1 mils

METALLIZATION:
Type: Al/Si/Cu
Thickness: 10kÅ ± 2kÅ

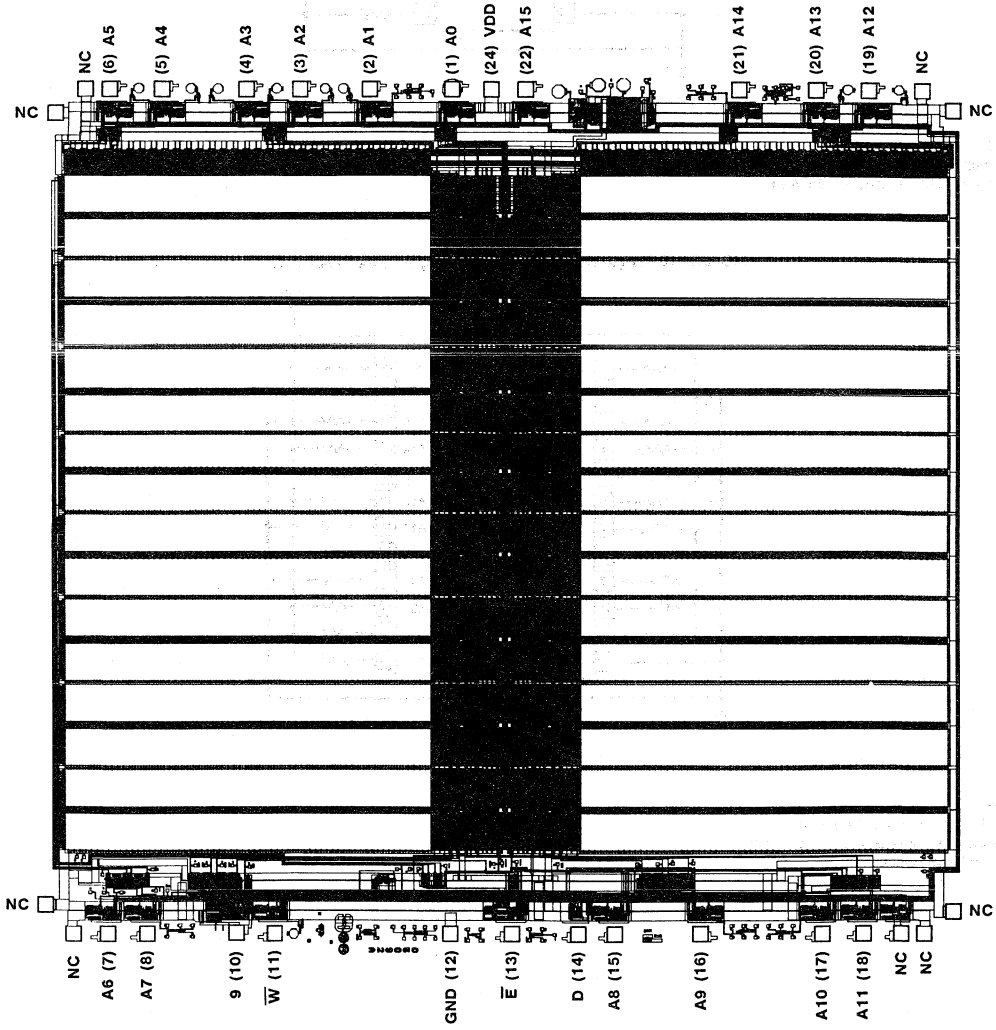
GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ to 9kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY: 1.5 x 10^5 Amps/cm^2

Metallization Mask Layout

HS-65643RH



HARRIS HS-65647RH

PRELIMINARY

July 1990

Radiation Hardened 8K x 8 SOS CMOS Static RAM

Features

- 1.2 Micron Radiation Hardened SOS CMOS
  - ▸ Total Dose ..... 1×10^6 RAD (Si)
  - ▸ Transient Upset ..... 1×10^{11} RAD (Si)/s
  - ▸ Single Event Upset .... 1×10^{-12} Errors/bit-day
- Latch-up Free
- LET Threshold .....120 Mev/mg/cm^2
- Low Standby Supply Current ..... 2mA (Max)
- Low Operating Supply Current... 3mA/MHz (Max)
- Fast Access Time ..... 40ns (Max)
- High Output Drive Capability.....±8mA
- Gated Input Buffers (Gated by E2)
- Six Transistor Memory Cell
- Fully Static Design
- Aynchronous Operation
- CMOS Inputs
- 5V Single Power Supply
- Standard JEDEC DIP Pinout
- Tri-State Outputs
- Military Temperature Range ....-55°C to +125°C

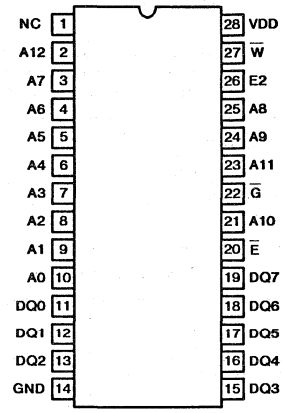
Description

The Harris HS-65647RH is a fully asynchronous 8K x 8 radiation hardened static RAM. This RAM is fabricated using the Harris 1.2 micron silicon-on-sapphire CMOS technology. This technology gives exceptional hardness to all types of radiation, including neutron fluence, total ionizing dose, high intensity ionizing dose rates, and cosmic rays.

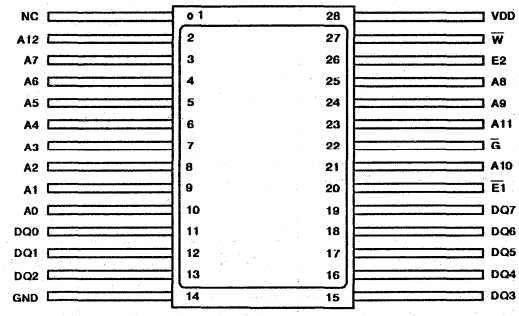
Low power operation is provided by a fully static design. Low standby power can be achieved without pull-up resistors, due to the gated input buffer design.

Pinouts

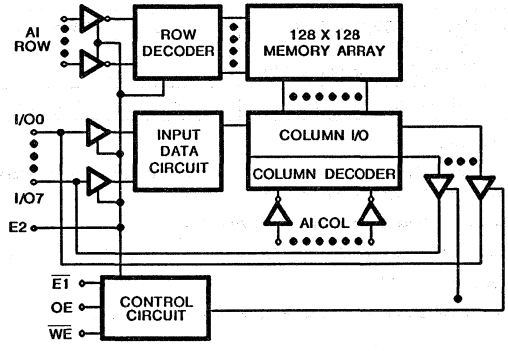
28 PIN CERAMIC DIP
TOP VIEW



28 PIN FLAT PACK
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND -0.3V to VDD +0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering Ten Seconds) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 3mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance Junction-to-Case (θ_{jc})
Ceramic DIP ..... TBD °C/W
Braze Seal Flat Pack ..... TBD °C/W
Thermal Impedance Junction-to-Ambient (θ_{ja})
Ceramic DIP ..... TBD °C/W
Braze Seal Flat Pack ..... TBD °C/W
Maximum Package Power Dissipation at +125°C
Ceramic DIP ..... TBD Watts
Braze Seal Flat Pack ..... TBD Watts
Gate Count ..... 101066 Gates

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulitng in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance" are the only conditions recommended for satisfactory operation.

Operating Conditions

Operating Supply Voltage (VDD) ..... 4.5V to 5.5V
Operating Temperature (TA) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... VDD - 0.8V to VDD
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HS-65647 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

D.C. PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH 1	VDD = 4.5V, IO = -8.0ma	1, 2, 3	$-55 \le T_A \le +125$	2.4	-	V
	VOH 2	VDD = 4.5V, IO = -100µa			VDD -0.4		
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 8.0mA	1, 2, 3	$-55 \le T_A \le +125$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VDD = 5.5V, VI/O = GND or VDD, G = VDD - 0.8V	1, 2, 3	$-55 \le T_A \le +125$	-30	30	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	$-55 \le T_A \le +125$	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, $\overline{E1}$ = VDD - 0.3V, and E2 = GND + 0.3V (Note 6)	1, 2, 3	$-55 \le T_A \le +125$	-	2	mA
						Pre-Rad = 500	µA
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, $\overline{E1}$ = VDD - 0.8V, and E2 = 0.8V (Note 6)	1, 2, 3	$-55 \le T_A \le +125$	-	10	mA
Enable Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, $\overline{E1}$ = 0.8V, E2 = VDD - 0.8V	1, 2, 3	$-55 \le T_A \le +125$	-	25	mA
Operating Supply Current	IDDOP	VDD = 5.5V, $\overline{G}$ = 5.5V, f = 1MHz, $\overline{E1}$ = 0.8V, E2 = VDD - 0.8V, (Note 5)	1, 2, 3	$-55 \le T_A \le +125$	-	25	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, $\overline{E1}$ = VCC - 0.3V and E2 = GND + 0.3V (Note 6)	1, 2, 3	$-55 \le T_A \le +125$	-	TBD	µA
Functional Test	FT	VDD = 4.5V (Note 4)	7, 8A, 8B	$-55 \le T_A \le +125$	-	-	-

NOTES:
1. All Voltages referenced to device GND.
2. A.C. measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD -0.8V, timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≥ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.
4. Tested as follows: f = 1MHz, VIH = 4.0V,VIL = 0.4V, IOH = -8.0mA, IOL = 8.0mA, VOH ≥ 1.5V and VOL ≤ 1.5V.
5. Typical derating = 3mA/MHz increase in IDDOP.
6. In order for the device to assume a low power drain standby mode, E2 must be disabled.

TABLE 2. HS-65647RH A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Address Access Time	TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Output Enable Access Time	TGLQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	15	ns
Chip Enable Access Time	TE1LQV TE2HQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Write Recovery Time	TWHAX TE1HAX TE2LAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Enable to End-of-Write	TE1LE1H TE2HE2L	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
Address Setup Time	TAVWL TAVE1L TAVE2H	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Write Enable Pulse Width	TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	ns
Data Setup Time	TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
	TDVE1H TDVE2L				TBD		
Data Hold Time	TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
	TE1HDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TBD	-	ns
	TE2LDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	TBD	-	ns

NOTES: 1. All voltages referenced to device GND.

2. A.C. measurements assume transition time $\leq$ 5ns; input levels = 0.0V to VDD - 0.8V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\geq$ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.

3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.

4. Tested as follows: f = 1MHz, VIH = 4.0V, VIL = 0.4V, IOH = -8.0mA, IOL = 8.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.

5. Typical derating = 3mA/MHz increase in IDDOP.

6. In order for the device to assume a low power drain standby mode, E2 must be disabled.

TABLE 3. HS-65647RH ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	10	pF
		VDD = Open, f = 1MHz All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	TBD	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	12	pF
		VDD = Open, f = 1MHz All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	TBD	pF
Write Enable to Output in High Z	TWLQZ	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	10	ns
Write Enable High to Output ON	TWHQX	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Enable to Output ON	TE1LQX TE2HQX	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Output Enable to Output ON	TGLQX	VDD = 4.5 and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
Chip Enable to Output in High Z	TE1HQZ	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	15	ns
	TE2LQZ		1	$-55^oC \leq T_A \leq +125^oC$	-	15	ns
Output Disable to Output in High Z	TGHQZ	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	-	15	ns
Output Hold from Address Change	TAXQX	VDD = 4.5V and 5.5V	1	$-55^oC \leq T_A \leq +125^oC$	0	-	ns

NOTES: 1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

2. Applies to DIP device types only.

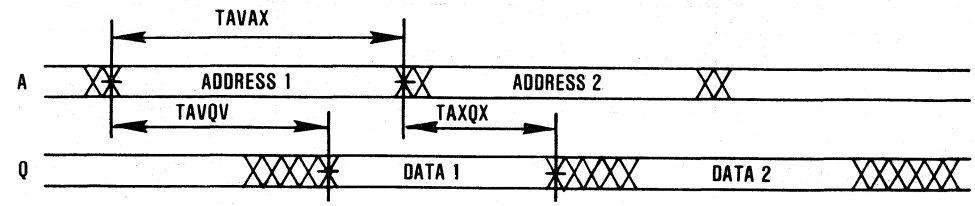
3. Applies to Flat Pack device types only.

TABLE 4. APPLICABLE SUBGROUPS

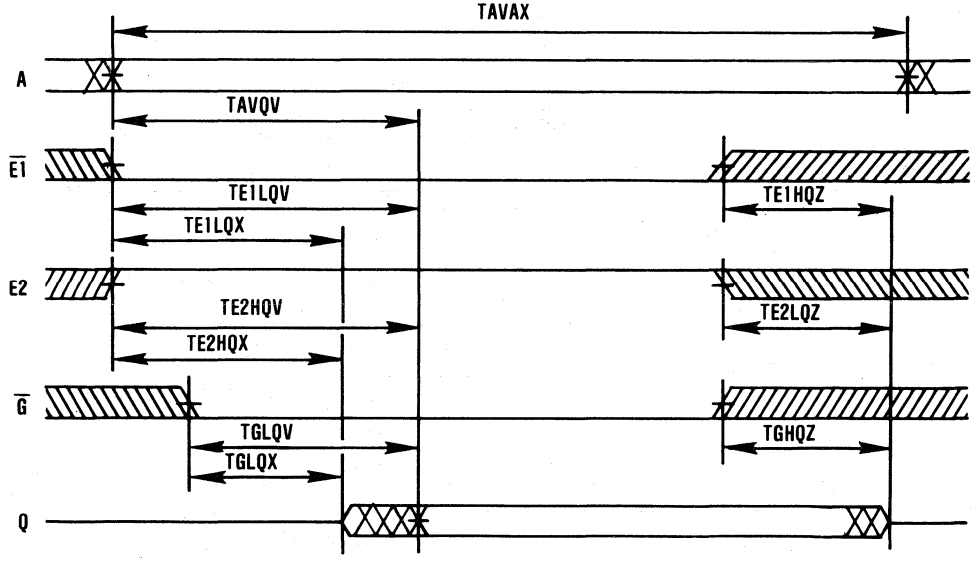
CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Groups C		Samples/5005	N/A	1, 7
Group D		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

Read Cycles

READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW

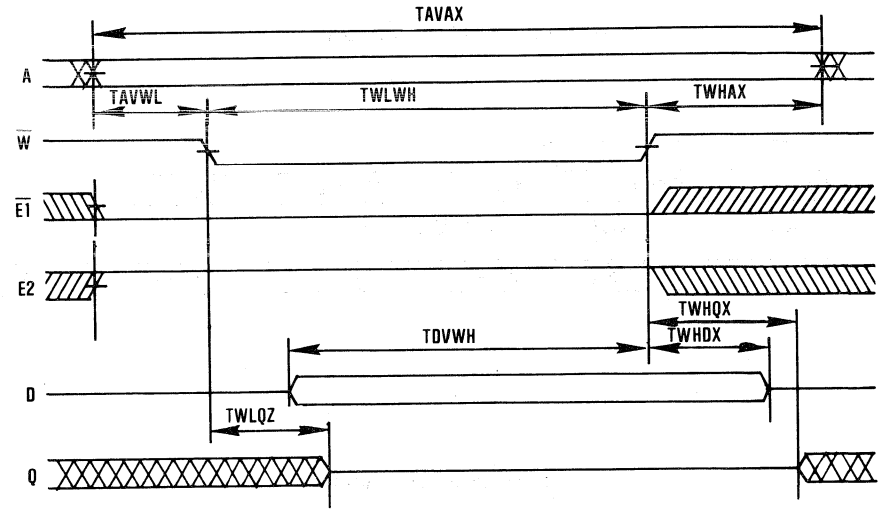


READ CYCLE II: $\overline{W}$ HIGH

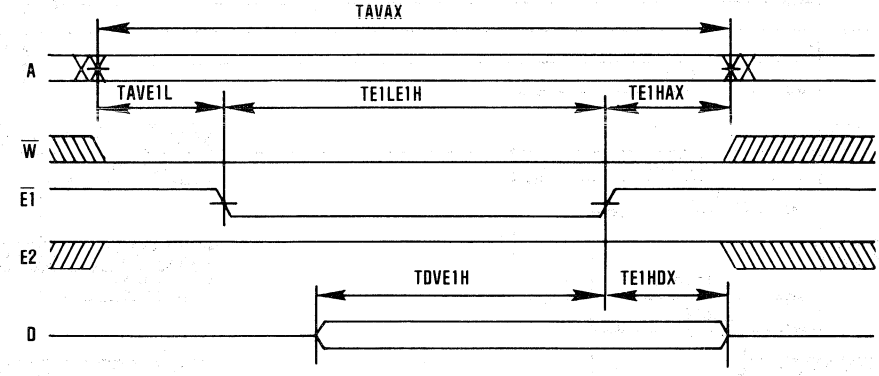


Write Cycles

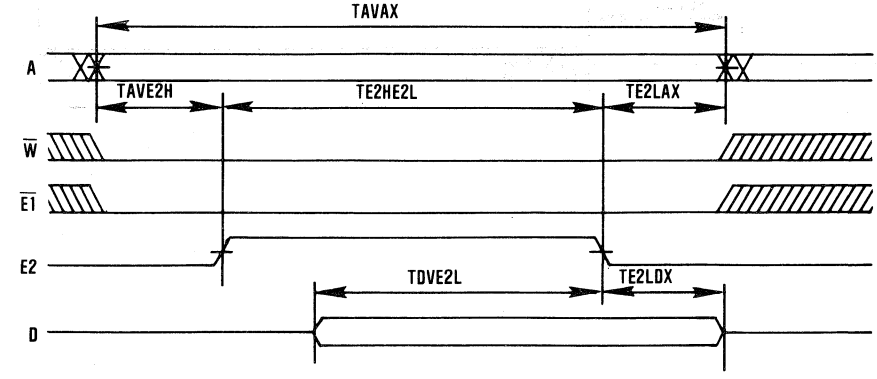
WRITE CYCLE I: LATE WRITE



WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E1}$

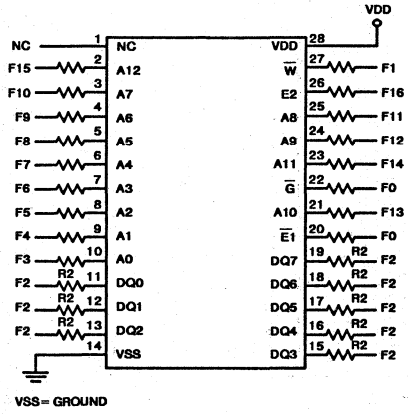


WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2



Burn-In Circuits

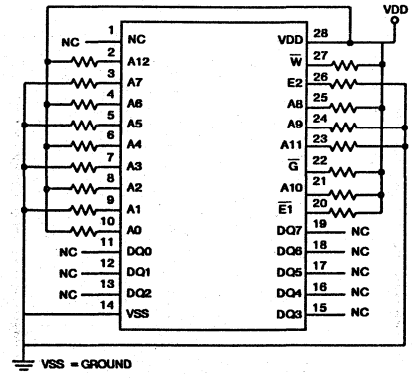
HS-65647RH (8K X 8 TSOS4 SRAM) 28 PIN FLAT PACK



DYNAMIC CONFIGURATION

NOTES:
Power Supply: VDD = 5.5V ±0.5V
Resistors = 10kΩ ±10%, > 0.25 Watt except R2 = 47kΩ ±10%, > 0.25 Watt
IDD < 20mA per Socket
Input Levels: VIH = VDD - 1.0V (±0.5V); VIL = 0.8V Max
F0 = 100kHz ± 10%, 50% Duty Cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2;..... F16 = F15/2

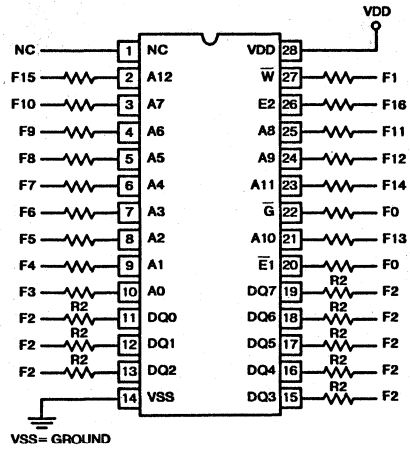
HS-65647RH (8K x 8 TSOS4 SRAM) 28 PIN FLAT PACK



STATIC CONFIGURATION

NOTES:
Power Supply: VDD = 5.5V ±0.5V
All Resistors = 10kΩ ±10%, > 0.25 Watt
IDD < 5mA per Socket

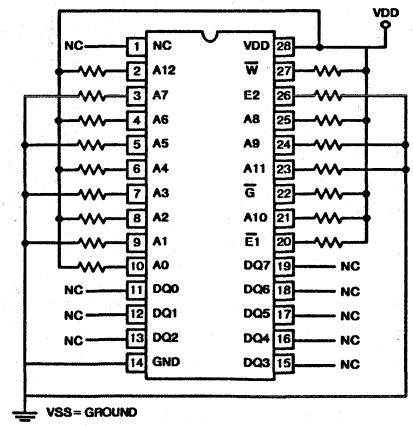
HS-65647RH (8K x 8 TSOS4 SRAM) 28 LEAD DIP



DYNAMIC CONFIGURATION

NOTES:
Power Supply: VDD = 5.5V ±0.5V
Resistors = 10kΩ ±10%, > 0.25 Watt except R2 = 47kΩ ±10%, > 0.25 Watt
IDD < 20mA per Socket
Input Levels: VIH = VDD - 1.0V (±0.5V); VIL = 0.8V Max
F0 = 100kHz ± 10%, 50% Duty Cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2;..... F16 = F15/2

HS-65647RH (8K x 8 TSOS4 SRAM) 28 LEAD DIP

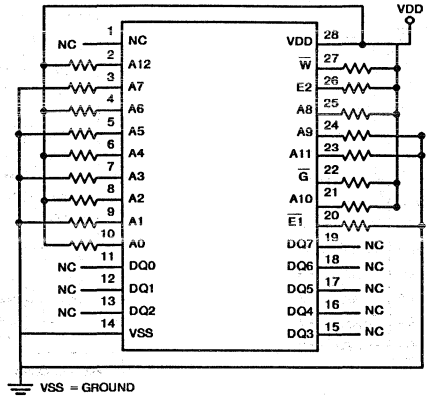


STATIC CONFIGURATION

NOTES:
Power Supply: VDD = 5.5V ±0.5V
All Resistors = 10kΩ ±10%, > 0.25 Watt
IDD < 5mA per Socket

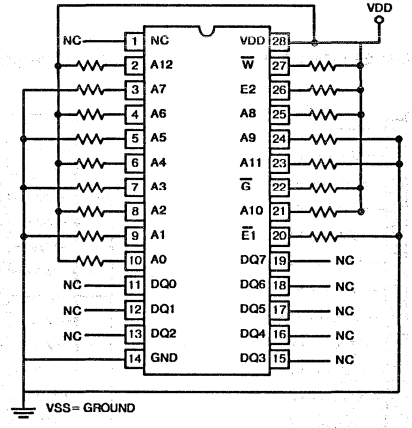
Irradiation Circuits

HS-65647RH (8K X 8 TSOS4 SRAM) 28 PIN FLAT PACK



NOTES:
Power Supply: VDD = 5.5V ±0.5V
All Resistors = 10kΩ ±10%, > 0.25 Watt

HS-65647RH (8K X 8 TSOS4 SRAM) 28 PIN LEAD DIP



NOTES:
Power Supply: VDD = 5.5V ±0.5V
All Resistors = 10kΩ ±10%, > 0.25 Watt

Metallization Topology

DIE DIMENSIONS:
228 x 313 mils x 21±1 mils

METALLIZATION:
Type: Al/Si/Cu
Thickness: 10kÅ ± 2kÅ

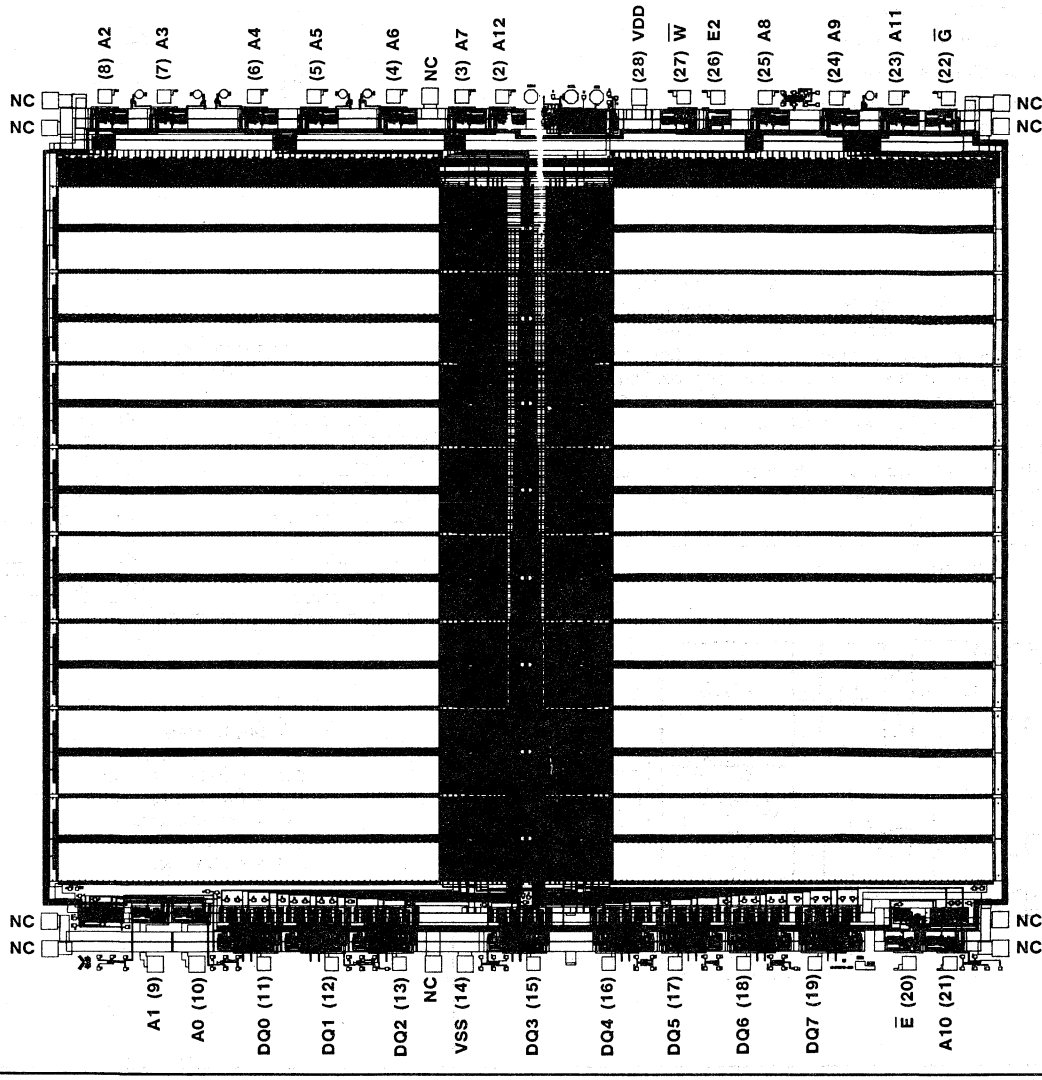
GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ to 9kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY: 1.5×10^5 Amps/cm^2

Metallization Mask Layout

HS-65647RH



HARRIS HS-65C162RRH

April 1990

Radiation Hardened 2048 x 8-Bit Asynchronous CMOS Static RAM

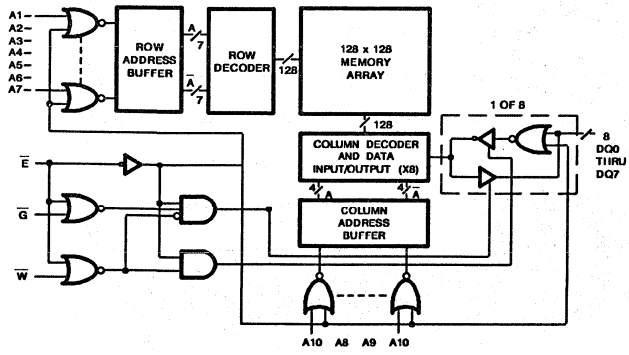
Features

- Radiation Hardened EPI-CMOS
- Total Dose ..... 2×10^5 RAD(Si)
- Transient Upset ..... $> 1 \times 10^9$ RAD(Si)/s
- Latch-Up Free ..... $> 1 \times 10^{12}$ RAD(Si)/s
- Single Event Upset Hardened Option
- Low Standby Current .....200µA Max
- Fast Access Time.....160ns Max
- 2048 x 8-Bit
- Single +5V Power Supply
- Asynchronous Operation
- CMOS Compatible Inputs
- Completely Static Operation
- Three-State Output
- Military Temperature Range.....-55°C to +125°C Operation
- Functionally Equivalent to Harris HM-65162

Description

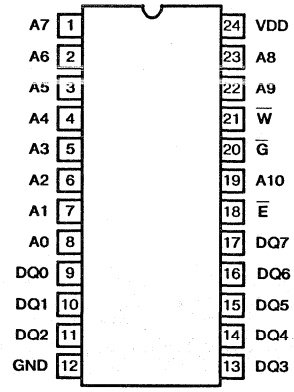
The HS-65C162RRH is designed to be functionally compatible with the Harris HM-65162. This device is a asynchronous 2048 x 8-bit static CMOS RAM fabricated using the Harris radiation hardened, self-aligned junction isolated silicon gate technology. This technology completely eliminates the need for guardbands. The HS-65C162RRH is designed to have a maximum access time of 160ns after exposure to 2×10^5 Rads(Si) over the full military temperature range. Latch-up free operation is achieved by the use of epitaxial starting material. In addition, the device is single event upset hardened. Operation is designed for +5V. Contact your nearest Harris representative for sample availability.

Functional Diagram

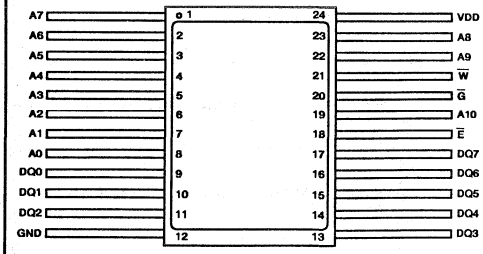


Pinouts

24 PIN SIDEBRAZED DIP
TOP VIEW



24 PIN FLATPACK
TOP VIEW



PIN NAMES

A = Address Input
DQ = Data Input/Output
E = Chip Enable
G = Output Enable
W = Write Enable
NC = No Connect

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied .... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 2

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Brazed Seal DIP Package	56°C/W	12°C/W
Brazed Seal Flatpack Package	66°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.89W
Braze Seal Flatpack Package 0.76W
Gate Count ..... 26000 Gates

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance" are the only conditions recommended for satisfactory operation.

Operating Conditions

Operating Supply Voltage (VDD) ..... 4.5V to 5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
SEU Immunity Operating Temperature Range ... -20°C to +80°C
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... VDD-1.5 to VDD+0.3
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Times ..... 40ns Max

TABLE 1. HS-65C162RRH D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
	VOH2	VDD = 4.5V, IO = -100µA	1, 2, 3	$-55°C \le T_A \le +125°C$	VDD-0.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 5.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VDD = 5.5V, $\overline{G}$ = 5.5V, or $\overline{E}$ = 5.5V VI/O = GND or VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, $\overline{E}$ = 5.5V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	200	µA
Operating Supply Current	IDDOP	VDD = 5.5V, $\overline{G}$ = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	100	mA
Enable Supply Current	ENIDD	VDD = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V VDD = VIH, VIL = 0V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	100	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, $\overline{E}$ = VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-	100	µA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	$-55°C \le T_A \le +125°C$	-	-	-

TABLE 2. HS-65C162RRH A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	200	-	ns
Address Access Time	TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	160	ns
Output Enable Access Time	TGLQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$		120	ns
Chip Enable Access Time	TELQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	160	ns
Write Enable Read Setup Time	TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	20	-	ns
Address Setup Time	TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	20	-	ns
Chip Selection to End of Write	TELWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	180	-	ns
Write Enable Pulse Setup Time	TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns
Chip Enable Data Setup Time	TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns
Address Valid to End of Write	TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	180	-	ns
Write Enable Pulse Width	TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	160	-	ns
Data Setup Time	TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	160	-	ns
Data Hold Time	TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	30	-	ns

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HS-65C162RRH ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

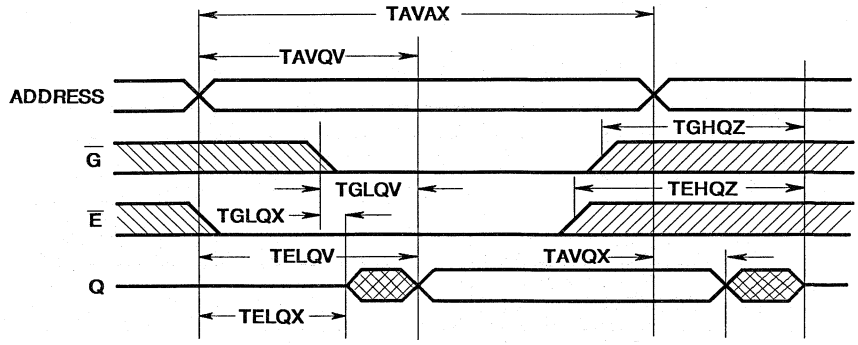
PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6, 8	+25°C	-	15	pF
		VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6, 9	+25°C	-	12	pF
I/O Capacitance	CI/O	VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6, 8	+25°C	-	12	pF
		VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6, 9	+25°C	-	10	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	60	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Chip Enable to Output ON	TELQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Chip Enable High to Output ON	TEHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	60	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	40	ns
Output Hold from Address Change	TAVQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to VDD-1.5; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 5mA/MHz increase in ICCOP.
5. Tested as follows: f = 3MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. This is a "typical" value and not a "maximum" value.
8. Applies to DIP device types only.
9. Applies to Flatpack device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, D	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7, 9	N/A
Group C		Samples/5005	N/A	1, 7, 9
Group D		Samples/5005	1, 7, 9	1, 7, 9

Read Cycle

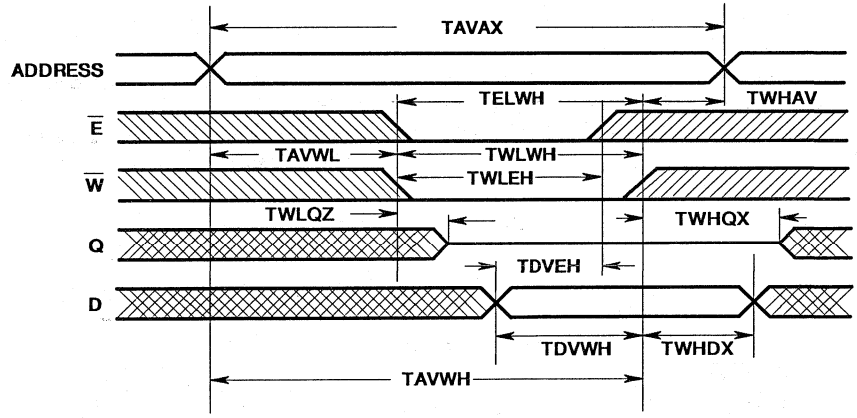


NOTE: $\overline{W}$ is high for a Read Cycle

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be $\leq$ VIL and W $\geq$ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

Write Cycles

WRITE CYCLE I

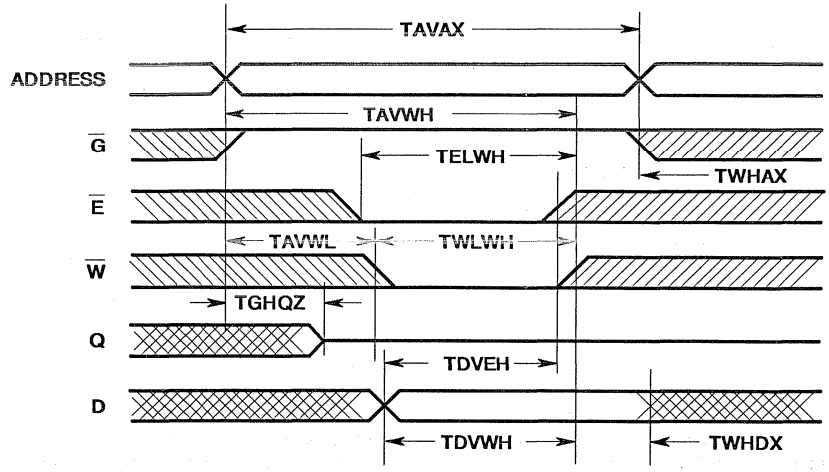


NOTE: $\overline{G}$ is low throughout Write Cycle

To write, addresses must be stable, $\overline{E}$ low and W falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of $\overline{W}$. (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied. (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low or after the W transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

Write Cycles (Continued)

WRITE CYCLE II



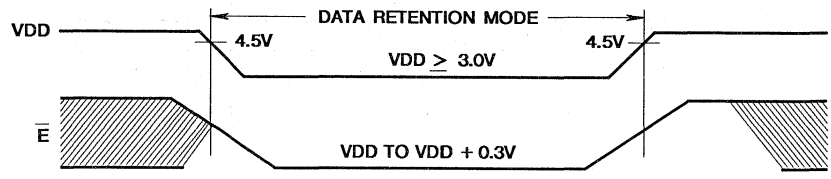
In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

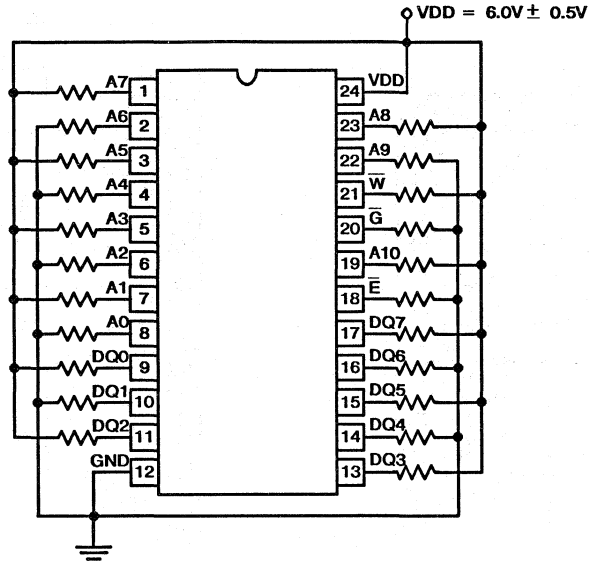
1. Chip Enable ($\overline{E}$) must be held high during data retention; within VDD to VDD +0.3V
2. $\overline{E}$ must be kept between VDD +0.3V and 70% of VDD during the power up and power down transitions.

DATA RETENTION TIMING



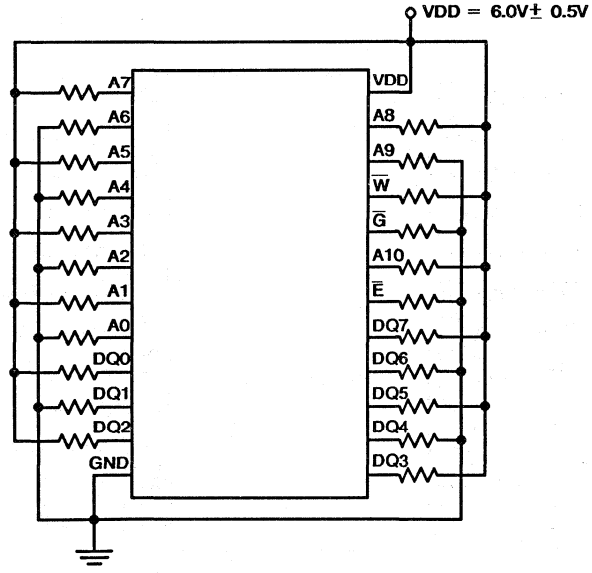
Burn-In Circuits

HS-65C162RRH (CERAMIC DIP)



STATIC CONFIGURATION

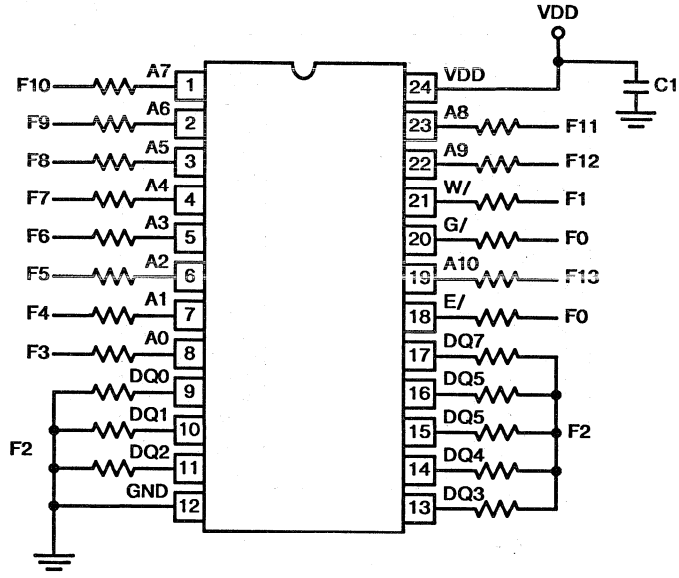
HS-65C162RRH (FLATPACK)



STATIC CONFIGURATION

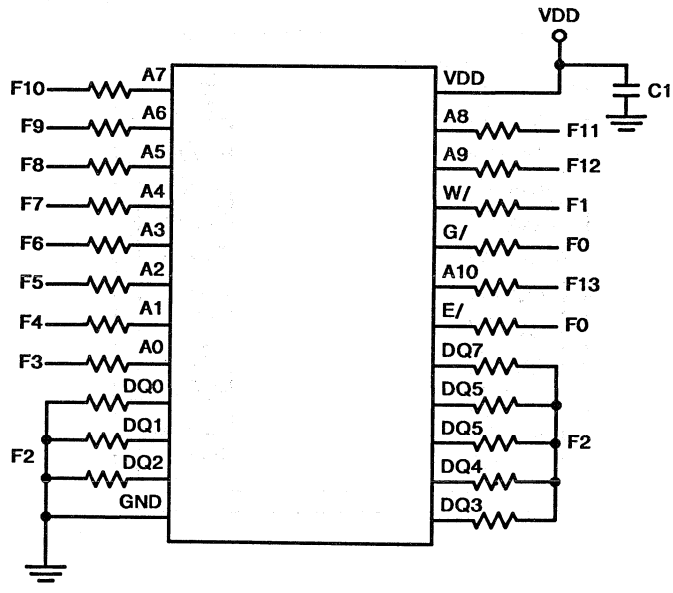
Burn-In Circuits

HS-65C162RRH (CERAMIC DIP)



DYNAMIC CONFIGURATION

HS-65C162RRH (FLATPACK)

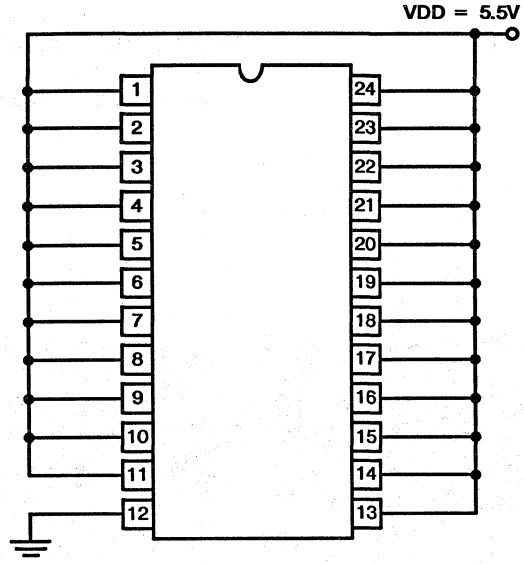


VDD = 6.0V ± 0.5V
VIH = 4.0V to VCC
VIL = 0.8V (max)
C1 = 0.01µF (min)
All resistors = 47kΩ ± 5%
F0 = 100KHz ± 10%, 50% duty cycle
F1 = F0/2, F2/F1/2, • • • F13 = F12/2

DYNAMIC CONFIGURATION

Irradiation Circuit

HS-65C162RRH (CERAMIC DIP)



NOTES:

1. Pin 12 to Ground
2. All other pins tied to VDD

Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 2 x 10^5 Rad(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = +5V. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The sample devices shall be tested within one hour after irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.

Metal Topology

DIE DIMENSIONS:
198 x 270 x 19 ±1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11.5kÅ - 14.5kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ - 9kÅ

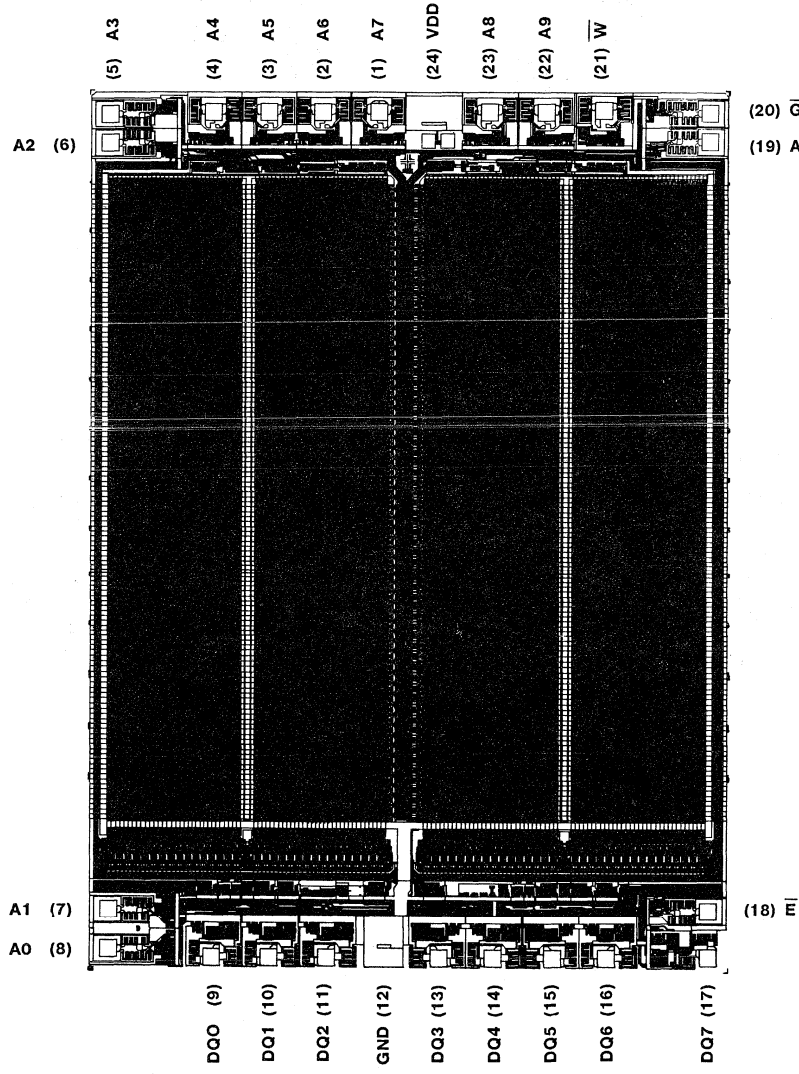
DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Braze Seal DIP — 460°C (Max)
Braze Seal Flatpack — 460°C (Max)

WORST CASE CURRENT DENSITY:
1.4×10^5 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-65C162RRH-8/-Q



HARRIS HS-65C262RH/RRH HS-65T262RRH

Radiation Hardened 16K x 1 CMOS RAM

July 1990

Features

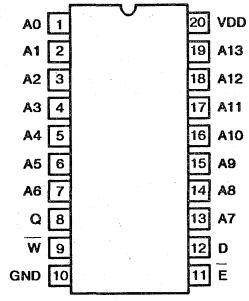
- Radiation Hardened EPI-CMOS
  - Total Dose ..... 2×10^5 RAD(Si)
  - Transient Upset ..... $> 5 \times 10^8$ RAD(Si)/sec
  - Latch-up Free..... $> 1 \times 10^{12}$ RAD(Si)/sec
- Single Event Upset Resistant Option
- Low Standby Current ..... 200µA (Max)
- Low Operating Current ..... 6mA/MHz (Max)
- Fast Access Time..... 150ns (Typ)
- 16,384 x 1-Bit
- Single +5V Power Supply
- Asynchronous Operation
- CMOS or TTL Compatible Inputs
- Completely Static Operation
- Three-State Output
- Military Temperature Range..... -55°C to +125°C

Description

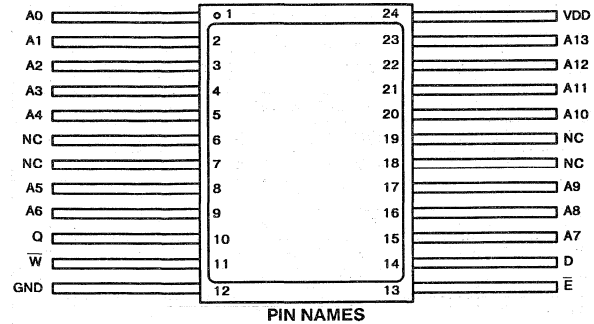
The HS-65C262RH and HS-65T262RRH are both designed to be functionally compatible with the Harris HM-65262. Two versions of the radiation hardened CMOS RAM are offered to provide both CMOS input levels (HS-65C262RH) and TTL compatible input levels (HS-65T262RRH). Both RAMs are asynchronous 16,384 x 1 bit static CMOS RAMs fabricated using the Harris radiation hardened, self-aligned junction isolated silicon gate technology. This technology completely eliminates the need for guardbands. The devices are designed to have a maximum access time of 150ns for CMOS input levels and 175ns for TTL input levels after exposure to 2×10^5 Rads(Si) over the full military temperature range. Latch-up free operation is achieved by the use of epitaxial starting material. In addition, the devices have the option to be single event upset resistant. Operation is designed for +5V. Contact your nearest Harris representative for sample availability.

Pinouts

20 PIN CERAMIC DIP
TOP VIEW



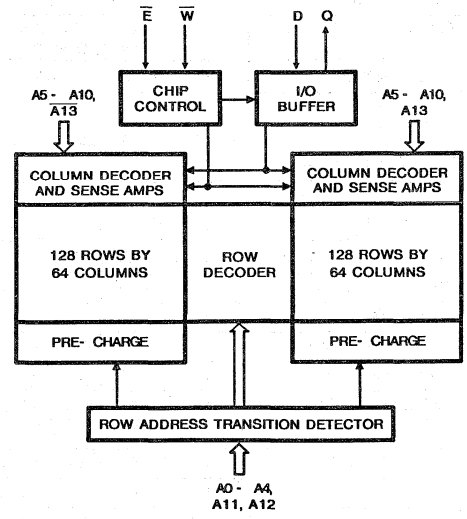
24 PIN FLATPACK
TOP VIEW



PIN NAMES

A	= Address Input	$\overline{E}$	= Chip Enable
D	= Data Input	$\overline{W}$	= Write Enable
Q	= Data Output	NC	= No Connect

Functional Diagram



11 MEMORIES

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 6mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	78°C/W	13°C/W
Braze Seal FP Package	91°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.64W
Braze Seal FP Package 0.55W
Gate Count ..... 26256 Gates

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance" are the only conditions recommended for satisfactory operation.

Operating Conditions

Operating Supply Voltage (VDD) ..... 4.5V to 5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... VDD -1.5 to VDD
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HS-65C262RH D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

D.C. PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	-55°C≤T_A≤+125°C	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 5.0mA	1, 2, 3	-55°C≤T_A≤+125°C	-	0.4	V
High Impedance Output Leakage Current	IOZ	VDD = 5.5V, E = 5.5V, VO = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, E = VDD -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	200	µA
Operating Supply Current	IDDOP	VDD = 5.5V, (Note 4), f = 1MHz, E = 0.8V, VI = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-	6	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, E = VDD -0.3V, VI = VDD or GND	1, 2, 3	-55°C≤T_A≤+125°C	-	100	µA
Enable Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, E = 0.8V VI = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-	200	µA
Functional Test	FT	VDD = 4.5V (Note 5)	7, 8A, 8B	-55°C≤T_A≤+125°C	-	-	-

TABLE 2. HS-65C262RH A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

A.C. PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1, 2, 3) SUBGROUPS	GROUP A TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	(1) TAVAX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	150	-	ns
Address Access Time	(2) TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	145	ns
Chip Enable to End of Write	(3) TELWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	95	-	ns
Chip Enable Access Time	(4) TELQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	150	ns
Address Hold Time	(5) TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Setup Time	(6) TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	10	-	ns
Address Valid to End of Write	(7) TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	95	-	ns
Address Setup Time	(8) TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Hold Time	(9) TEHAX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Valid to End of Write	(10) TAVEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	95	-	ns
Write Enable Pulse Write	(11) TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	85	-	ns
Data Setup Time	(12) TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	85	-	ns
Data Hold Time	(13) TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Enable Pulse Width	(14) TELEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	150	-	ns
Write to End of Write	(15) TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	85	-	ns
Data Setup Time	(16) TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	85	-	ns
Data Hold Time	(17) TEHDX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns

TABLE 3. HS-65C262RRH ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 7	$T_A = +25^oC$	-	8	pF
		VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 8	$T_A = +25^oC$	-	10	pF
Output Capacitance	CO	VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 7	$T_A = +25^oC$	-	10	pF
		VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 8	$T_A = +25^oC$	-	12	pF
Write Enable to Output in High Z	(18) TWLQZ	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	30	ns
Write Enable High to Output ON	(19) TWHQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable to Output ON	(20) TELQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Output Enable High to Output in High Z	(21) TEHQZ	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	25	ns
Chip Disable to Output Hold Time	(22) TEHQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Address Invalid Output Hold Time	(23) TAXQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
High Level Output Voltage	VOH2	VDD = 4.5V, IO = -100µA	6	$-55^oC \leq T_A \leq +125^oC$	VDD -0.4V	-	V

NOTES:
1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to VDD-1.5V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 6mA/MHz increase in IDDOP.
5. Tested as follows: f = 3MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. Applies to DIP device types only.
8. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Group C		Samples/5005	N/A	1, 7
Group D		Samples/5005	1, 7	1, 7
Group E	Subgroup 2	Samples/5005	1, 7	1, 7

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 6mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	78°C/W	13°C/W
Braze Seal FP Package	91°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.64W
Braze Seal FP Package 0.55W
Gate Count ..... 26256 Gates

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance" are the only conditions recommended for satisfactory operation.

Operating Conditions

Operating Supply Voltage (VDD) ..... 4.5V to 5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.8V
SEU Immunity Operating Temperature Range ... -20°C to +80°C
Input High Voltage (VIH) ..... VDD -1.5 to VDD
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HS-65C262RRH D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

D.C. PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	-55°C≤T_A≤+125°C	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 5.0mA	1, 2, 3	-55°C≤T_A≤+125°C	-	0.4	V
High Impedance Output Leakage Current	IOZ	VDD = 5.5V, $\overline{E}$ = 5.5V, VO = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, $\overline{E}$ = VDD -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	200	µA
Operating Supply Current	IDDOP	VDD = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V, VI = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-	6	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, $\overline{E}$ = VDD -0.3V, VI = VDD or GND	1, 2, 3	-55°C≤T_A≤+125°C	-	100	µA
Enable Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, E = 0.8V VI = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-	200	µA
Functional Test	FT	VDD = 4.5V (Note 5)	7, 8A, 8B	-55°C≤T_A≤+125°C	-	-	-

TABLE 2. HS-65C262RRH A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	(1) TAVAX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	150	-	ns
Address Access Time	(2) TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	145	ns
Chip Enable to End of Write	(3) TELWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	150	-	ns
Chip Enable Access Time	(4) TELQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	150	ns
Address Hold Time	(5) TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Setup Time	(6) TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	10	-	ns
Address Valid to End of Write	(7) TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	150	-	ns
Address Setup Time	(8) TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Hold Time	(9) TEHAX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Valid to End of Write	(10) TAVEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	150	-	ns
Write Enable Pulse Write	(11) TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	140	-	ns
Data Setup Time	(12) TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	140	-	ns
Data Hold Time	(13) TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ms
Enable Pulse Width	(14) TELEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	150	-	ns
Write to End of Write	(15) TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	140	-	ns
Data Setup Time	(16) TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	140	-	ns
Data Hold Time	(17) TEHDX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns

TABLE 3. HS-65C262RRH ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 7	$T_A = +25^oC$	-	8	pF
		VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 8	$T_A = +25^oC$	-	TBD	pF
Output Capacitance	CO	VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 7	$T_A = +25^oC$	-	10	pF
		VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 8	$T_A = +25^oC$	-	TBD	pF
Write Enable to Output in High Z	(18) TWLQZ	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	30	ns
Write Enable High to Output ON	(19) TWHQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable to Output ON	(20) TELQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Output Enable High to Output in High Z	(21) TEHQZ	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	25	ns
Chip Disable to Output Hold Time	(22) TEHQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Address Invalid Output Hold Time	(23) TAXQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
High Level Output Voltage	VOH2	VDD = 4.5V, IO = -100µA	6	$-55^oC \leq T_A \leq +125^oC$	VDD -0.4V	-	V

NOTES:
1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to VDD-1.5V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 6mA/MHz increase in IDDOP.
5. Tested as follows: f = 3MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. Applies to DIP device types only.
8. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Group C		Samples/5005	N/A	1, 7
Group D		Samples/5005	1, 7	1, 7
Group E	Subgroup 2	Samples/5005	1, 7	1, 7

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 6mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	78°C/W	13°C/W
Braze Seal FP Package	91°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.64W
Braze Seal FP Package 0.55W
Gate Count ..... 26256 Gates

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance" are the only conditions recommended for satisfactory operation.

Operating Conditions

Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.8V
SEU Immunity Operating Temperature Range ... -20°C to +80°C
Input High Voltage (VIH) ..... +2.3V to VCC
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. HS-65T262RRH D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

D.C. PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	-55°C≤T_A≤+125°C	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 8.0mA	1, 2, 3	-55°C≤T_A≤+125°C	-	0.4	V
High Impedance Output Leakage Current	IOZ	VDD = 5.5V, $\overline{E}$ = 5.5V, VO = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA $\overline{E}$ = VDD -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	200	µA
Standby Supply Current	IDDSB2	VDD = 5.5V, IO = 0mA, $\overline{E}$ = 2.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	5	mA
Operating Supply Current	IDDOP	VDD = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V, VI = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-	6	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, $\overline{E}$ = VDD -0.3V, VI = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-	100	µA
Enable Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V VI = GND or VDD	1, 2, 3	-55°C≤T_A≤+125°C	-	50	mA
Functional Test	FT	VDD = 4.5V (Note 5)	7, 8A, 8B	-55°C≤T_A≤+125°C	-	-	-

TABLE 2. HS-65T262RRH A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	(1) TAVAX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	175	-	ns
Address Access Time	(2) TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	165	ns
Chip Enable to End of Write	(3) TELWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	175	-	ns
Chip Enable Access Time	(4) TELQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	175	ns
Address Hold Time	(5) TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Setup Time	(6) TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	10	-	ns
Address Valid to End of Write	(7) TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	175	-	ns
Address Setup Time	(8) TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Hold Time	(9) TEHAX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns
Address Valid to End of Write	(10) TAVEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	175	-	ns
Write Enable Pulse Write	(11) TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	165	-	ns
Data Setup Time	(12) TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	165	-	ns
Data Hold Time	(13) TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ms
Enable Pulse Width	(14) TELEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	175	-	ns
Write to End of Write	(15) TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	165	-	ns
Data Setup Time	(16) TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	165	-	ns
Data Hold Time	(17) TEHDX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	0	-	ns

TABLE 3. HS-65T262RRH ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 7	$T_A = +25^oC$	-	8	pF
		VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 8	$T_A = +25^oC$	-	TBD	pF
Output Capacitance	CO	VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 7	$T_A = +25^oC$	-	10	pF
		VDD = Open, f = 1MHz, All Measurements Referenced To Device Grounds	6, 8	$T_A = +25^oC$	-	TBD	pF
Write Enable to Output in High Z	(18) TWLQZ	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	30	ns
Write Enable High to Output ON	(19) TWHQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Enable to Output ON	(20) TELQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Output Enable High to Output in High Z	(21) TEHQZ	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	30	ns
Chip Disable to Output Hold Time	(22) TEHQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	15	-	ns
Address Invalid Output Hold Time	(23) TAXQX	VDD = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
High Level Output Voltage	VOH2	VDD = 4.5V, IO = -100µA	6	$-55^oC \leq T_A \leq +125^oC$	VDD -0.4V	-	V

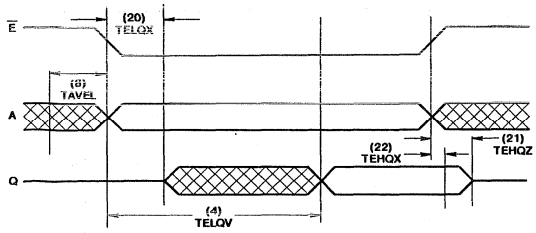
NOTES:
1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 6mA/MHz increase in IDDOP.
5. Tested as follows: f = 3MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. Applies to DIP device types only.
8. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Group C		Samples/5005	N/A	1, 7
Group D		Samples/5005	1, 7	1, 7
Group E	Subgroup 2	Samples/5005	1, 7	1, 7

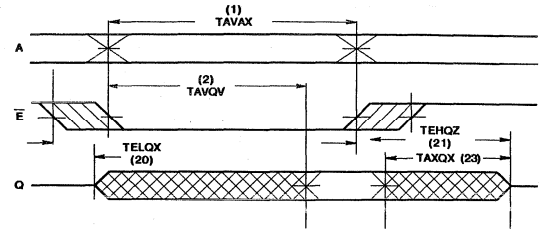
Read Cycles

READ CYCLE 1: CONTROLLED BY E



NOTE: $\overline{W}$ is held high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until E goes high.

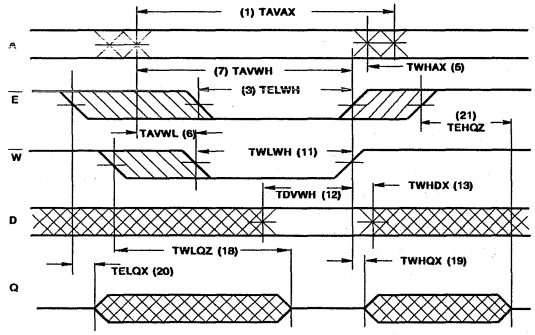
READ CYCLE 2: CONTROLLED BY ADDRESS



NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

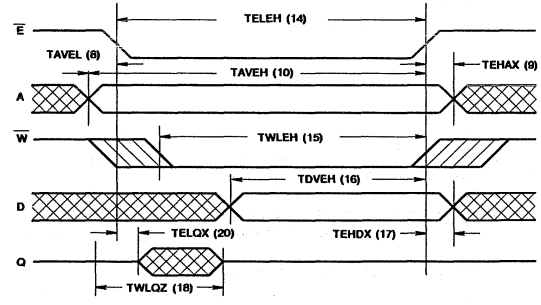
Write Cycles

WRITE CYCLE 1: CONTROLLED BY $\overline{W}$ (LATE WRITE)



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

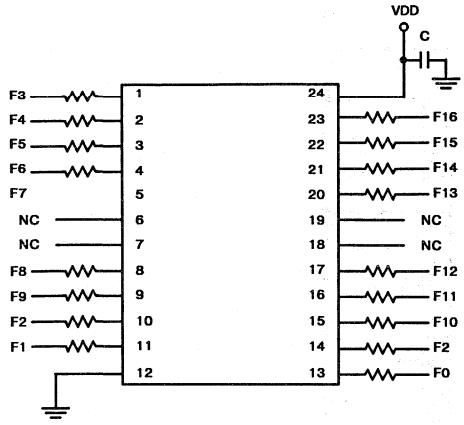
WRITE CYCLE 2: CONTROLLED BY $\overline{E}$ (EARLY WRITE)



NOTE: In this mode, $\overline{W}$ rises after $\overline{E}$. If W falls before $\overline{E}$ by a time exceeding TWLQZ (Max) TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) - TWHQZ (min), then Q will remain in the high impedance state throughout the cycle

Burn-In Circuits

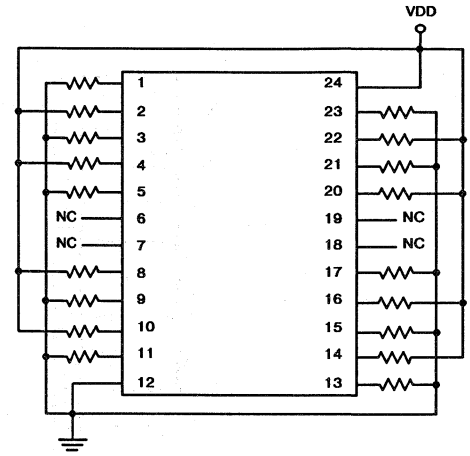
HS-65C262RH 24 PIN FLAT PACK



DYNAMIC CONFIGURATION

NOTES:
All Resistors = 47kΩ ±10%
F0 = 100kHz ± 10%
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2;..... F16 = F15/2
VDD = 6.0V ±0.5V
VIH = 4.5V ± 10%
VIL = -0.2 to +0.8V
C = 0.01nf (Min.)

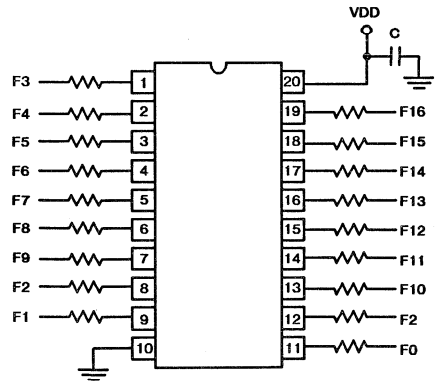
HS-65C262RH 24 PIN FLAT PACK



STATIC CONFIGURATION

NOTES:
All Resistors = 47kΩ ±10%
VDD = 6.0V ±0.5V

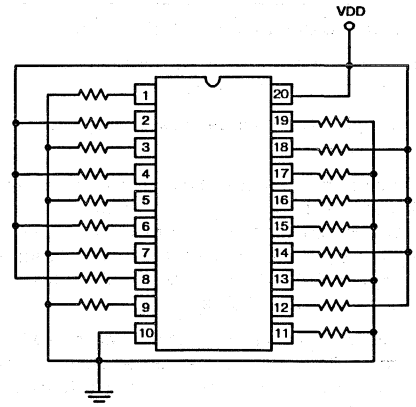
HS-65C262RH 20 LEAD DIP



DYNAMIC CONFIGURATION

NOTES:
All Resistors = 47kΩ ±10%
F0 = 100kHz ± 10%
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2;..... F16 = F15/2
VDD = 6.0V ±0.5V
VIH = 4.5V ± 10%
VIL = -0.2 to +0.8V
C = 0.01nf (Min.)

HS-65C262RH 20 LEAD DIP

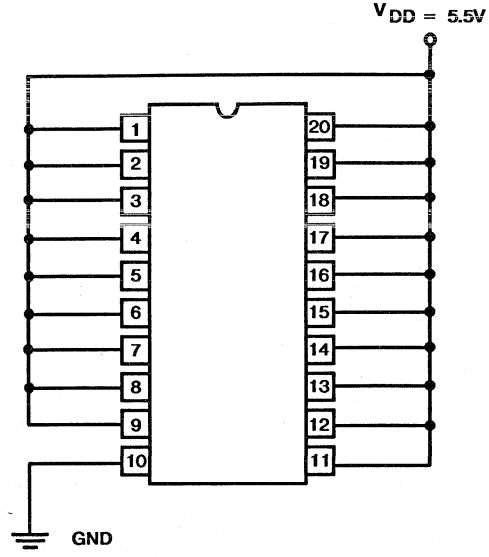


STATIC CONFIGURATION

NOTES:
All Resistors = 47kΩ ±10%
VDD = 6.0V ±0.5V

Irradiation Circuits

HS-65C262RH/HS-25T262RH 20 PIN LEAD DIP



NOTES:
Pin 10 is tied to GND
Output (Pin 8) floats
All other pins tied to VDD
VDD = 5.5V

Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 2 x 10^5 Rad(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = +5V. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The sample devices shall be tested within one hour after irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.

Metallization Topology

DIE DIMENSIONS:
258 x 177 x 19±1 mils

METALLIZATION:
Type: Silicon-Aluminum
Thickness: 11.5kÅ to 14.5kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ to 9kÅ

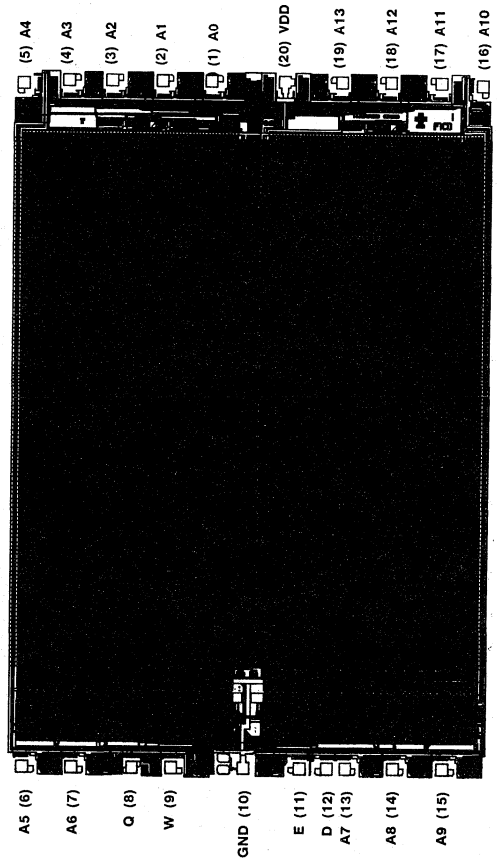
DIE ATTACH:
Material: Gold-Silicon Eutectic Alloy
Temperature: Braze Seal DIP - 460°C (Max)
Braze Seal Flatpack - 460°C (Max)

WORST CASE CURRENT DENSITY: 1.6 x 10^5 Amps/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-65C262/65T262RH



HARRIS HS-65758RH

ADVANCED INFORMATION

July 1990

Radiation Hardened 256K Bit SOI SRAM

Features

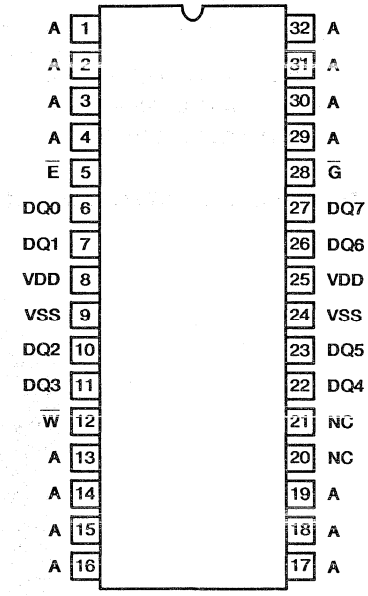
- 0.9μm Radiation Hardened SOI CMOS
  - Total Dose ..... 1×10^6 RADs
  - Data Upset ..... 1×10^{11} RAD/Sec
  - Latch Up Free SOI Process
  - SEU Error Rate ..... $< 1 \times 10^{-12}$ Errors/Bit Day
- Available in 3 Organizations
  - 256K x 1
  - 32K x 8
  - 64K x 4
- Fast Access Time < 25ns Over Voltage, Temperature and Radiation
- Single 5V Power Supply
- Low Power Consumption
  - IDDSB < 500μA Pre RAD
  - IDDSB < 2mA Post 1MRAD
  - IDDOP 145mA (x 1, 40MHz)
  - IDDOP 220mA (x 8, 40MHZ)
- Fully Static 6T Memory Cell

Description

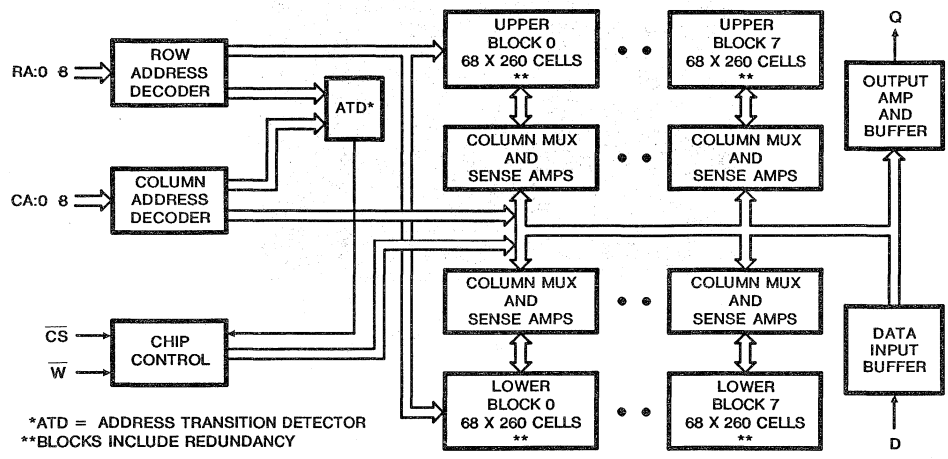
The HS-65758RH is an asynchronous, fully static RAM fabricated with the Harris SIMOX (Silicon Isolated by Implanted Oxygen) radiation hardened process. The use of this process provides excellent total dose, dose rate and single event immunity. As with any oxide isolated circuits, the HS-65758RH will not latch-up under any conditions. This high speed SRAM is available in 256 x 1, 64K x 4 and 32K x 8 organizations.

Pinout

32K x 8 SRAM
TOP VIEW



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

HS-6617RH

Radiation Hardened 2K x 8 CMOS PROM

July 1990

Features

- Total Dose ..... 1×10^5 RAD (Si)
- Latch-Up Free ..... $>1 \times 10^{12}$ RAD (Si)/s
- Field Programmable
- Functionally Equivalent to HM-6617
- Pin Compatible with Intel 2716
- Low Standby Power ..... 550µW Max.
- Low Operating Power ..... 137.5mW/MHz Max.
- Fast Access Time..... 100ns Max.
- TTL Compatible Inputs/Outputs
- Synchronous Operation
- On Chip Address Latches
- Three-State Outputs
- Nicrome Fuse Links
- Easy Microprocessor Interfacing
- Military Temperature Range.....-55°C to +125°C

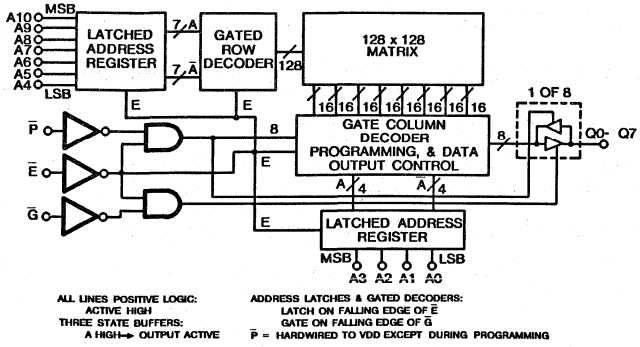
Description

The Harris HS-6617RH is a radiation hardened 16K CMOS PROM, organized in a 2K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and is designed to be functionally equivalent to the HM-6617. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structure, such as the HS-80C85RH or HS-80C86RH. The output enable control ($\overline{G}$) simplifies microprocessor system interfacing by allowing output data bus control, in addition to, the chip enable control. Synchronous operation of the HS-6617RH is ideal for high speed pipelined architecture systems and also in synchronous logic replacement functions.

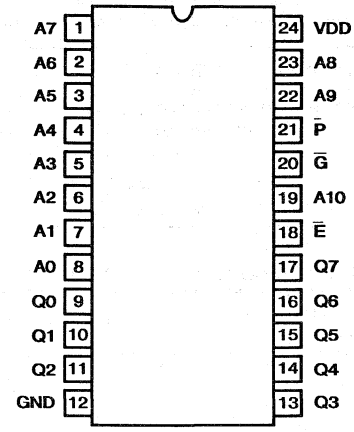
Applications for the HS-6617RH CMOS PROM include low power microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement. A high reliability version is available for satellite and other critical applications. Contact your nearest Harris representative.

Functional Diagram



Pinouts

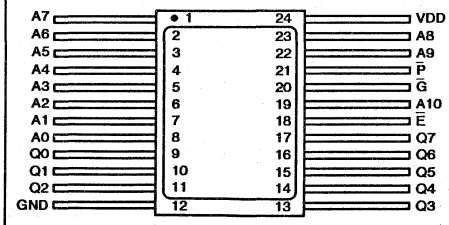
24 PIN BRAZE SEAL DIP
TOP VIEW



PIN NAMES

A	Address Input	$\overline{P}$	Program Enable ($\overline{P}$ Hardwired to VDD, except during programming)
Q	Data Output		
$\overline{E}$	Chip Enable		
$\overline{G}$	Output Enable		

24 PIN FLATPACK CARRIER
TOP VIEW



11 MEMORIES

Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND) .... +7.0V
Input or Output Voltage Applied for all Grades ..... GND-0.3V to V_{DD}+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	56°C/W	12°C/W
Braze Seal FP Package	91.3°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.89W
Braze Seal FP Package 0.55W
Gate Count ..... 5473 Gates

CAUTION: As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance" are the only conditions recommended for satisfactory operation. As with all semiconductors, thermal characteristics should always be considered during system design.

Operating Conditions

Operating Supply Voltage (V_{DD}) ..... 4.5V to 5.5V
Operating Temperature (T_A) ..... -55°C to +125°C
Input Low Voltage (V_{IL}) ..... 0V to +0.8V
Input High Voltage (V_{IH}) ..... +2.4V to V_{DD}

TABLE 1. HS-6617RH D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

D.C. PARAMETERS	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	V_{OH1}	V_{DD} = 4.5V, IO = -2.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{DD} = 4.5V, IO = +4.8mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	V_{DD} = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or V_{DD}	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	10	µA
Input Leakage Current	II	V_{DD} = 5.5V, VI = GND or V_{DD}, $\overline{P}$ Not Tested	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB	VI = V_{DD} or GND, V_{DD} = 5.5V, IO = 0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Operating Supply Current	IDDOP	V_{DD} = 5.5V, $\overline{G}$ = GND, (Note 3), f = 1MHz, IO = 0mA, VI = V_{DD} or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	25	mA
Functional Test	FT	V_{DD} = 4.5V (Note 12)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	

TABLE 2. HS-6617RH A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	TAVQV	V_{DD} = 4.5V and 5.5V (Note 5)	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	120	ns
Output Enable Access Time	TGLQV	V_{DD} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	50	ns
Chip Enable Access Time	TELQV	V_{DD} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	100	ns
Address Setup Time	TAVEL	V_{DD} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	ns
Address Hold Time	TELAX	V_{DD} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	25	-	ns
Chip Enable Low Width	TELEH	V_{DD} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	120	-	ns
Chip Enable High Width	TEHEL	V_{DD} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	40	-	ns
Read Cycle Time	TELEL	V_{DD} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	160	-	ns

NOTES: 1. All voltages referenced to Device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≈ 50pF.
3. Typical derating = 20mA/MHz increase in IDDOP.
4. All tests performed with $\overline{P}$ hardwired to V_{DD}.
5. TAVQV = TELQV + TAVEL

TABLE 3. HS-6617RH A.C. AND D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 4) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	C_{IN}	V_{DD} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 9	+25°C	-	10	pF
		V_{DD} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 11	+25°C	-	10	pF
I/O Capacitance	$C_{I/O}$	V_{DD} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 9	+25°C	-	12	pF
		V_{DD} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 11	+25°C	-	12	pF
Chip Enable Time	TELQX	V_{DD} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	5	-	ns
Output Enable Time	TGLQX	V_{DD} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	5	-	ns
Chip Disable Time	TEHQZ	V_{DD} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	-	50	ns
Output Disable Time	TGHQZ	V_{DD} = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	-	50	ns
Output High Voltage	V_{OH2}	V_{DD} = 4.5V, IO = 100µA	6	$-55°C \leq T_A \leq +125°C$	V_{DD}-1V	-	V

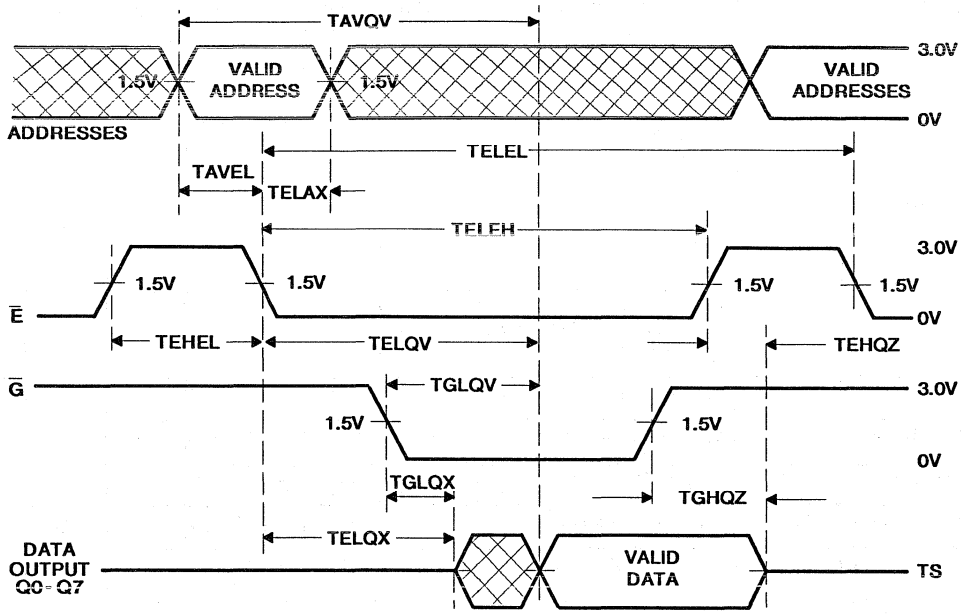
NOTES:
6. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after design or process changes which would affect these characteristics.
7. Tested as follows: f = 2MHz, V_{IH} = 2.4V, V_{IL} = 0.4V, I_{OH} = -4.0mA, $V_{OH} \geq$ 1.5V, and $V_{OL} \leq$ 1.5V.
8. This is a "typical" value and not a "maximum" value.
9. Applies to .600 inch Braze Seal Dual-In-Line (DIP) device types only.
10. Applies to .300 inch Ceramic Dual-In-Line (DIP) device types only.
11. Applies to Braze Seal Flat Pack device types only.
12. Tested as follows: f = 1MHz, V_{IH} = 2.4V, V_{IL} = 0.8V, I_{OH} = -1mA, I_{OL} = +1mA, $V_{OH} \geq$ 1.5V, $V_{OL} \leq$ 1.5V.

TABLE 4. APPLICABLE SUBGROUPS

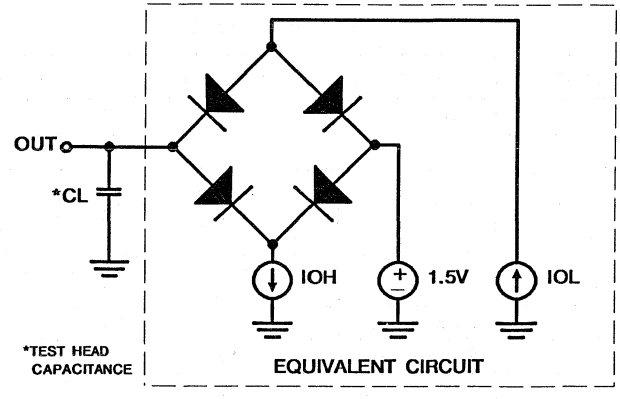
CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Groups C		Samples/5005	N/A	1, 7
Group D		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

Switching Waveforms

READ CYCLE

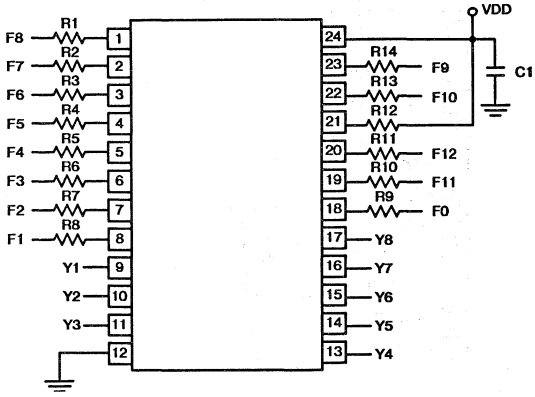


Test Circuit



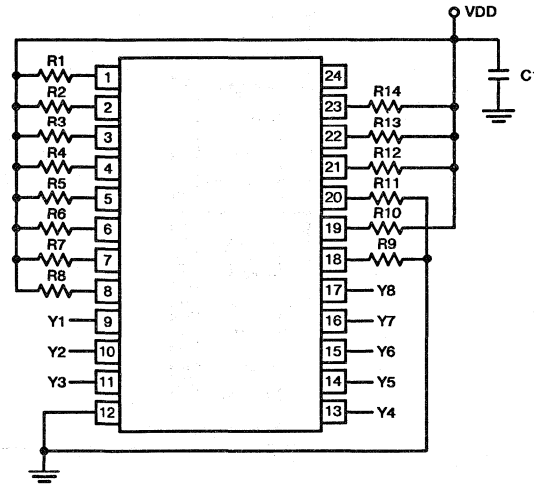
Burn-In Circuits

HS-6617RH (.600) 24 BRAZE SEAL FLAT PACK



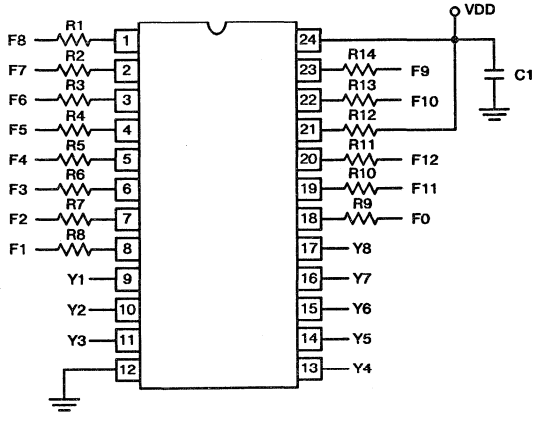
DYNAMIC CONFIGURATION

HS-6617RH (.600) 24 BRAZE SEAL FLAT PACK



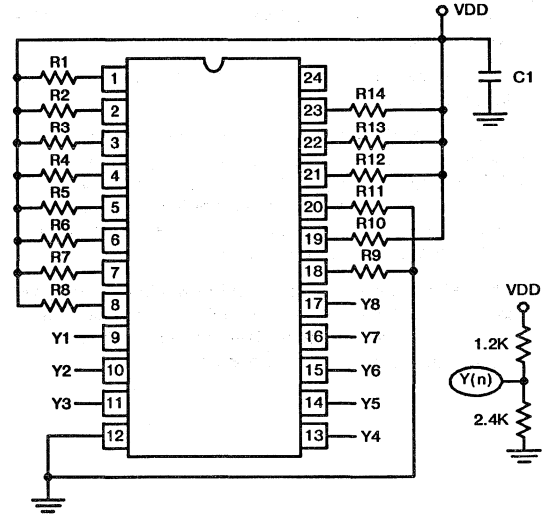
STATIC CONFIGURATION

HS-6617RH (.600) 24 BRAZE SEAL DIP



DYNAMIC CONFIGURATION

HS-6617RH (.600) 24 BRAZE SEAL DIP

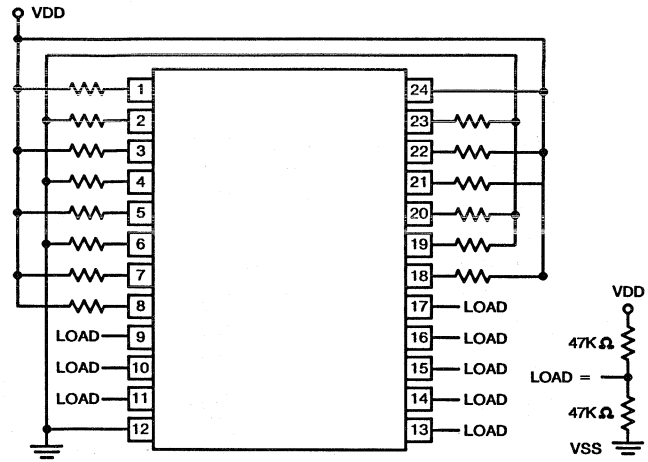


STATIC CONFIGURATION

NOTES:
Power Supply: VDD = 6.00 ±0.5V
All Resistors = 47kΩ ±5%, unless otherwise noted
Input Levels: VIH = 2.2V to VDD + 0.3V; VIL = -0.3V to 0.3V
F0 = 100kHz ± 10%, 50% Duty Cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2;..... F12 = F11/2
C1 = 0.01µf

Irradiation Circuits

HS-6617RH 24 PIN FLAT PACK



NOTES:
Power Supply: VDD = 5.5V
All Resistors = 47KΩ

Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = +5V. The dose rate shall be between 100 rads/sec and 300 rads/sec.
4. The sample devices shall be tested within one hour after irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.

Metallization Topology

DIE DIMENSIONS:
164 x 250 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ - 15kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ - 9kÅ

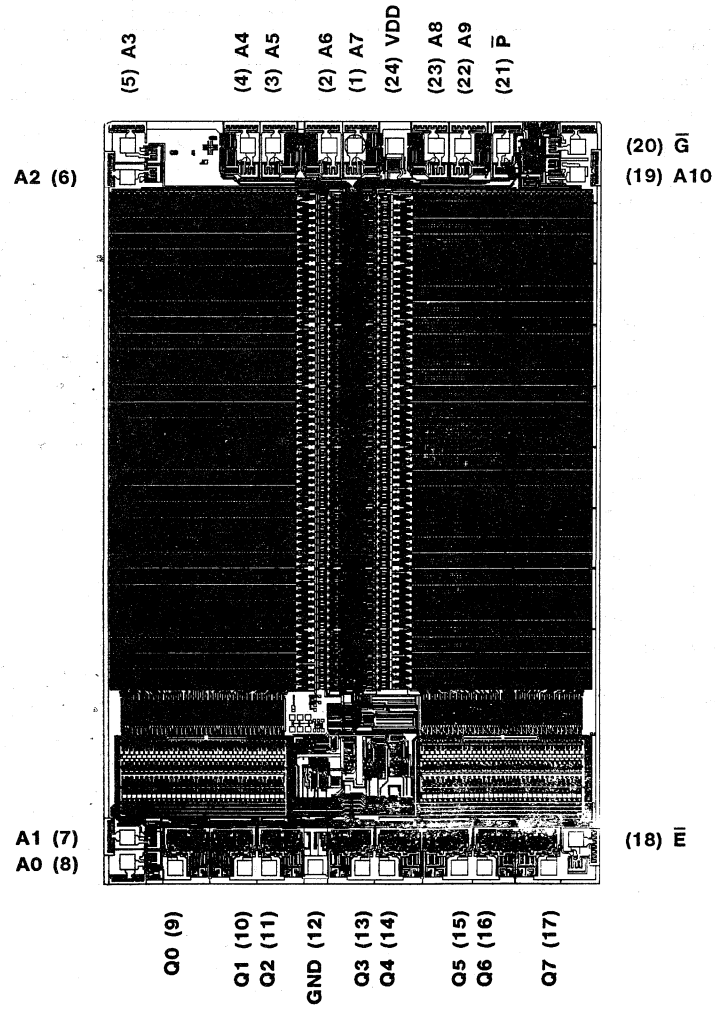
DIE ATTACH:
Material: Si - Au Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Braze Seal Flat Pack — 460°C (Max)

WORST CASE CURRENT DENSITY:
1×10^5 A/cm^2

SUBSTRATE POTENTIAL:
VDD

Metallization Mask Layout

HS-6617RH



DESIGN INFORMATION

2K x 8 CMOS PROM

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Background Information HS-6617RH Programming

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IL}	Input "0"	0.0	0.2	0.8	V	
V_{IH}	Voltage "1"	V_{DD}-2	V_{DD}	V_{DD}+0.3	V	6
V_{DDPROG}	Programming V_{DD}	10.0	10.0	10.0	V	2
V_{DD1}	Operating V_{DD}	4.5	5.5	5.5	V	
V_{DD2}	Special Verify	4.0	-	6.0	V	3
t_d	Delay Time	1.0	1.0	-	µs	
t_r	Rise Time	1.0	10.0	10.0	µs	
t_f	Fall Time	1.0	10.0	10.0	µs	
TEHEL	Chip Enable Pulse Width	50	-	-	ns	
TAVEL	Address Valid to Chip Enable Low Time	20	-	-	ns	
TELQV	Chip Enable Low to Output Valid Time	-	-	120	ns	
t_{pw}	Programming Pulse Width	90	100	110	µs	4
I_{IP}	Input Leakage at $V_{DD} = V_{DDPROG}$	-10	+1.0	10	µA	
I_{OP}	Data Output Current at $V_{DD} = V_{DDPROG}$	-	-5.0	-10	mA	
R_n	Output Pull-Up Resistor	5	10	15	kΩ	5
T_A	Ambient Temperature	-	25	-	°C	

NOTES:

1. All inputs must track V_{DD} (pin 24) within these limits.
2. V_{DDPROG} must be capable of supplying 500mA. V_{DDPROG} Power Supply tolerence ±3% (Max.)
3. See Steps 22 through 29 of the Programming Algorithm.
4. See Step 11 of the Programming Algorithm.
5. All outputs should be pulled up to V_{DD} through a resistor of value R_n.
6. Except during programming (See Programming Cycle Waveforms).

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Background Information Programming Algorithm

The HS-6617 CMOS PROM is manufactured with all bits containing a logical zero (output low). Any bit can be programmed selectively to a logical one (output high) state by following the procedure shown below. To accomplish this, a programmer can be built that meets the specifications shown, or use of an approved commercial programmer is recommended.

PROGRAMMING SEQUENCE OF EVENTS

1) Apply a voltage of V_{DD1} to V_{DD} of the PROM.
2) Read all fuse locations to verify that the PROM is blank (output low).
3) Place the PROM in the initial state for programming: $\overline{E} = V_{IH}$, $\overline{P} = V_{IH}$, $\overline{G} = V_{IL}$.
4) Apply the correct binary address for the word to be programmed. No inputs should be left open circuit.
5) After a delay of t_d, apply voltage of V_{IL} to $\overline{E}$ (pin 18) to access the addressed word.
6) The address may be held through the cycle, but must be held valid at least for a time equal to t_d after the falling edge of $\overline{E}$. None of the inputs should be allowed to float to an invalid logic level.
7) After a delay of t_d, disable the outputs by applying a voltage of V_{IH} to $\overline{G}$ (pin 20).
8) After a delay of t_d, apply voltage of V_{IL} to $\overline{P}$ (pin 21).
9) After delay of t_d, raise V_{DD} (pin 24) to V_{DDPROG} with a rise time of t_r. All outputs at V_{IH} should track V_{DD} within V_{DD}-2.0V to V_{DD}+0.3V. This could be accomplished by pulling outputs at V_{IH} to V_{DD} through pull-up resistors of value R_n.
10) After a delay of t_d, pull the output which corresponds to the bit to be programmed to V_{IL}. Only one bit should be programmed at a time.
11) After a delay of t_{pw}, allow the output to be pulled to V_{IH} through pull-up resistor R_n.
12) After a delay of t_d, reduce V_{DD} (pin 24) to V_{DD1} with a fall time of t_f. All outputs at V_{IH} should track V_{DD} with V_{DD}-2.0V to V_{DD}+0.3V. This could be accomplished by pulling outputs at V_{IH} to V_{DD} through pull-up resistors of value R_n.
13) Apply a voltage of V_{IH} to $\overline{P}$ (pin 21).
14) After a delay of t_d, apply a voltage of V_{IL} to $\overline{G}$ (pin 20).
15) After a delay of t_d, examine the outputs for correct data. If any location verifies incorrectly, it should be considered a programming reject.
16) Repeat steps 3 through 15 for all other bits to be programmed in the PROM.

POST-PROGRAMMING VERIFICATION

17) Place the PROM in the post-programming verification mode: $\overline{E} = V_{IH}$, $\overline{G} = V_{IL}$, $\overline{P} = V_{IH}$, V_{DD} (pin 24) = V_{DD1}.
18) Apply the correct binary address of the word to be verified to the PROM.
19) After a delay of t_d, apply a voltage of V_{IL} to $\overline{E}$ (pin 18).
20) After a delay of t_d, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
21) Repeat steps 17 through 20 for all possible programming locations.

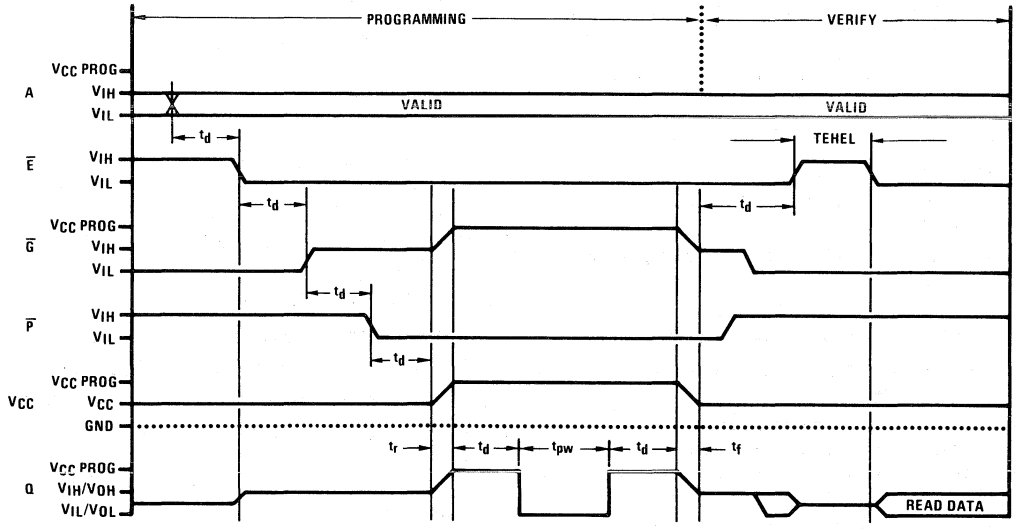
POST-PROGRAMMING READ

22) Apply a voltage of V_{DD2} = 4.0V to V_{DD} (pin 24).
23) After a delay of t_d, apply a voltage of V_{IH} to $\overline{E}$ (pin 18).
24) Apply the correct binary address of the word to be read.
25) After a delay of TAVEL, apply a voltage of V_{IL} to $\overline{E}$ (pin 18).
26) After a delay of TELQV, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
27) Repeat steps 23 through 26 for all address locations.
28) Apply a voltage of V_{DD2} = 6.0V to V_{DD} (pin 24).
29) Repeat steps 23 through 26 for all address locations.

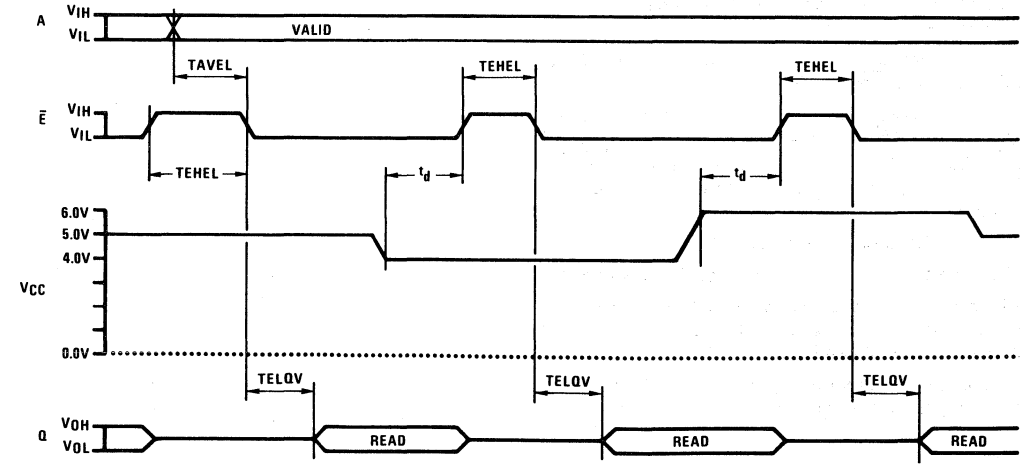
DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

HS-6617RH PROGRAMMING CYCLE



HS-6617RH POST PROGRAMMING VERIFY CYCLE



RAD-HARD 12

LOGIC CIRCUITS

Harris offers three families of Rad-Hard logic; information on these families is presented differently.

The HCS and HCTS families are broken down into gates, flip-flops and MSI circuit functions. Two datasheets (one for HCS and one for HCTS) contain information on all of the gates. Flip-flop and MSI sections contain individual datasheets for each product.

The CD4000 series consists of an index to data, radiation characteristics and standard and nonstandard electrical characteristics. Standard electricals apply across the family; nonstandard characteristics are those that deviate from the standard table and are listed by device type.

HCS/HCTS Family Description

The high speeds and low quiescent power dissipation that characterizes the Harris HC/HCT family are made possible by utilizing a three-micron, self-aligned silicon gate CMOS process. The three micron process minimizes the internal parasitic capacitances of the circuit, which results in increased switching speed.

The polysilicon gates of the transistors are deposited over a thin gate oxide before the source and drain diffusions are defined. Ion implantation is then used to form the source and drain areas, with the polysilicon gates acting as a mask for the implantation. The source and drain are automatically aligned to the gate, hence the expression "self-aligned gate" process. In this manner, gate-to-source and gate-to-drain capacitances are minimized.

HCS/HCTS Structure

The basic polysilicon gate structure described above, is used for the HCS/HCTS (CMOS/SOS) family except that the devices are made on epitaxial Si islands on a sapphire substrate. This technique greatly reduces device capacitance and completely eliminates latch-up. A special SOS process is also used to achieve the megarad hardness levels.

HCS/HCTS Derived from HC/HCT Layouts

- Optimized output device size ratios for CMOS/SOS process parameters
- Optimized input device size ratios to meet:
  - V_{IH} = 2.5V
  - V_{IL} = 0.8V
- ESD protection by use of "closed" (edgeless) input and output transistors as well as CMOS/SOS compatible resistor/diode circuitry
- 200 functions from 20 basic masks

The conversion from Bulk Silicon structure to CMOS/SOS is relatively straightforward. Similar logic functions, or functions with similar pinouts, are combined into "groups" where all mask levels except metal are common, and the indivisual IC pinout functions are realized by metal mask options. Input and output protection diodes are also modified to suit the SOS technology.

Circuit functions are offered in two basic logic series, as follows:

1. HCTSXXXX-series types - feature LSTTL input voltage level compatibility and provide high speed CMOS direct drop-in replacements of LSTTL devices.
2. HCSXXXX-series types - feature CMOS input voltage level compatibility and are intended for use in CMOS systems.

HCS/HCTS Family Features

- New High Speed Low Power Radiation Hardened CMOS Logic Family
- 20X Faster Than 4000 Series
- SOS Based
- Wide Choice of Logic Functions Based on Bulk High Speed CMOS Family
- Class S Qualified

Exceptional Radiation Hardness Capability and Shorter Propagation Delay Times

Test results indicate that these devices show exceptionally high tolerance to total dose gamma radiation. Moreover, the sapphire substrate also enhances switching performance, allowing the devices to offer shorter propagation delay times than standard HC/HCT CMOS logic.

Radiation Performance - Inherent Radiation Properties of SOS

- Total Dose .... 200k RADs (Si) and 10^6 RADs (Si)
- Transient Upset ..... $> 10^{10}$ RADs (Si)/s Rate
- SEU ..... $< 10^{-10}$ Upsets/Bit/Day (For Storage Elements)
- Latch-Up ..... Not Possible (SOS Technology)

HCTS Speed Performance Examples

TYPE	PARAMETER	CONDITION	SOS 3μ HCTS (ns)	BULK 3μ HCT (ns)
HCTS240 Octal Buffer	$t_{PLH_{A-Y}}$ $t_{PHL_{A-Y}}$	Max (+25°C) (50pF) (4.5V)	15 15	22 22
	$t_{PLH_{A-Y}}$ $t_{PHL_{A-Y}}$	Max (+125°C) (50pF) (4.5V)	20 20	33 33
HCTS161 4-Bit Binary Counter	$t_{PLH_{A-Y}}$ $t_{PHL_{A-Y}}$	Max (+25°C) (50pF) (4.5V)	23 31	39 39
	$t_{PLH_{A-Y}}$ $t_{PHL_{A-Y}}$	Max (+125°C) (50pF) (4.5V)	28 36	59 59
HCTS244 Octal Buffer	$t_{PLH_{A-Y}}$ $t_{PHL_{A-Y}}$	Max (+25°C) (50pF) (4.5V)	17 23	25 25
	$t_{PLH_{A-Y}}$ $t_{PHL_{A-Y}}$	Max (+125°C) (50pF) (4.5V)	20 26	38 38
HCTS373 Octal Latch	$t_{PLH_{D-Q}}$ $t_{PHL_{D-Q}}$	Max (+25°C) (50pF) (4.5V)	19 26	32 32
	$t_{PLH_{D-Q}}$ $t_{PHL_{D-Q}}$	Max (+125°C) (50pF) (4.5V)	24 30	48 48
HCTS374 Octal D Flip-Flop	$t_{PLH_{CL-Q}}$ $t_{PHL_{CL-Q}}$	Max (+25°C) (50pF) (4.5V)	27 31	33 33
	$t_{PLH_{CL-Q}}$ $t_{PHL_{CL-Q}}$	Max (+125°C) (50pF) (4.5V)	31 35	50 50

Worst-Case Performance Comparisons - Radiation Hardened CMOS/SOS Logic vs. CMOS and TTL Bipolar

TYPE	S4LS240	54ALS240	CD4502B	54HCT240	HCTS240
Technology	TTL Bipolar	TTL Bipolar	7μ CMOS	3μ CMOS	3μ CMOS/SOS
Function	Octal Buffer 3-State Inverting	Octal Buffer 3-State Inverting	Hex Buffer 3-State Inverting	Octal Buffer 3-State Inverting	Octal Buffer 3-State Inverting
Quiescent Supply Current	50mA at 5.5V -55°C/+125°C	25mA at 5.5V -55°C/+125°C	0.03mA at 5.0V +125°C	0.16mA at 6.0V -55°C/+125°C	0.25mA at 5.5V +125°C
t_{PLH} or t_{PHL}	18ns at 5.0V C_L = 45pF +25°C	12ns at 4.5V C_L = 50pF -55/+25/+125°C	380ns at 5.0V C_L = 50pF +25°C	22ns at 4.5V C_L = 50pF +25°C	15ns at 4.5V C_L = 50pF +25°C
I_{OH}	-12mA at 4.5V V_O = 2.0V V_{IL} = 0.5V -55/+25/+125°C	-12mA at 4.5V V_O = 2.0V -55/+25/+125°C	00.36mA at 5.0V V_O = 2.5V +125°C	-6mA at 4.5V V_O = 3.7V V_{IL} = 0.8V -55/+125°C	Typ 35mA at 4.5V V_O = 3.1V +125°C

Class S Screening Per Mil-Std-883, Method 5004

Wafer Lot Acceptance (All Lots)	Method 5007 (Includes SEM)
Radiation Verification (Each Wafer)	Method 1019 - 200k RADs (Si), 4 samples/wafer, 0 rejects
Nondestructive Bond Pull (100%)	Method 2023
Internal Visual Inspection (100%)	Modified Method 2010 - see 'Internal Visual Inspection'
Temperature Cycling (100%)	Method 1010 - Condition C (-65°C to +150°C)
Constant Acceleration (100%)	Method 2001 - Condition E_1, Y_1, (30,000 g)
PIND Testing (100%)	Method 2020 - Condition A (20 g peak at 60Hz)
External Visual Inspection (100%)	-
Initial Electrical Tests (100%)	See Table 1
Serialization (100%)	-
Static Burn-In I (100%)	24 hours, +125°C
Interim Electrical Tests I (100%)	See note below, see Table I
Static Burn-In II (100%)	24 hours, +125°C
Interim Electrical Tests (100%)	See note below, see Table I
Dynamic Burn-In II (100%)	240 hours, +125°C
Interim Electrical Tests (100%)	PDA 5% all tests, PDA 3% functional, see Table I
Final Electrical Tests (100%)	See Table I
Fine and Gross Seal (100%)	Method 1014
Radiographic (100%)	Method 2012 (2 views)
External Visual (100%)	Method 2009
Quality Conformance	
Group A (All tests)	Method 5005 (Class S), see Table I
Group B (Optional)	Method 5005 (Class S), see Table I
Group D (Optional)	Method 5005 (Class S), see Table I
CSI and or GSI (Optional)	-

NOTE:
Failures from Interim Electrical and delta calculations are combined for determining PDA (PDA = 5% all tests, 3% functional)

Visual Inspection For SOS Technology

Visual inspection for Class S is performed to Mil-Std-883, Method 2010, Condition A **with the following modification:** Semicircular cracks not in an active area, which start and end at the pellet edge, are acceptable.

Table I. Electrical Tests

Post Radiation	See Post-Radiation Performance, $T_A = +25°C$
Initial Electrical Tests	See Static, Switching, and Functional Characteristics, $T_A = +25°C$
Interim Electrical Tests	Same as above (+25°C)
Final Electrical Tests	Same as above (-55°C, +125°C)
Quality Conformance: (Optional-must be indicated on P.O.)	
Group A	Same as above (-55°C, +25°C, +125°C)
Group B	See Static, Switching, and Functional Characteristics at -55°C, +25°C, +125°C
Group D	See Static, Switching, and Functional Characteristics at -55°C, +25°C, +125°C

PRELIMINARY

HCS00
HCS02
HCS04
HCS08
HCS27
HCS32

High Reliability, Radiation Hardened High Speed CMOS SOS Gates with CMOS Compatible Inputs

Aerospace Class S Screening

Radiation Features

- Radiation hardened to 200k or 1M RADs (Si)
- Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day
- Latch-up free under transient radiation
- Transient upset > 10^{10} RADs/sec, 20ns pulse

These gates utilize advanced CMOS/SOS technology to achieve high speed operation similar to LSTTL and high speed CMOS while providing radiation hardness. These parts are a member of a family of radiation hardness, high speed, CMOS/SOS logic devices with CMOS compatible inputs.

These gates are supplied in 14 lead weld seal ceramic flatpack packages (K suffix) and 14 lead dual-in-line ceramic packages (D suffix).

Family Features

- Fanout (over temperature range)
  - Standard outputs ..... 10 LSTTL loads
  - Bus driver outputs ..... 15 LSTTL loads
- Wide operating temperature range .....-55°C to +125°C
- Significant power reduction compared to LSTTL logic ICs
- HCS types
  - CMOS input compatibility ..... $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

Operating Conditions T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range

CHARACTERISTICS	LIMITS		UNITS
	MIN	MAX	
DC Operating Voltage Range	4.5	5.5	V

Maximum Ratings, Absolute Maximum Values

DC Supply Voltage Range (V_{CC}), All voltage values referenced to V_{SS} terminal ..... -0.5V to +7V
Input Voltage Range, All Inputs ..... -0.5 to V_{CC} +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output 25mA
Power Dissipation Per Package (P_D)
- T_A = -55°C to +100°C 500mW
- T_A = +100°C to +125°C ..... Derate Linearly at 12mW/°C 200mW

Device Dissipation Per Output Transistor
- T_A = Full Package Temperature Range 100mW

θ_{jc} ..... 28°C/W
T_{jmax} ..... +175°C
Operating Temperature Range (T_A) .....-55°C to +125°C
Storage Temperature Range (T_{stg}) .....-65°C to +150°C
Lead Temperature (During Soldering) For Package
- At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) for case for 10s maximum ..... +265°C

Static Electrical Characteristics V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS +25°C MIN	LIMITS +25°C MAX	LIMITS -55°C/+125°C MIN	LIMITS -55°C/+125°C MAX	UNITS
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	10	-	200	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.8	-	-4	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{DD}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	40	-	52	pF

* Guaranteed but not tested **Characterized but not tested

Switching Characteristics t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN	LIMITS +25°C MAX	LIMITS -55°C/+125°C MIN	LIMITS -55°C/+125°C MAX	UNITS
Propagation Delay	t_{PHL}	4.5	-	18	-	20	ns
Input to Output	t_{PLH}	4.5	-	20	-	22	ns

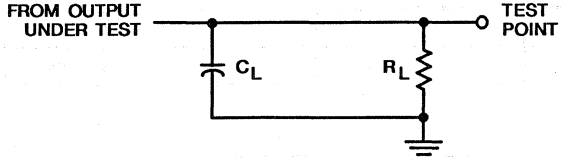


Figure 1. Load Circuit for t_{PHL}, t_{PLH}

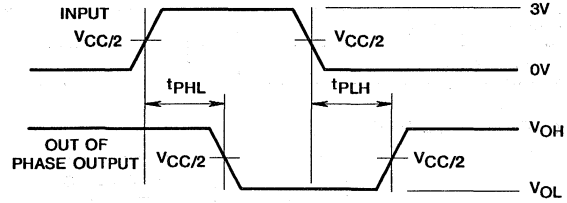


Figure 2. Timing Diagrams

Inherent Radiation Properties of SOS

Latch-Up ..... Not Possible
Transient Survival ..... > 10^{12} RADs (Si)/s
Transient Upset ..... > 10^{10} RADs (Si)/s

Post Radiation* Performance $T_A = +25^oC$

* Radiation measurements are made on 4 samples/wafer. The limits shown are for within 1 hour of irradiation

Static Electrical Characteristics $V_{CC} = 5V \pm 10\%$

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k RADS (Si)		1M RADS (Si)		
			MIN	MAX	MIN	MAX	
Quiescent Device Current	I_{CC}	V_{IN} - 0V or V_{CC}	-	0.2	-	1	mA
Output (Sink) Current	I_{OL}	$V_{OUT} = 0.4V$	4	-	4	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC} - 0.4V$	-4	-	-4	-	mA
Output Voltage, Low Level	V_{OL}	$I_{OL} = 50\mu A$	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	$I_{OH} = -50\mu A$	$V_{CC} - 0.1$	-	$V_{CC} - 0.1$	-	V
Input Low Voltage	V_{IL}	-	-	$0.3\,V_{CC}$	-	$0.2\,V_{CC}$	V
Input High Voltage	V_{IH}	-	$0.7\,V_{CC}$	-	$0.7\,V_{CC}$	-	V
Input Leakage Current	I_{IL}	$V_{IN} = 0V$ or V_{CC}	-	±5	-	±5	µA

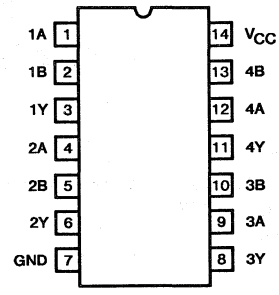
Switching Characteristics $t_r, t_f = 3ns, C_L = 50pF, R_L = 500\Omega$

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k RADS (Si)		1M RADS (Si)		
			MIN	MAX	MIN	MAX	
Propagation Delay	t_{PHL}	4.5	-	20	-	25	ns
Input to Output	t_{PLH}	4.5	-	22	-	26	ns

CPDs By Product Type

TYPE	CPD +25°C TYPICAL	CPD -55°C/+125°C TYPICAL	UNITS
HCS00	38	51	pF
HCS02	TBD	TBD	pF
HCS04	TBD	TBD	pF
HCS08	TBD	TBD	pF
HCS27	TBD	TBD	pF
HCS32	TBD	TBD	pF

HCS00MS
Quad 2-Input NAND Gate



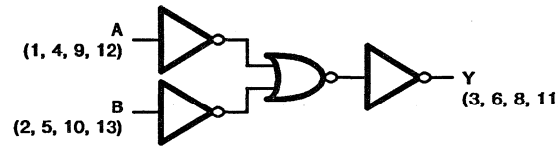
TERMINAL ASSIGNMENT

Type Features

- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

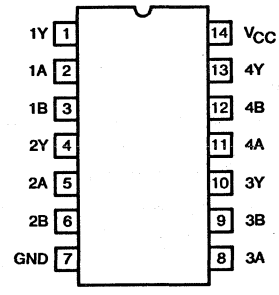
TRUTH TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



LOGIC DIAGRAM

HCS02MS
Quad 2-Input NOR Gate



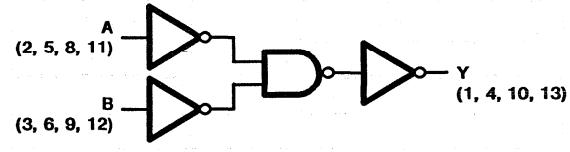
TERMINAL ASSIGNMENT

Type Features

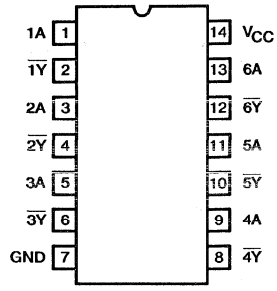
- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

TRUTH TABLE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



LOGIC DIAGRAM

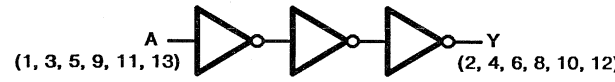


TERMINAL ASSIGNMENT

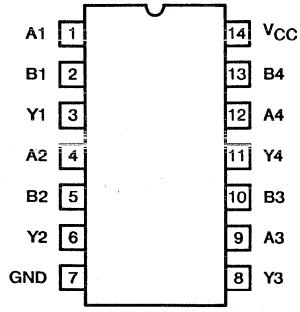
HCS04MS
Hex Inverter

Type Features

- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

HCS08MS
Quad 2-Input AND Gate

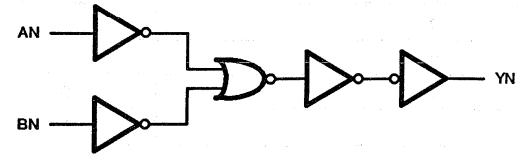
Type Features

- Radiation hardened to 200K or 1 MegaRADs (Si)
- Cosmic Ray Upset Immunity (typical 2 x 10^{-9} errors/bit-day)
- Latch-up free under transient radiation
- Transient upset > 10^{10} RADs/s 20ns pulse

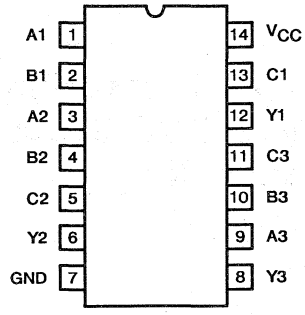
TRUTH TABLE

INPUTS		OUTPUT
An	Bn	Yn
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Voltage Level. L = LOW Voltage Level.



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

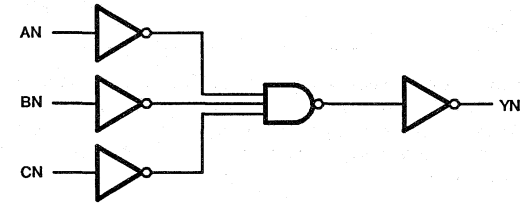
HCS27MS
Triple 3-Input NOR Gate

Type Features

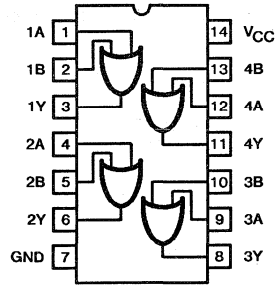
- Radiation hardened to 200K or 1 MegaRADs (Si)
- Cosmic Ray Upset Immunity (typical 2 x 10^{-9} errors/bit-day)
- Latch-up free under transient radiation
- Transient upset > 10^{10} RADs/s 20ns pulse

TRUTH TABLE

An	Bn	Cn	Yn
L	L	L	H
L	L	H	L
L	H	L	L
H	L	L	L
H	H	L	L
L	H	H	L
H	L	H	L
H	H	H	L



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

HCS32MS
Quad 2-Input OR Gate

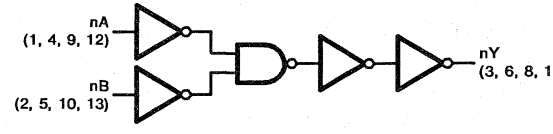
Type Features

- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Voltage Level. L = LOW Voltage Level.



LOGIC DIAGRAM

PRELIMINARY

HCTS00 HCTS14
HCTS02 HCTS20
HCTS04 HCTS21
HCTS08 HCTS27
HCTS10 HCTS30
HCTS11 HCTS32

High Reliability, Radiation Hardened High Speed CMOS SOS Gates with TTL Compatible Inputs

Aerospace Class S Screening

Radiation Features

- Radiation hardened to 200k or 1M RADs (Si)
- Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day
- Latch-up free under transient radiation
- Transient upset > 10^{10} RADs/sec, 20ns pulse

These gates utilize advanced CMOS/SOS technology to achieve high speed operation similar to LSTTL and high speed CMOS while providing radiation hardness. These parts are a member of a family of radiation hardness, high speed, CMOS/SOS logic devices with TTL compatible inputs.

These gates are supplied in 14 lead weld seal ceramic flatpack packages (K suffix) and 14 lead dual-in-line ceramic packages (D suffix).

Family Features

- Fanout (over temperature range)
  - Standard outputs ..... 10 LSTTL loads
  - Bus driver outputs ..... 15 LSTTL loads
- Wide operating temperature range .....-55°C to +125°C
- Significant power reduction compared to LSTTL logic ICs
- HCTS types
  - 4.5 to 5.5V operation
  - LSTTL input logic compatibility
    - V_{IL} = 0.8V maximum, V_{IH} = V_{CC}/2 minimum

Operating Conditions T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range

CHARACTERISTICS	LIMITS MIN	LIMITS MAX	UNITS
DC Operating Voltage Range	4.5	5.5	V

Maximum Ratings, Absolute Maximum Values

DC Supply Voltage Range (V_{CC}), All voltage values referenced to V_{SS} terminal ..... -0.5V to +7V
Input Voltage Range, All Inputs ..... -0.5 to V_{CC} +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output 25mA
Power Dissipation Per Package (P_D)
- T_A = -55°C to +100°C 500mW
- T_A = +100°C to +125°C ..... Derate Linearly at 12mW/°C 200mW

Device Dissipation Per Output Transistor
- T_A = Full Package Temperature Range 100mW

θ_{jc} ..... 28°C/W
T_{jmax} ..... +175°C
Operating Temperature Range (T_A) .....-55°C to +125°C
Storage Temperature Range (T_{stg}) .....-65°C to +150°C
Lead Temperature (During Soldering) For Package
- At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) for case for 10s maximum ..... +265°C

Static Electrical Characteristics V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS +25°C MIN	LIMITS +25°C MAX	LIMITS -55°C/+125°C MIN	LIMITS -55°C/+125°C MAX	UNITS
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	10	-	200	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.8	-	-4	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{DD}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}	-	-	40	-	52	pF

* Guaranteed but not tested

Switching Characteristics t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN	LIMITS +25°C MAX	LIMITS -55°C/+125°C MIN	LIMITS -55°C/+125°C MAX	UNITS
Propagation Delay	t_{PHL}	4.5	-	18	-	20	ns
Input to Output	t_{PLH}	4.5	-	20	-	22	ns

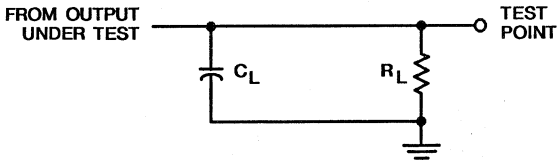


Figure 1. Load Circuit for t_{PHL}, t_{PLH}

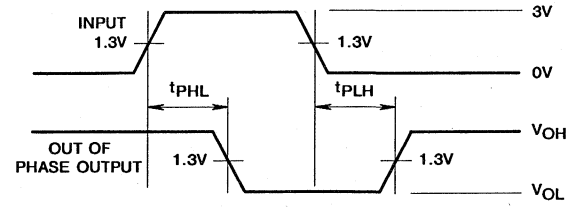


Figure 2. Timing Diagrams

Inherent Radiation Properties of SOS

Latch-Up ..... Not Possible
Transient Survival ..... > 10^{12} RADs (Si)/s
Transient Upset ..... > 10^{10} RADs (Si)/s

Post Radiation* Performance $T_A = +25^oC$

* Radiation measurements are made on 4 samples/wafer. The limits shown are for within 1 hour of irradiation

Static Electrical Characteristics $V_{CC} = 5V \pm 10\%$

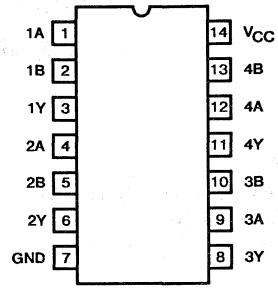
CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k RADS (Si)		1M RADS (Si)		
			MIN	MAX	MIN	MAX	
Quiescent Device Current	I_{CC}	V_{IN} - 0V or V_{CC}	-	0.2	-	1	mA
Output (Sink) Current	I_{OL}	$V_{OUT} = 0.4V$	4	-	4	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC} - 0.4V$	-4	-	-4	-	mA
Output Voltage, Low Level	V_{OL}	$I_{OL} = 50\mu A$	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	$I_{OH} = -50\mu A$	$V_{CC} - 0.1$	-	$V_{CC} - 0.1$	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.4	V
Input High Voltage	V_{IH}	-	$V_{CC}/2$	-	$V_{CC}/2$	-	V
Input Leakage Current	I_{IL}	$V_{IN} = 0V$ or V_{CC}	-	±5	-	±5	µA

Switching Characteristics $t_r, t_f = 3ns, C_L = 50pF, R_L = 500\Omega$

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k RADS (Si)		1M RADS (Si)		
			MIN	MAX	MIN	MAX	
Propagation Delay	t_{PHL}	4.5	-	20	-	25	ns
Input to Output	t_{PLH}	4.5	-	22	-	26	ns

CPDs By Product Type

TYPE	CPD +25°C TYPICAL	CPD -55°C/+125°C TYPICAL	UNITS
HCS00	25	48	pF
HCTS02	27	43	pF
HCTS04	33	63	pF
HCTS08	27	50	pF
HCTS10	32	44	pF
HCTS11	TBD	TBD	pF
HCTS14	17	19	pF
HCTS20	38	77	pF
HCTS21	TBD	TBD	pF
HCTS27	19	19	pF
HCTS30	TBD	TBD	pF
HCTS32	TBD	TBD	pF



TERMINAL ASSIGNMENT

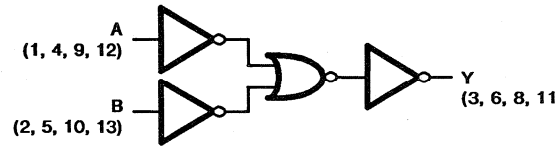
HCTS00MS
Quad 2-Input NAND Gate

Type Features

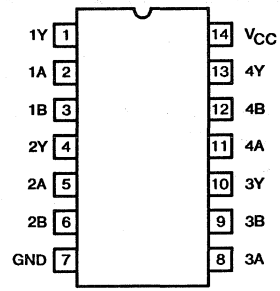
- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

TRUTH TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

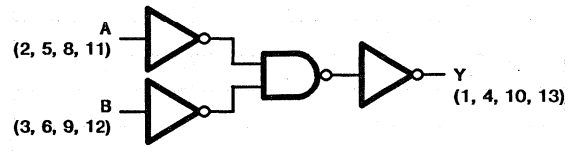
HCTS02MS
Quad 2-Input NOR Gate

Type Features

- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

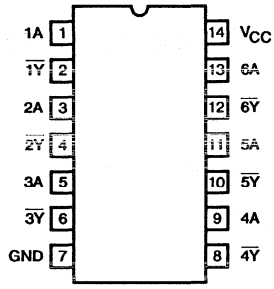
TRUTH TABLE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



LOGIC DIAGRAM

HCTS04MS
Hex Inverter



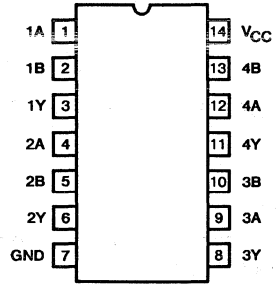
TERMINAL ASSIGNMENT

Type Features

- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

LOGIC DIAGRAM

HCTS08MS
Quad 2-Input AND Gate



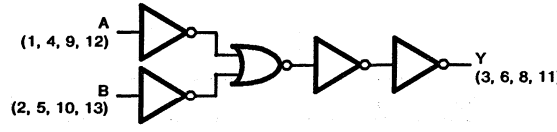
TERMINAL ASSIGNMENT

Type Features

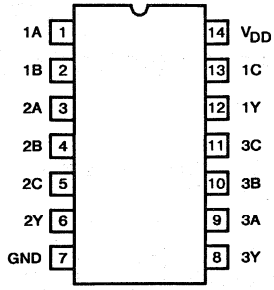
- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

TRUTH TABLE

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

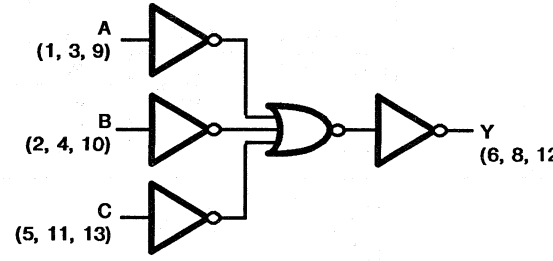
HCTS10MS
Triple 3-Input NAND Gate

Type Features

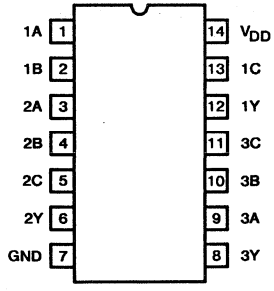
- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

TRUTH TABLE

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

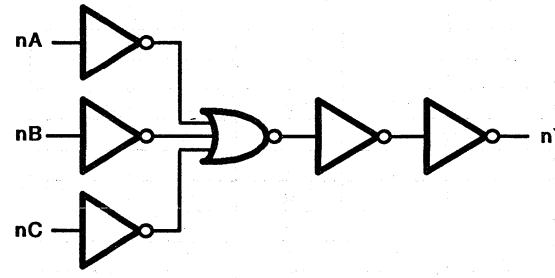
HCTS11MS
Triple 3-Input AND Gate

Type Features

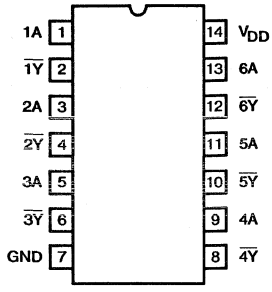
- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

TRUTH TABLE

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	0	1	0
1	1	1	1



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

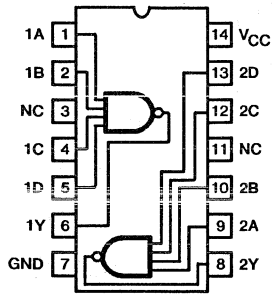
HCTS14MS
Hex Inverter Schmitt Trigger

Type Features

- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

LOGIC DIAGRAM

CHARACTERISTICS		V_{DD}	+25°C MIN	+25°C MAX	-55°C/+125°C MIN	-55°C/+125°C MAX	UNIT
Input Switch Points	Vt+	4.5V	1.2	1.8	1.2	1.8	V
	Vt-	4.5V	0.9	1.6	0.9	1.6	V
	VH	4.5V	0.1	0.9	0.1	0.9	V



TERMINAL ASSIGNMENT

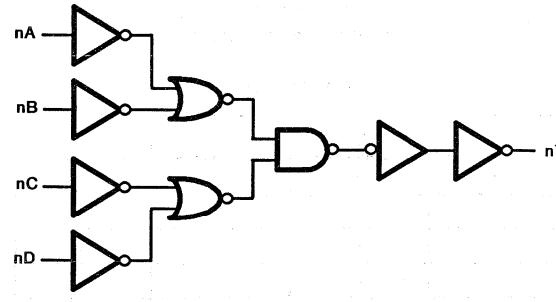
HCTS20MS
Dual 4-Input NAND Gate

Type Features

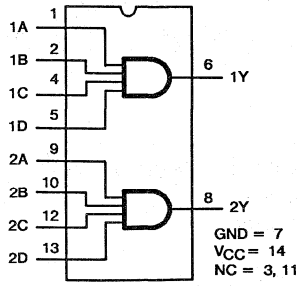
- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

TRUTH TABLE

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

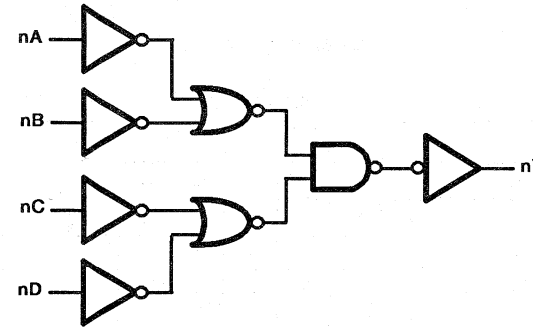
TRUTH TABLE

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

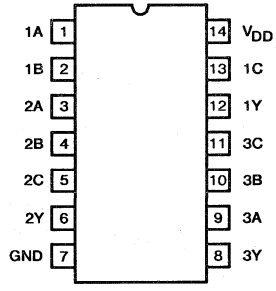
HCTS21MS
Dual 4-Input AND Gate

Type Features

- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

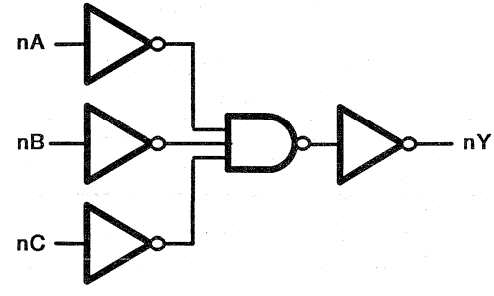
TRUTH TABLE

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	0	1	0
1	1	1	0

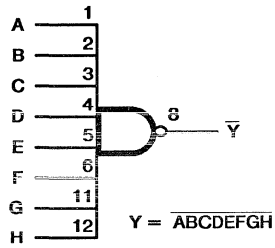
HCTS27MS
Triple 3-Input NOR Gate

Type Features

- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

HCTS30MS
8-Input NAND Gate

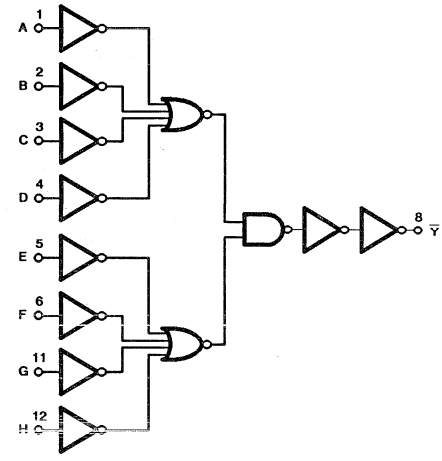
Type Features

- Radiation hardened to 200K or 1 MegaRADs (Si)
- Cosmic Ray Upset Immunity (typical 2 x 10^{-9} errors/bit-day)
- Latch-up free under transient radiation
- Transient upset > 10^{10} RADs/s 20ns pulse

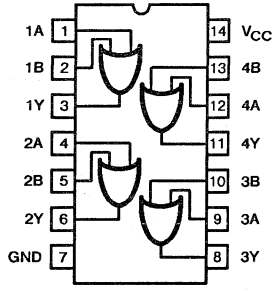
TRUTH TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	$\overline{Y}$
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level. L = LOW Voltage Level.



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

HCTS32MS
Quad 2-Input OR Gate

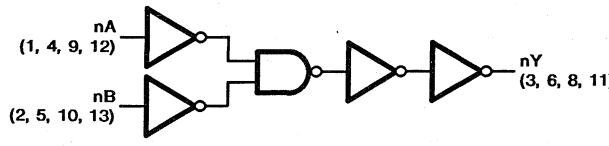
Type Features

- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

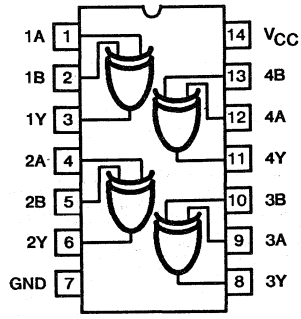
TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Voltage Level. L = LOW Voltage Level.



LOGIC DIAGRAM



TERMINAL ASSIGNMENT

HCTS86MS
Quad 2-Input Exclusive-OR Gate

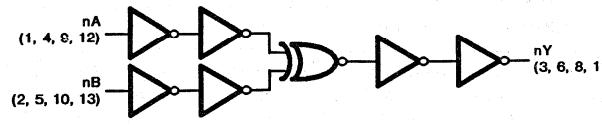
Type Features

- Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = +25°C
- Buffered inputs

TRUTH TABLE

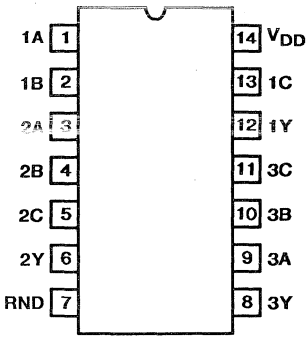
INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	L	L

H = HIGH Voltage Level. L = LOW Voltage Level.



LOGIC DIAGRAM

HCS10MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Triple 3-Input NAND Gate.

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs*

The HCS10MS is a triple 3-input NAND gate. The HCS10MS utilizes advanced CMOS/SOS technology to achieve high-speed operation similiar to LSTTL and high-speed CMOS while providing radiation-hardness. The HCS10MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs which are available.

The HCS10MS is presently supplied in a 14-lead weld-seal ceramic flatpack package (K suffix) or a 14-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8 max., V_{IH} = V_{DD}/2 min.
  CMOS Input Compatibility
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

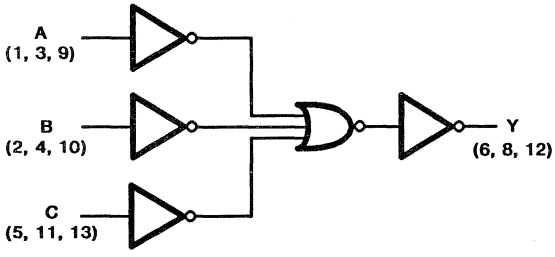


Figure 1 - Logic diagram.

TRUTH TABLE

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

File Number **2435**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, Output (I/O) = $-0.5V < V_O < V_{DD} + 0.5V$ ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	10	-	200	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC} - 0.4V$	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	$I_{OH} = -50\mu A$	V_{DD} -0.1	-	V_{DD} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 VDD	-	0.3 VDD	V
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	0.7 V_{DD}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}	-	±0.5	-	±5	µ
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Output Capacitance	C_{OUT}*	-	-	-	-	-	pF
Power Dissipation Capacitance	C_{PD}*	-	-	TBE	-	TBE	pF

* Guaranteed but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF

CHARACTERISTICS		V_{DD} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PHL}	4.5	-	18	-	20	ns
Input to Output	t_{PLH}	4.5	-	20	-	22	ns

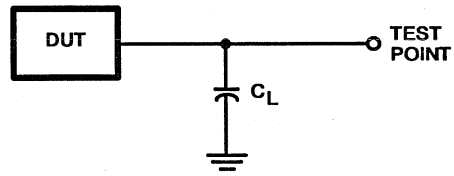


Figure 2 - Load circuit for T_{PZL}, T_{PLZ}.

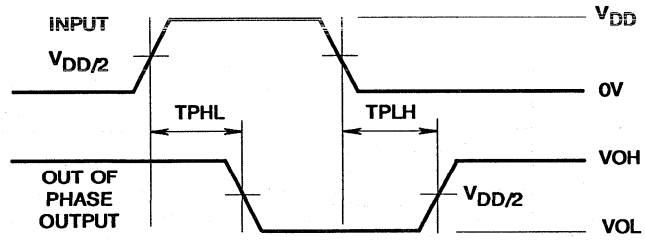


Figure 3 - Timing diagram

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of radiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0V or V_{DD}	-	0.2	-	1.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{DD} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{DD} -0.1	-	V_{DD} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{DD}	-	0.2 V_{DD}	V
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	0.7 V_{DD}	-	V
Input Leakage Current	I_{IL}	V_{IN} = 0V or V_{DD}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PHL}	4.5	-	20	-	25	ns
Input to Output	t_{PLH}	4.5	-	22	-	26	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS10MS	6, 8, 12,	1-5, 7, 9-11, 13	14	6, 8, 12,	7	1-5, 9-11, 13, 14
Dynamic Burn-In Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCS10MS	-	7	6, 8, 12,	14	1-5, 9-11, 13	-

NOTE: Each pin except 7 and 14 shall have a resistor of 10kΩ for static burn-in and 1kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{DD}	10μA	+3μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

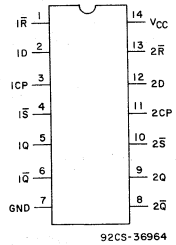
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
6, 8, 12,	7	1-5, 9-11, 13

NOTE: Each pin except 7 and 14 shall have a resistor of 680Ω - 47kΩ.

HCS74MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Dual-D Flip-Flop with Set and Reset. Positive Edge Trigger.

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2×10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 21ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs*

The HCS74MS dual D flip-flop with set and reset, positive edge triggered utilizes advanced CMOS/SOS technology to achieve high-speed operation similiar to LSTTL and high-speed CMOS while providing radiation-hardness. The HCS74MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs which are available.

The HCS74MS is supplied in a 14-lead weld-seal ceramic flatpack package (K suffix) or a 14-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types:*
  4.5 to 5.5V operation

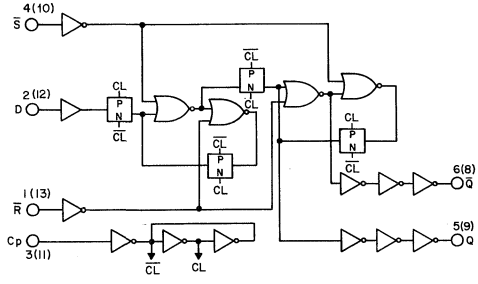


Figure 1 - Logic diagram.

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	⎍	H	H	L
H	H	⎍	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care

⎍ = Transition from Low to High Level

NOTES:

Q0 = the level of Q before the indicated input conditions were established.

*This configuration is non-stable, that is, it will not persist when set and reset inputs return to their inactive (High) level.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100° C ..... 500 mW
For T_A = +100 to +125° C ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

OPERATING CONDITIONS at T_A = -55° C to +125° C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25° C		-55° C/+125° C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	20	—	400	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	4.8	—	4	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-4.8	—	-4	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1	—	V_{CC}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.3 V_{CC}	—	0.3 V_{CC}	
Input High Voltage	V_{IH}	—	0.7 V_{CC}	—	0.7 V_{CC}	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±0.5	—	±5	μA
Input Capacitance	C_{IN}*	—	—	10	—	10	pF
Power Dissipation Capacitance	C_{PD}**	—	—	35	—	35	

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, (t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω)

CHARACTERISTIC		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C/+125°C MIN.	LIMITS -55°C/+125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	—	26	—	31	ns
CP to Q, $\overline{Q}$	t_{PHL}		—	27	—	32	
$\overline{S}$ to Q	t_{PLH}		—	26	—	31	
$\overline{S}$ to $\overline{Q}$	t_{PHL}		—	27	—	32	
$\overline{R}$ to Q	t_{PHL}		—	24	—	29	
$\overline{R}$ to $\overline{Q}$	t_{PLH}		—	15	—	30	

PREREQUISITE FOR SWITCHING:

CHARACTERISTIC		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C/+125°C MIN.	LIMITS -55°C/+125°C MAX.	UNITS
Data to CP Setup Time	t_{SU}	4.5	11	—	12	—	ns
Hold Time	t_H		3	—	3	—	
Removal Time, $\overline{R}$, $\overline{S}$ to CP	t_{REM}		5	—	6	—	
Pulse Width, $\overline{R}$, $\overline{S}$	t_W		14	—	16	—	
Pulse Width, CP	t_W		14	—	16	—	

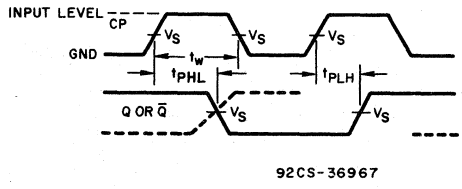


Fig. 2 - Clock pre-requisite and propagation delays.

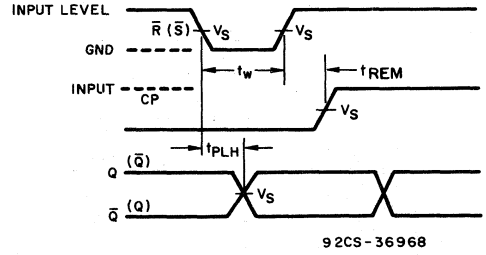


Fig. 3 - $\overline{Reset}$ or $\overline{Set}$ pre-requisite and propagation delays.

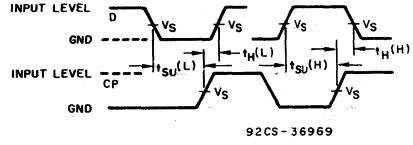


Fig. 4 - Data pre-requisite times.

	HCS
Input Level	**V_{CC}**
V_S	50% V_{CC}

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION† PERFORMANCE at T_A = +25°C

†Radiation measurements are made on 4 samples/wafer. The limits shown are for within 1 hour of radiating.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.4	—	1.5	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	4	—	4	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-4	—	-4	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1	—	V_{CC}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.3 V_{CC}	—	0.2 V_{CC}	
Input High Voltage	V_{IH}	—	0.7 V_{CC}	—	0.7 V_{CC}	—	
Input Leakage Current	I_{IL}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA

SWITCHING CHARACTERISTICS, t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS				UNITS
			200K Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	—	23	—	29	ns
CP to Q, $\overline{Q}$	t_{PHL}		—	27	—	34	
$\overline{S}$ to Q	t_{PLH}		—	17	—	22	
$\overline{S}$ to $\overline{Q}$	t_{PHL}		—	28	—	35	
$\overline{R}$ to Q	t_{PHL}		—	29	—	37	
$\overline{R}$ to $\overline{Q}$	t_{PLH}		—	25	—	32	

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCS74MS	5, 6, 8, 9	1, 2, 3, 4, 7, 10, 11, 12, 13	14	5, 6, 8, 9	7	1, 2, 3, 4 10, 12, 13, 14

Dynamic Burn-In Test-Circuit Connections						
TYPE	OPEN	GROUND	½ V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR	
					50 kHz	25 kHz
HCS74MS	—	7	5, 6, 8, 9	1, 4, 10, 13, 14	3, 11	2, 12

NOTE: Each pin except 7 and 14 shall have a resistor of 10kΩ for static burn-in and 1kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	20 μA	+6 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value

*All measurements will not exceed the absolute limit.

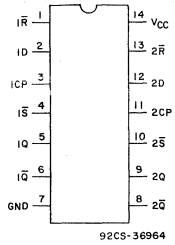
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
5, 6, 8, 9	7	1, 2, 3, 4 10, 11, 12, 13, 14

NOTE:
Each pin except 7, 14 shall have a resistor of 680 Ω - 47 kΩ.

HCTS74MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Dual-D Flip-Flop with Set and Reset. Positive Edge Trigger.

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 21ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs*

The HCTS74MS dual D flip-flop with set and reset, positive edge triggered utilizes advanced CMOS/SOS technology to achieve high-speed operation similiar to LSTTL and high-speed CMOS while providing radiation-hardness. The HCTS74MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs which are available.

The HCTS74MS is supplied in a 14-lead weld-seal ceramic flatpack package (K suffix) or a 14-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation

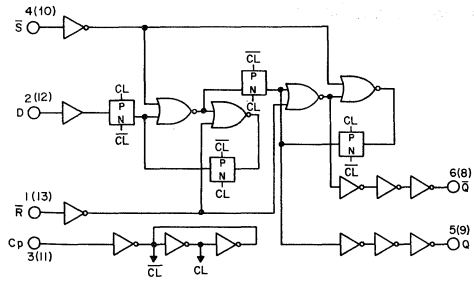


Figure 1 - Logic diagram.

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care

↑ = Transition from Low to High Level

NOTES:

Q0 = the level of Q before the indicated input conditions were established.

*This configuration is non-stable, that is, it will not persist when set and reset inputs return to their inactive (High) level.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C/+125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	20	—	400	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	4.8	—	4	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-4.8	—	-4	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1	—	V_{CC}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.8	—	0.8	
Input High Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±0.5	—	±5	μA
Input Capacitance	C_{IN}•	—	—	10	—	10	pF
Power Dissipation Capacitance	C_{PD}••	—	—	35	—	35	

• Guaranteed but not tested.
•• Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C/+125°C MIN.	LIMITS -55°C/+125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	—	27	—	31	ns
CP to Q, $\overline{Q}$	t_{PHL}		—	31	—	37	
$\overline{S}$ to Q	t_{PLH}		—	21	—	24	
$\overline{S}$ to $\overline{Q}$	t_{PHL}		—	33	—	38	
$\overline{R}$ to Q	t_{PHL}		—	35	—	40	
$\overline{R}$ to $\overline{Q}$	t_{PLH}		—	29	—	34	

PREREQUISITE FOR SWITCHING:

CHARACTERISTIC		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C/+125°C MIN.	LIMITS -55°C/+125°C MAX.	UNITS
Data to CP Setup Time	t_{SU}•	4.5	11	—	12	—	ns
Hold Time	t_H•		3	—	3	—	
Removal Time, $\overline{R}$, $\overline{S}$ to CP	t_{REM}•		5	—	6	—	
Pulse Width, $\overline{R}$, $\overline{S}$	t_W•		14	—	16	—	
Pulse Width, CP	t_W•		16	—	18	—	

• Guaranteed but not tested.

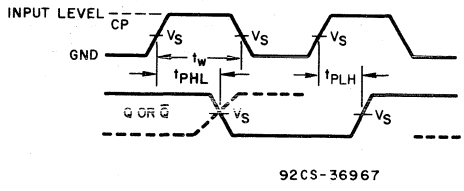


Fig. 2 - Clock pre-requisite and propagation delays.

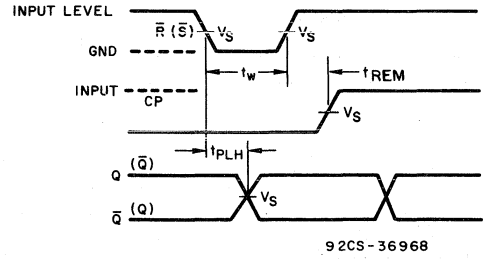


Fig. 3 - $\overline{Reset}$ or $\overline{Set}$ pre-requisite and propagation delays.

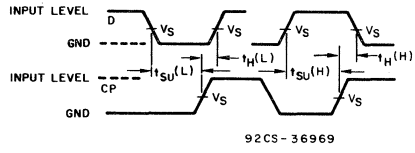


Fig. 4 - Data pre-requisite times.

	HCTS
Input Level	**3 V**
V_S	1.3 V

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20-ns pulse

POST-RADIATION† PERFORMANCE at T_A = +25°C

†Radiation measurements are made on 4 samples/wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.4	—	1.5	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	4	—	4	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-4	—	-4	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1	—	V_{CC}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.8	—	0.4	
Input High Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IL}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA

SWITCHING CHARACTERISTICS, (t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω)

CHARACTERISTIC		V_{CC} (V)	LIMITS				UNITS
			200K Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	—	31	—	39	ns
CP to Q, $\overline{Q}$	t_{PHL}		—	37	—	46	
$\overline{S}$ to Q	t_{PLH}		—	24	—	30	
$\overline{S}$ to $\overline{Q}$	t_{PHL}		—	38	—	48	
$\overline{R}$ to Q	t_{PHL}		—	40	—	50	
$\overline{R}$ to $\overline{Q}$	t_{PLH}		—	34	—	43	

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCTS74MS	5, 6, 8, 9	1, 2, 3, 4, 7, 10, 11, 12, 13	14	5, 6, 8, 9	7	1, 2, 3, 4 10, 11, 12, 13, 14
Dynamic Burn-in Test-Circuit Connections						
TYPE	OPEN	GROUND	½ V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR	
					50 kHz	25 kHz
HCTS74MS	—	7	5, 6, 8, 9	1, 4, 10, 13, 14	3, 11	2, 12

NOTE: Each pin except 7 and 14 shall have a resistor of 10kΩ for static burn-in and 1kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	20 μA	+6 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value

*All measurements will not exceed the absolute limit.

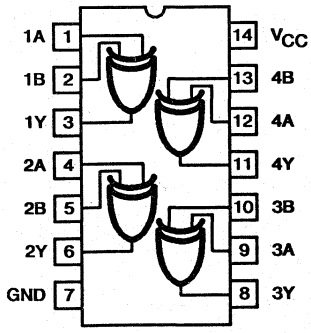
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
5, 6, 8, 9	7	1, 2, 3, 4 10, 11, 12, 13, 14

NOTE:
Each pin except 7, 14 shall have a resistor of 680 Ω - 47 kΩ.

HCTS86MS



FUNCTIONAL DIAGRAM

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Quad 2-Input Exclusive-OR Gate

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2×10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 21ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs*

The HCTS86MS is a quad 2-input Exclusive-OR gate. The HCTS86MS utlilizes advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and QMOS while providing radiation-hardness. The HCTS86MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs which are available.

The HCTS86MS is supplied in a 14-lead weld-seal ceramic flatpack package (K suffix) or a 14-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8 max., V_{IH} = V_{CC}/2 min.
  CMOS Input Compatibility
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

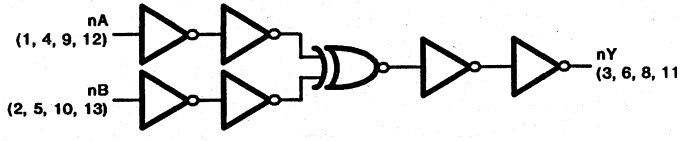


Figure 1 - Logic diagram.

TRUTH TABLE

INPUTS		OUTPUTS
nA	nB1	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = High Voltage Level
L = Low Voltage Level

12 LOGIC CIRCUITS

File Number 2249

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	10	-	200	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	V_{CC}/2	-	V_{CC}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissapation Capacitance	C_{PD}*	-	-	TBE	-	TBE	pF

* Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PHL}	4.5	-	18	-	20	ns
Input to Output	t_{PLH}	4.5	-	20	-	22	ns

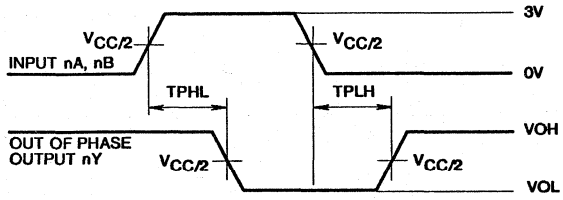


Figure 2 - Timing diagram.

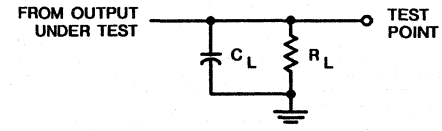


Figure 3 - Load circuit.

INHERENT PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.2	-	1.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.4	-	0.4	V
Input High Voltage	V_{IH}	-	V_{CC}/2	-	V_{CC}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PHL}	4.5	-	20	-	25	ns
Input to Output	t_{PLH}	4.5	-	22	-	26	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS86MS	3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	14	3, 6, 8, 11	7	1, 2, 4, 5, 7, 9, 10, 12, 13, 14

Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS86MS	-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTE: Each pin except 7 and 14 is connected to the test circuit through a resistor of 10kΩ for static burn-in and 1kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	10μA	+3μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

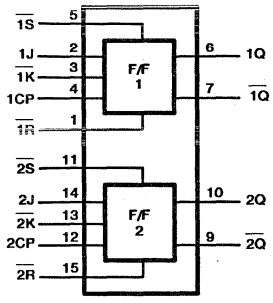
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
1, 4, 10, 13	7	1, 2, 4, 5, 7, 9, 10, 12, 13, 14

NOTE: Each pin except 7 and 14 is connected to the test circuit through a resistor of 680Ω - 47kΩ.

HCS109MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS, Dual J-$\overline{K}$ Flip-Flop

Aerospace Class S Screening

Radiation Features:
- *Radiation Hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

The HCS109 is a radiation-hardened dual J-$\overline{K}$ flip-flop with set and reset. The HCS109 utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation-hardened, high-speed, CMOS/SOS logic family with either TTL or CMOS input compatibility.

The HCS109 is supplied in a 16 lead weld seal ceramic flatpack package (K suffix) or a 16 lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types:*
  4.5 to 5.5V operation
  CMOS input logic compatibility
  V_{IL} = 0.3 V_{CC} max., V_{IH} = 0.7 V_{CC}
  CMOS input compatibility
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

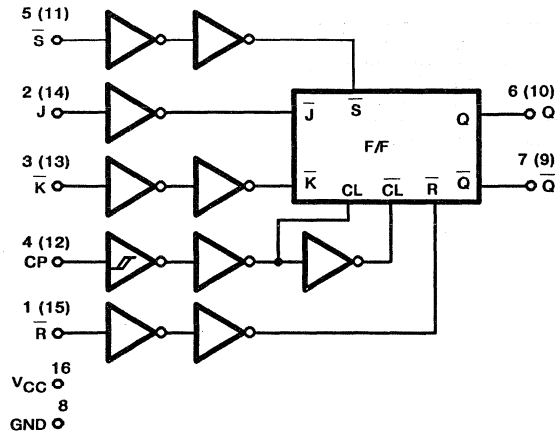


Figure 1 - Logic Diagram.

TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↓	H	L	TOGGLE	
H	H	↓	L	H	NO CHANGE	
H	H	↓	H	H	H	L
H	H	L	X	X	NO CHANGE	

*Unpredictable and unstable condition if both $\overline{S}$ and $\overline{R}$ go high simultaneously.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	20	-	400	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	27	-	37	pF

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay CP to Q, $\overline{Q}$	t_{PLH}	4.5	-	26	-	30	ns
	t_{PHL}	4.5	-	30	-	35	ns
Propagation Delay $\overline{S}$ to Q	t_{PLH}	4.5	-	19	-	23	ns
Propagation Delay $\overline{S}$ to $\overline{Q}$	t_{PHL}	4.5	-	31	-	33	ns
Propagation Delay $\overline{R}$ to Q	t_{PHL}	4.5	-	31	-	33	ns
Propagation Delay $\overline{R}$ to $\overline{Q}$	t_{PLH}	4.5	-	31	-	33	ns

PREREQUISITE FOR SWITCHING

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Setup Time, J, $\overline{K}$ to CP	t_{SU}*	4.5	16	-	18	-	ns
Hold Time, J, $\overline{K}$ to CP	t_H*	4.5	3	-	3	-	ns
Removal Time, $\overline{R}$, $\overline{S}$ to CP	t_{REM}*	4.5	16	-	18	-	ns
Pulse Width, $\overline{R}$, $\overline{S}$	t_W*	4.5	16	-	18	-	ns
Pulse Width, CP	t_W*	4.5	24	-	27	-	ns

* Guaranteed by not tested.

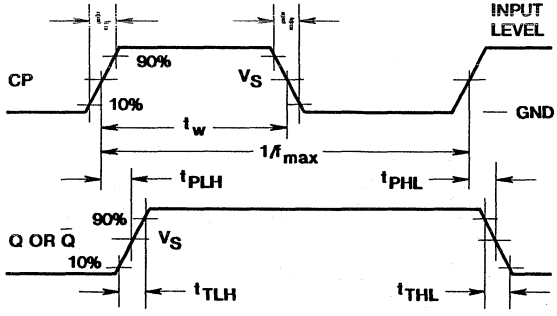


Figure 2 - Clock to output delays and clock pulse width.

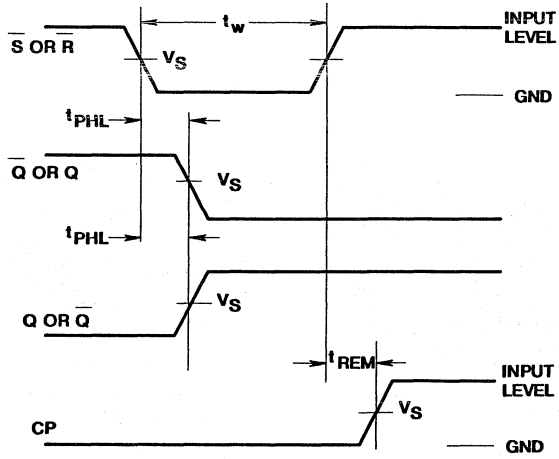


Figure 3 - $\overline{Reset}$ or $\overline{Set}$ prerequisite and propagation delays.

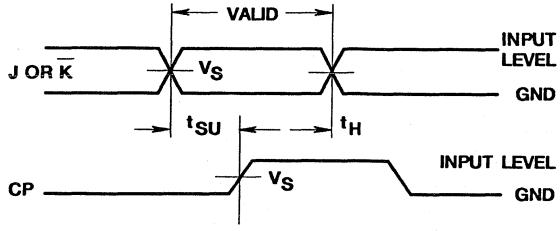


Figure 4 - Data set-up and hold times.

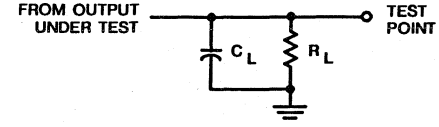


Figure 5 - Load Circuit.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.2 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	30	-	38	ns
CP to Q, $\overline{Q}$	t_{PHL}	4.5	-	35	-	44	ns
Propagation Delay $\overline{S}$ to Q	t_{PLH}	4.5	-	23	-	29	ns
Propagation Delay $\overline{S}$ to $\overline{Q}$	t_{PHL}	4.5	-	33	-	41	ns
Propagation Delay $\overline{R}$ to Q	t_{PHL}	4.5	-	33	-	41	ns
PropagationDelay $\overline{R}$ to $\overline{Q}$	t_{PLH}	4.5	-	33	-	41	ns

	HCS109MS
Input Level	V_{CC}
Switching Voltage, V_S	$V_{CC}/2$

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections

TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS109MS	6, 7, 9, 10	1, 2, 4, 5, 8, 11 12, 13, 14, 15	16	6, 7, 9, 10	8	1, 2, 3, 4, 5, 11, 12, 13, 14, 15, 16

Dynamic Burn-in Test-Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	OSCILLATOR	
					50kHz	25kHz
HCS109MS	-	8	6, 7, 9, 10	1, 2, 3, 5, 11, 13, 14, 15, 16	4, 12	-

NOTE: Each pin except V_{CC} and V_{SS} shall have a resistor of 10kΩ for static burn-in and 1kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	20μA	+6μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value
I_{OZL}	-1μA	-200nA
I_{OZH}	+1μA	+200nA

* All measurements will not exceed the absolute limit.

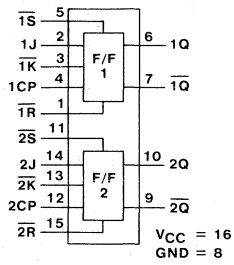
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
6, 7, 9, 10	8	1, 2, 3, 4, 5, 11, 12 13, 14, 15, 16

NOTE: Each pin except V_{CC} and V_{SS} shall have a resistor of 680Ω - 47kΩ.

HCTS109MS



FUNCTIONAL DIAGRAM

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Dual J-$\overline{K}$ Flip-Flop with Set and Reset. Positive Edge Trigger.

Aerospace Class S Screening

Radiation Features:
- *Radiation Hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 25ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs*

The HCTS109 dual J-$\overline{K}$ flip-flop with set and reset is positive edge triggered and utilizes advanced CMOS/SOS technology to achieve high-speed operation similiar to LSTTL and high-speed CMOS while providing radiation-hardness. The HCTS109 is a member of a familiy of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs which are available.

The HCTS109 is supplied in a 16 lead weld seal ceramic flatpack package (K suffix) or a 16 lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL input logic compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{CC}/2 min.
  CMOS input compatibility
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

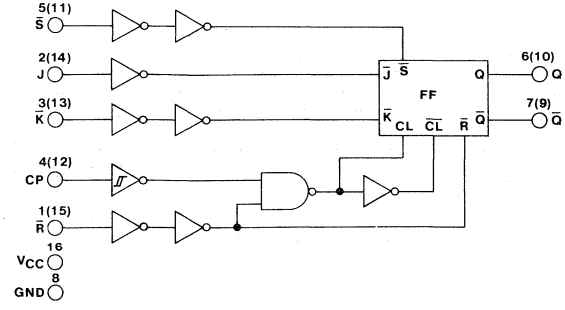


Figure 1 - Logic Diagram.

TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↓	H	L	TOGGLE	
H	H	↓	L	H	NO CHANGE	
H	H	↓	H	H	H	L
H	H	L	X	X	NO CHANGE	

*Unpredictable and unstable condition if both $\overline{S}$ and $\overline{R}$ go high simultaneously.

12 LOGIC CIRCUITS

File Number 2141

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE, (V_{CC}):
All voltage values referenced to the V_{SS} terminal ..... -0.5 V to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 V to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C ..... 500 mW
For T_A = +100°C to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package Temperature Range ..... 100 mW
OPERATING TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C

For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C/+125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	20	—	400	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	4.8	—	4.0	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4 V	-4.8	—	-4.0	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Input Low Voltage	V_{IL}	—	—	0.8	—	0.8	
Input High Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{CC}	—	±0.5	—	±5	μA
Input Capacitance	C_{IN} *	—	—	10	—	10	pF
Power Dissipation Capacitance	C_{PD} **	—	—	53	—	53	

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, t_r, t_f = 3 ns)

CHARACTERISTIC		V_{CC}	LIMITS				UNITS
			+25°C		-55°C/+125°C		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5 V	—	26	—	30	ns
CP to Q, $\overline{Q}$	t_{PHL}	4.5 V	—	30	—	35	
Propagation Delay $\overline{S}$ to Q	t_{PLH}	4.5 V	—	19	—	23	
Propagation Delay $\overline{S}$ to $\overline{Q}$	t_{PHL}	4.5 V	—	31	—	33	
Propagation Delay $\overline{R}$ to Q	t_{PHL}	4.5 V	—	31	—	33	
Propagation Delay $\overline{R}$ to $\overline{Q}$	t_{PLH}	4.5 V	—	31	—	33	

PREREQUISITE FOR SWITCHING:

CHARACTERISTIC		V_{CC}	LIMITS				UNITS
			+25°C		-55°C/+125°C		
			MIN.	MAX.	MIN.	MAX.	
Setup Time, J, $\overline{K}$ to CP	t_{SU}*	4.5 V	16	—	18	—	ns
Hold Time, J, $\overline{K}$ to CP	t_H*	4.5 V	3	—	3	—	
Removal Time, $\overline{R}$, $\overline{S}$ to CP	t_{REM}*	4.5 V	16	—	18	—	
Pulse Width, $\overline{R}$, $\overline{S}$	t_W*	4.5 V	16	—	18	—	
Pulse Width, CP	t_W*	4.5 V	24	—	27	—	

* Guaranteed but not tested.

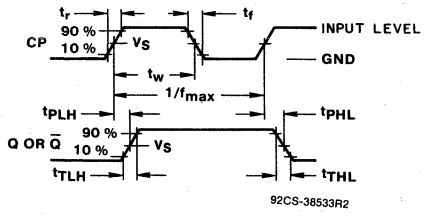


Fig. 2 - Clock to output delays and clock pulse width.

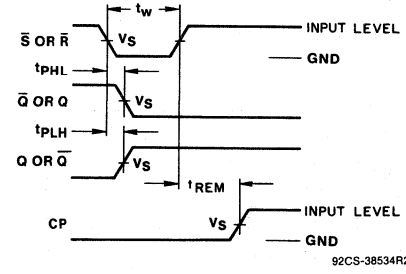


Fig. 3 - $\overline{Reset}$ or $\overline{Set}$ prerequisite and propagation delays.

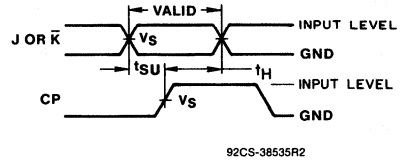


Fig. 4 - Data set-up and hold times.

	HCTS
Input Level	3 V
Switching Voltage, V_S	1.3 V

INHERENT PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ Rad(Si)/S
Transient Upset ..... $\geq 10^{10}$ Rad(Si)/S, 20 ns pulse

POST-RADIATION † PERFORMANCE at T_A = +25°C

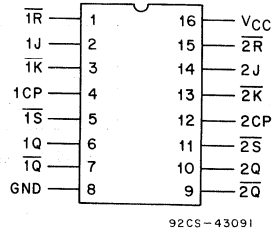
† Radiation measurements are made on 4 samples/wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k RADS (Si)		1M RADS (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.4	—	1.5	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	4.0	—	4.0	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4 V	-4.0	—	-4.0	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Input Low Voltage	V_{IL}	—	—	0.8	—	0.3	
Input High Voltage	V_{IH}	—	$V_{CC}/2$	—	$V_{CC}/2$	—	
Input Leakage Current	I_{IL}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA

SWITCHING CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, t_r, t_f = 3 ns)

CHARACTERISTIC		V_{CC}	LIMITS				UNITS
			200k RADS (Si)		1M RADS (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5 V	—	30	—	38	ns
CP to Q, $\overline{Q}$	t_{PHL}	4.5 V	—	35	—	44	
Propagation Delay $\overline{S}$ to Q	t_{PLH}	4.5 V	—	23	—	29	
Propagation Delay $\overline{S}$ to $\overline{Q}$	t_{PHL}	4.5 V	—	33	—	41	
Propagation Delay $\overline{R}$ to Q	t_{PHL}	4.5 V	—	33	—	41	
Propagation Delay $\overline{R}$ to $\overline{Q}$	t_{PLH}	4.5 V	—	33	—	41	



TERMINAL ASSIGNMENT

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCTS109MS	6, 7, 9, 10	1, 2, 3, 4, 5, 8, 11, 12, 13, 14, 15	16	6, 7, 9, 10	8	1, 2, 3, 4, 5, 11, 12, 13, 14, 15, 16

Dynamic Burn-In Test-Circuit Connections						
TYPE	OPEN	GROUND	1/2 V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR	
					50 kHz	25 kHz
HCTS109MS	—	8	6, 7, 9, 10	1, 2, 3, 5, 11, 13, 14, 15, 16	4, 12	—

NOTE: Each pin except 8 and 16 shall have a resistor of 10kΩ for static burn-in and 1kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT *	DELTA LIMIT
I_{CC}	20 μA	+6 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value

* All measurements will not exceed the absolute limit.

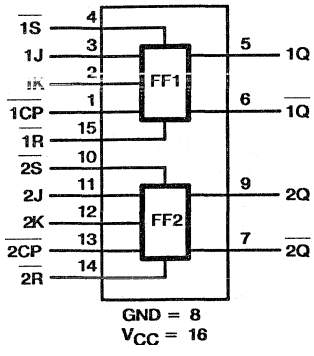
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
6, 7, 9, 10	8	1, 2, 3, 4, 5, 11, 12, 13, 14, 15, 16

Note: Each pin except 8, 16 shall have a resistor of 680 Ω - 47 kΩ.

HCTS112MS



FUNCTIONAL DIAGRAM

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Dual J-K Flip-Flop With Set and Reset. Negative Edge Trigger.

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 30ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs*

The HCTS112MS dual J-$\overline{K}$ flip-flop with set and reset is negative edge triggered. This device utilizes advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and QMOS while providing radiation hardness. The HCTS112MS is a member of a family of radiation-hardened, high speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs.

The HCTS112MS is presently supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) or a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard Outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8 max., V_{IH} = V_{CC}/2 min.
  CMOS Input Compatibility
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

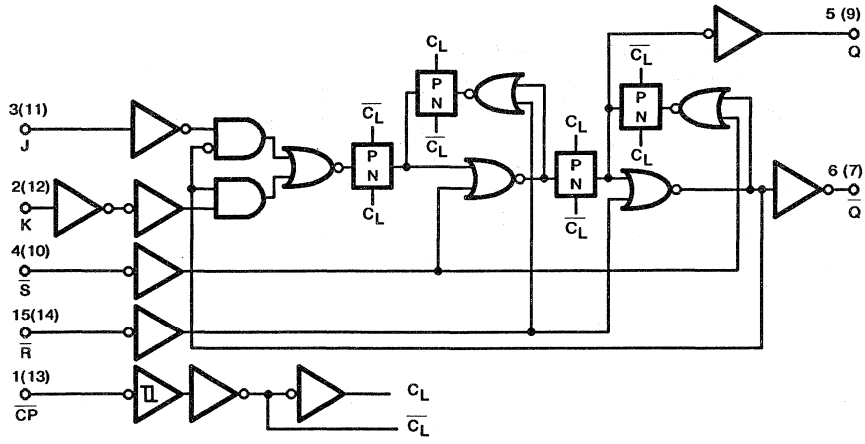


Figure 1 - Flip-flop logic diagram.

TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	L*
H	H	↓	L	L	No Change	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	No Change	

*Output states unpredictable if $\overline{S}$ and $\overline{R}$ go High simultaneously after both being low at the same time.

H = High Level (Steady State)

L = Low Level (Steady State)

X = Irrelevant

↓ = High-to-Low transition

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, Output (I/O) = $-0.5V < V_O < V_{DD} + 0.5V$ ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	20	-	400	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC} - 0.4V$	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	$V_{CC}/2$	-	$V_{CC}/2$	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µ
Input Capacitance	C_{IN}*	-	-	10	-	10	pF

* Guaranteed but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	34	-	38	ns
CP to Q, $\overline{Q}$	t_{PHL}	4.5	-	37	-	42	
$\overline{S}$ to Q	t_{PHL}	4.5	-	21	-	24	
$\overline{S}$ to $\overline{Q}$	t_{PHL}	4.5	-	35	-	41	
$\overline{R}$ to Q	t_{PHL}	4.5	-	33	-	38	
$\overline{R}$ to $\overline{Q}$	t_{PLH}	4.5	-	28	-	34	

PREREQUISITE FOR SWITCHING:

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Set-up Time, J, $\overline{K}$ to CP	t_{SU} •	4.5	14	-	16	-	ns
Hold Time, J, $\overline{K}$ to CP	t_H •	4.5	3	-	3	-	ns
Removal Time, $\overline{R}$, $\overline{S}$ to CP	t_{REM} •	4.5	18	-	20	-	ns
Pulse Width, $\overline{R}$, $\overline{S}$	t_W •	4.5	16	-	18	-	ns
Pulse Width, CP	tW •	4.5	14	-	16	-	ns

• Guaranteed but not tested.

	HCTS
Input Level	3V
Switching Voltage, V_S	1.3V

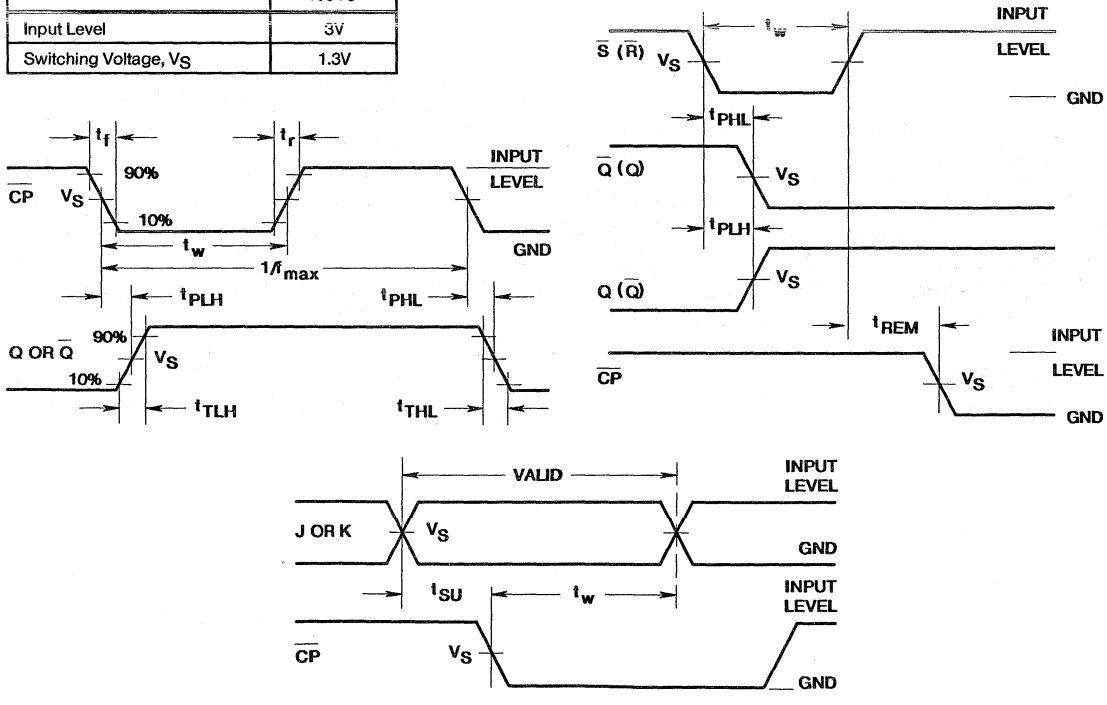


Figure 2 - Transition times, propagation delay times and setup and hold times.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

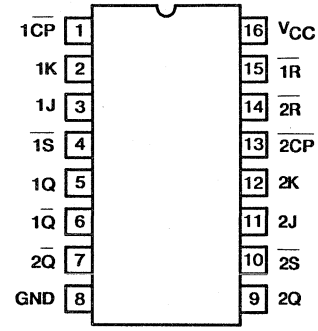
Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of radiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.4	-	1.5	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.4	V
Input High Voltage	V_{IH}	-	V_{CC}/2	-	V_{CC}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, RL = 500Ω

CHARACTERISTICS			V_{CC} (V)	LIMITS				UNITS
				200k Rads (Si)		1M Rads (Si)		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delay		t_{PLH}	4.5	-	38	-	48	ns
	CP to Q, $\overline{Q}$	t_{PHL}	4.5	-	42	-	53	
	$\overline{S}$ to Q	t_{PLH}	4.5	-	24	-	30	
	$\overline{S}$ to $\overline{Q}$	t_{PHL}	4.5	-	41	-	51	
	$\overline{R}$ to Q	t_{PHL}	4.5	-	38	-	48	
	$\overline{R}$ to $\overline{Q}$	t_{PLH}	4.5	-	34	-	43	



TERMINAL ASSIGNMENT

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS112MS	5-7, 9,	1-4, 8, 10-15	16	5-7, 9,	8	1-4, 10-16
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS112MS	-	8	5-7, 9,	2-4, 10-12, 14-16	1, 13	-

NOTE: Each pin except 8 and 16 shall have a resistor of 10kΩ for static burn-in and 1kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{DD}	20μA	+6μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

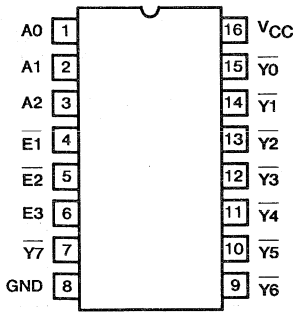
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
5-7, 9	8	1-4, 10-16

NOTE: Each pin except 8 and 16 shall have a resistor of 680Ω - 47kΩ.

HCS138MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Inverting 3-to-8 Line Decoder/Demultiplexer

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 23ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3 Enable inputs to simplify cascading*
- *Select one of eight data outputs (active low)*

The HCS138MS is a 3-to-8 Decoder/Demultiplexer with outputs active in the low state. This device utilizes advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and QMOS while providing radiation-hardness. The HCS138MS is a member of a family of radiation-hardened, high speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs.

The HCS138MS is presently supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) and in a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range): Bus-driver outputs - 15 LSTTL loads*
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types: LSTTL Input Logic Compatibility V_{IL} = 30%, V_{IH} = 70% of V_{CC}*

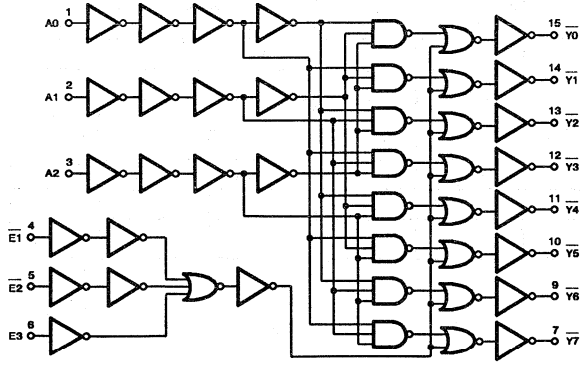


Figure 1 - Logic Diagram.

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level
L = Low Level
X = Don't Care

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-7.2	-	-6.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF

* Guaranteed but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay Address to Outputs	t_{PLH}	4.5	-	28	-	34	ns
	t_{PHL}	4.5	-	28	-	34	ns
Enable to Outputs	t_{PLH}	4.5	-	27	-	33	ns
	t_{PHL}	4.5	-	27	-	33	ns

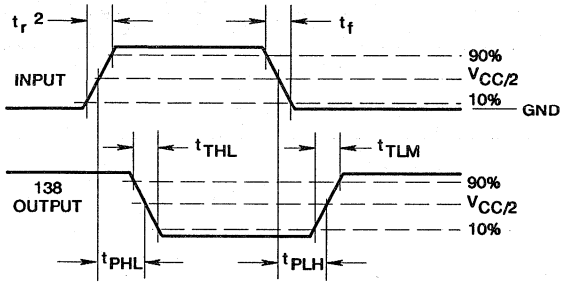


Figure 2 - Timing diagram.

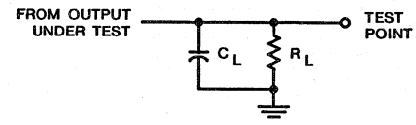


Figure 3 - Load circuit for t_{PLH}, t_{PHL}.

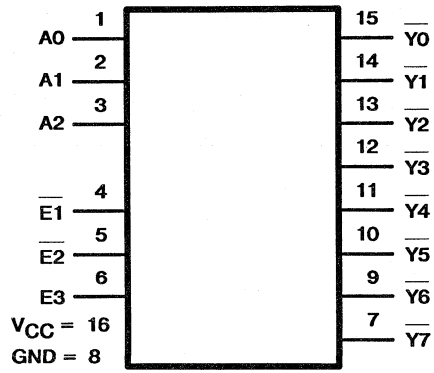


Figure 4 - Functional Diagram.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}		-	0.3 V_{CC}	-	0.2 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	34	-	41	ns
Address to Outputs	t_{PHL}	4.5	-	34	-	41	ns
Enable to Outputs	t_{PLH}	4.5	-	33	-	40	ns
	t_{PHL}	4.5	-	33	-	40	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS138MS	7, 9, 10, 11, 12, 13, 14, 15	1, 2, 3, 4, 5, 6, 8	16	7, 9, 10, 11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6, 16
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCS138MS	-	4, 5, 8	7, 9, 10, 11, 12, 13, 14, 15	3, 6, 16	2	1

NOTE: Each pin except 8 and 16 shall have a resistor of 10kΩ for static burn-in and 680Ω for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{DD}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

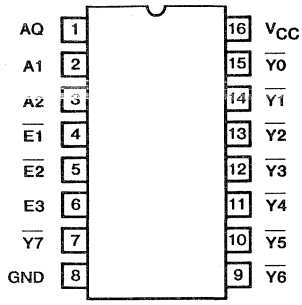
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
7, 9, 10, 11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6, 16

NOTE: Each pin except 10 and 20 shall have a resistor of 680Ω - 47kΩ.

HCTS138MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Inverting 3-to-8 Line Decoder/Demultiplexer

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 23ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3 Enable inputs to simplify cascading*
- *Select one of eight data outputs (active low)*

The HCTS138MS is a 3-to-8 Decoder/Demultiplexer with outputs active in the low state. This device utilizes advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and QMOS while providing radiation-hardness. The HCTS138MS is a member of a family of radiation-hardened, high speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs.

The HCTS138MS is presently supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) and in a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range): Bus-driver outputs - 15 LSTTL loads*
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5V to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{CC}/2 min.
  CMOS Input Compatibility
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

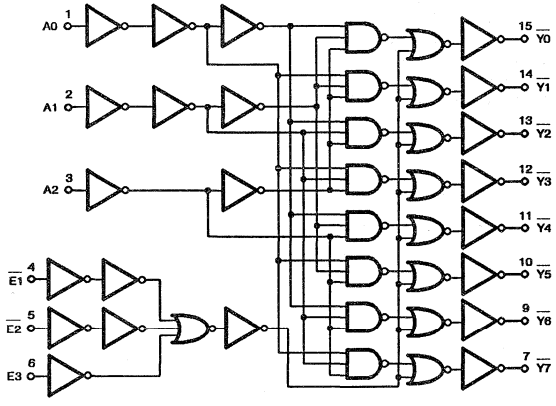


Figure 1 - Logic Diagram.

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level L = Low Level X = Don't Care

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-7.2	-	-6.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	V_{CC}/2	-	V_{CC}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	65	-	75	pF

* Guaranteed but not tested.
* Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay Address to Outputs	t_{PLH}	4.5	-	25	-	30	ns
	t_{PHL}	4.5	-	28	-	39	ns
Enable to Outputs	t_{PLH}	4.5	-	26	-	31	ns
	t_{PHL}	4.5	-	26	-	34	ns

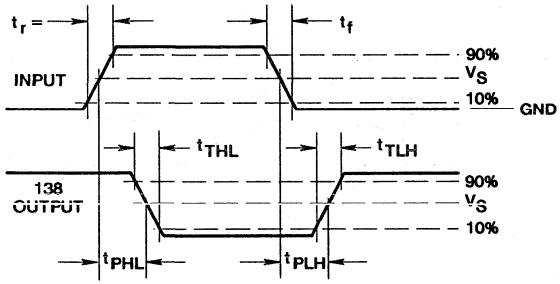


Figure 2 - Timing diagram.

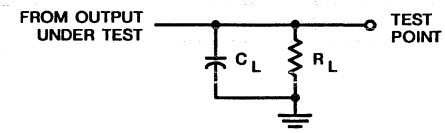


Figure 3 - Load circuit for t_{PLH}, t_{PHL}.

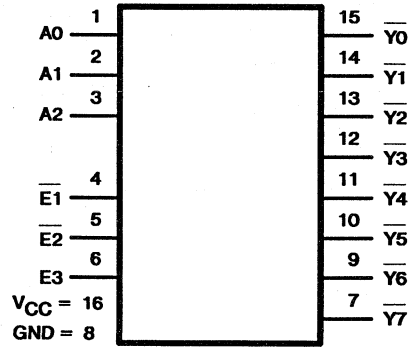


Figure 4 - Functional Diagram.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.3	V
Input High Voltage	V_{IH}	-	$V_{CC}/2$	-	$V_{CC}/2$	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	30	-	38	ns
Address to Outputs	t_{PHL}	4.5	-	39	-	49	ns
Enable to Outputs	t_{PLH}	4.5	-	31	-	39	ns
	t_{PHL}	4.5	-	34	-	43	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS138MS	7, 9, 10, 11, 12, 13, 14, 15	1, 2, 3, 4, 5, 6, 8	16	7, 9, 10, 11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6, 16
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS138MS	-	4, 5, 8	7, 9, 10, 11, 12, 13, 14, 15	3, 6, 16	2	1

NOTE: Each pin except 8 and 16 shall have a resistor of 10kΩ for static burn-in and 680kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{DD}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

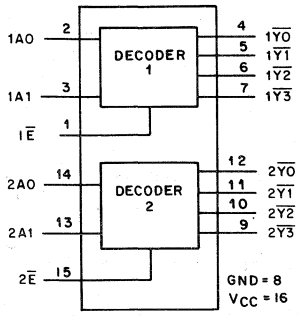
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
7, 9, 10, 11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6, 16

NOTE: Each pin except 10 and 20 shall have a resistor of 680Ω - 47kΩ.

HCTS139MS



FUNCTIONAL DIAGRAM

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Dual 2-to-4 Line Decoder/Demultiplexer

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Multifunction Capability: Binary to 1 of 4 Decoders or 1-to-4 Line Demultiplexer*
- *Typical propagation delay = 21ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Active low mutually exclusive outputs*

The HCTS139MS Dual 2-to-4 Line Decoder/Demultiplexer utilizes advance CMOS/SOS technology to achieve high-speed operation similiar to LSTTL and QMOS while providing radiation-hardness. The HCTS139MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs.

The HCTS139MS is presently supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) or a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range): Bus driver outputs - 15 LSTTL loads*
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  - *4.5 to 5.5V operation*
  - *LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 max., V_{IH} = V_{DD}/2 min.*
  - *CMOS Input Current Levels*
    - *$I_I \leq 5\mu A$ @ V_{OL}, V_{OH}*

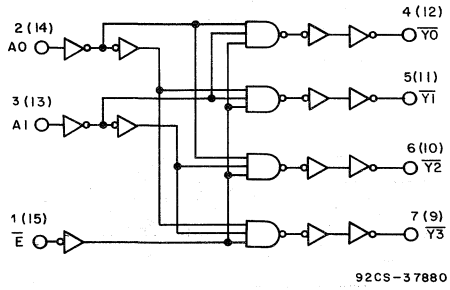


Figure 1 - Logic diagram.

TRUTH TABLE

INPUTS ENABLE SELECT			OUTPUTS			
$\overline{E}$	A1	A0	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

Logic 1 = High
Logic 0 = Low
X = Don't Care

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100° C ..... 500 mW
For T_A = +100 to +125° C ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

OPERATING CONDITIONS at T_A = -55° C to +125° C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V

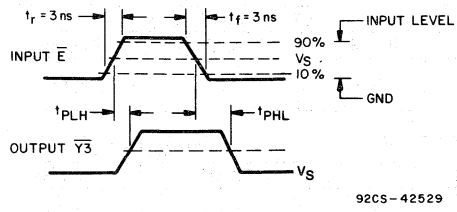
STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

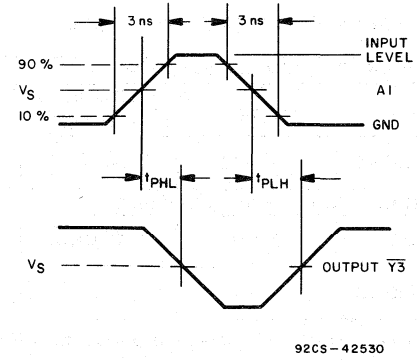
CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25° C		-55° C/+125° C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	40	—	750	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	7.2	—	6	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-7.2	—	-6	—	
Low-Level Output Voltage	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Low-Level Input Voltage	V_{IL}	—	—	0.8	—	0.8	
High-Level Input Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±0.5	—	±5	μA
Input Capacitance	C_{IN}*	—	—	10	—	10	pF
Power Dissipation Capacitance	C_{PD}**	—	—	50	—	60	

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

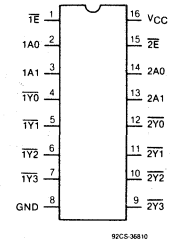
SWITCHING CHARACTERISTICS (t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω)

CHARACTERISTIC		V_{CC} (V)	LIMITS				UNITS
			+25° C		-55° C/+125° C		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	—	24	—	27	ns
A0,A1 to Outputs	t_{PHL}						
$\overline{E}$ to Outputs	t_{PLH}, t_{PHL}		—	24	—	27	





Propagation delay times.



TERMINAL ASSIGNMENT

INHERENT PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20-ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rad (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.75	—	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	6	—	5	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-6	—	-5	—	
Low-Level Output Voltage	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Low-Level Input Voltage	V_{IL}	—	—	0.8	—	0.3	
High-Level Input Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA

SWITCHING CHARACTERISTICS (t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω)

CHARACTERISTIC		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rad (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	—	27	—	34	ns
A0,A1 to Outputs	t_{PHL}						
$\overline{E}$ to Outputs	t_{PLH}, t_{PHL}		—	27	—	34	

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCTS139MS	4-7,9-12	1-3,8,13-15	16	4-7,9-12	8	1-3,13-16
Dynamic Burn-In Test-Circuit Connections						
TYPE	OPEN	GROUND	½ V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR	
					50 kHz	25 kHz
HCTS139MS	—	1, 8, 15	4-7,9-12	16	2,14	3,13

NOTE: Each pin except 8 and 16 shall have a resistor of 10kΩ for static burn-in and 680kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40 μA	+12 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value

*All measurements will not exceed the absolute limit.

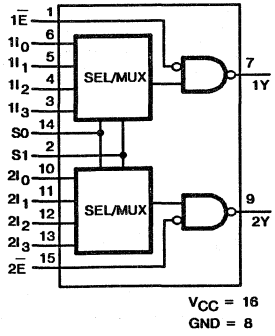
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
4-7,9-12	8	1-3,3-16

NOTE:
Each pin except 8 and 16 shall have a resistor of 680 Ω - 47 kΩ.

HCTS153MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Dual 4-Input Multiplexer

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 20ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs and outputs*
- *Separate enable inputs*
- *Common select inputs*

The HCTS153MS dual 4-input multiplexer utilizes advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and QMOS while providing radiation-hardness. The HCTS153MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs.

The HCTS153MS is presently supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) and in a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus-driver outputs - 15 LSTTL loads
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL input logic compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{DD}/2 min.
  CMOS input compatibility
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

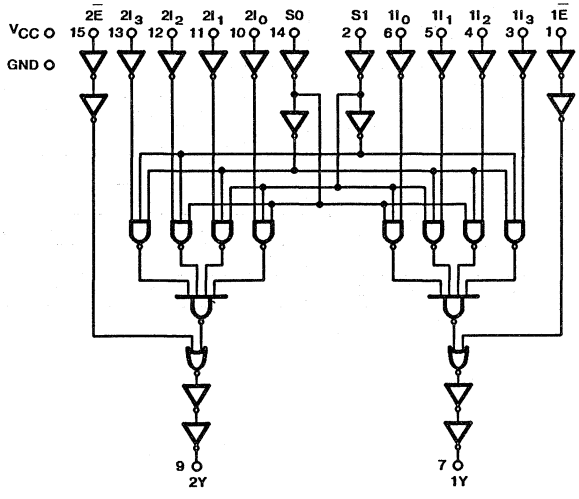


Figure 1 - Logic Diagram.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				ENABLE	OUTPUT
S_1	S_0	I_0	I_1	I_2	I_3	E	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = High Voltage Level
L = Low Voltage Level
X = Immaterial

File Number **2463**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

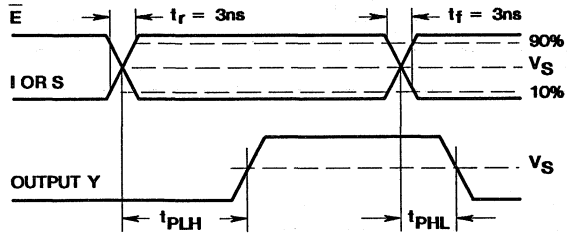
STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	V_{CC}/2	-	V_{CC}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissapation Capacitance	C_{PD}**	-	-	50	-	60	pF

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	20	-	23	ns
Input to Data	t_{PHL}	4.5	-	30	-	34	ns
Propagation Delay	t_{PLH}	4.5	-	28	-	32	ns
Select to Data	t_{PHL}	4.5	-	39	-	46	ns
Propagation Delay	t_{PLH}	4.5	-	19	-	22	ns
Enable to Data	t_{PHL}	4.5	-	17	-	19	ns



	HCTS
Input Level	3V
Switching Voltage, V_S	1.3V

Figure 2 - Transition and propagation delay times.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.3	V
Input High Voltage	V_{IH}	-	$V_{CC}/2$	-	$V_{CC}/2$	-	V
Input Leakage Current	I_{IL}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	23	-	29	ns
Input to Data	t_{PHL}	4.5	-	34	-	43	ns
Propagation Delay	t_{PLH}	4.5	-	32	-	40	ns
Select to Data	t_{PHL}	4.5	-	46	-	58	ns
Propagation Delay	t_{PLH}	4.5	-	22	-	28	ns
Enable to Data	t_{PHL}	4.5	-	19	-	24	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS153MS	7, 9	1 - 6, 8, 10 - 15	16	7, 9	8	1 - 6, 10 - 16
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS153MS	-	1, 3, 5, 8, 11, 13, 15	7, 9	4, 6, 10, 12, 16	14	2

NOTE: Each pin except 8 and 16 shall have a resistor of 10kΩ for static burn-in and 1kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT	DELTA LIMIT
I_{DD}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

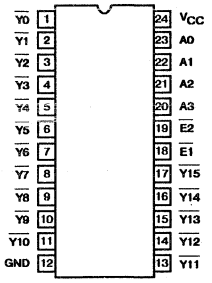
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
7, 9	8	1, 2, 3, 4, 5, 6, 10, 11, 12, 13, 14, 15, 16

NOTE: Each pin except 8 and 16 shall have a resistor of 680Ω - 47kΩ.

HCS154MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS 4-to-6 Line Decoder/Demultiplexer

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

The HCS154MS is a radiation-hardened 4-to-6 line decoder/demultiplexer with two enable inputs. A high on either enable input forces the output to a high state. The demultiplexer function is performed by using the four input lines A0 to A3 to select the desired output states.

The HCS154MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS logic family with either TTL or CMOS input compatibility.

The HCS154MS is supplied in a 24-lead weld-seal flatpack package (K suffix) or a dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus-driver outputs - 15 LSTTL loads
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types:*
  4.5V to 5.5V operation
  CMOS Input Logic Compatibility
  V_{IL} = 0.3V_{CC} max., V_{IH} = 0.7V_{CC} min.
  CMOS Input Current Levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

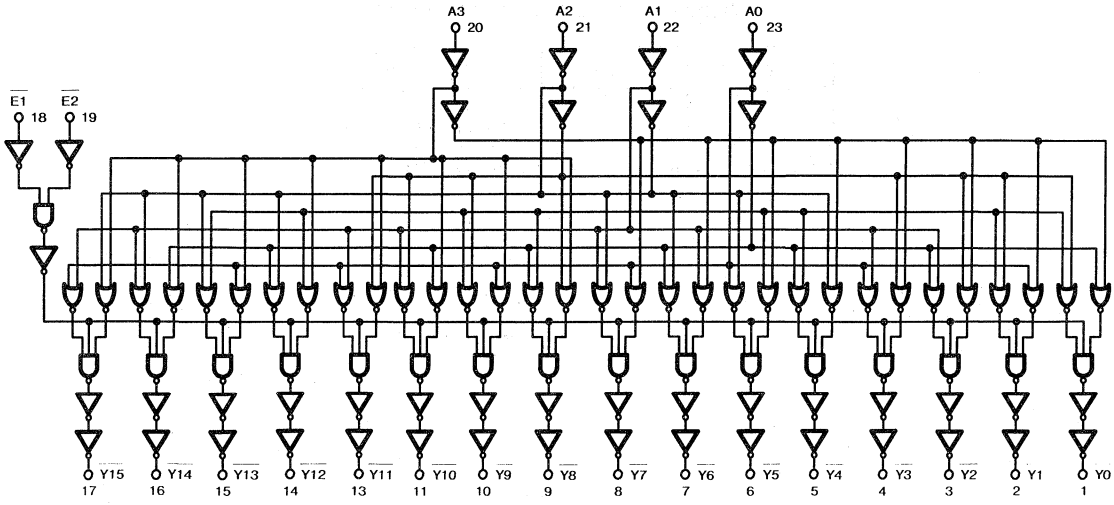


Figure 1 - Logic Diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	42	-	42	pF

* Guaranteed but not tested.
** Typical value. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Address to Output	t_{PLH}	4.5	-	29	-	34	ns
	t_{PHL}	4.5	-	27	-	31	ns
Enable to Output		4.5	-	27	-	27	ns

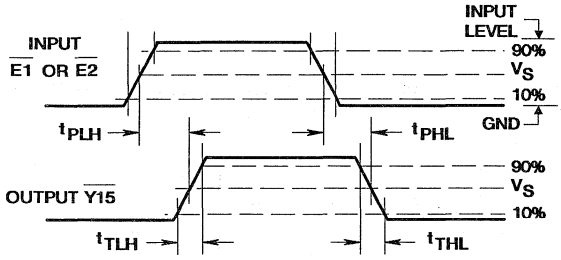


Figure 2 - Timing diagram.

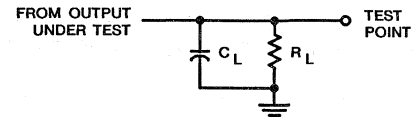


Figure 3 - Load circuit for prop delay.

Input Level	V_{CC}
Switching Voltage, V_S	$V_{CC}/2$

TRUTH TABLE

INPUTS						OUTPUTS														
$\overline{E1}$	$\overline{E2}$	A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level L = Low Level X = Immaterial

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.12 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Address to Output	t_{PLH}	4.5	-	34	-	43	ns
Address to Output	t_{PHL}	4.5	-	31	-	39	ns
Enable to Output		4.5	-	27	-	34	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS154MS	1-11, 13-17	12, 18-23	24	1-11	12	18-24
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCS154MS	-	12, 18-21	1-11, 13-17	24	23	22

NOTE: Each pin except V_{CC} and Ground shall have a resistor (10k ± -5% for static and 1k ± 5% for dynamic).

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

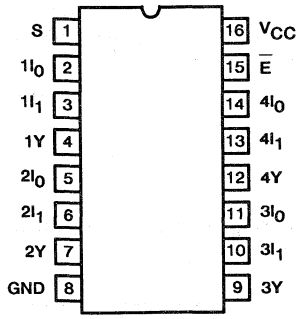
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
ii	initial Electrical Tests	interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
1-11, 13-17	12	18-23, 24

NOTE: Each pin except V_{CC} and Ground will have a resistor of 47kΩ.

HCTS157MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Quad 2-Input Multiplexer

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 20ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs*

The HCTS157MS is a quad 2 input multiplexer. The HCTS157 utilizes advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and QMOS while providing radiation hardness. The HCTS157MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL- or CMOS-compatible inputs which are available.

The HCTS157MS is presently supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) and in a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus-driver outputs - 15 LSTTL loads
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL input logic compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{DD}/2 min.
  CMOS input current levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

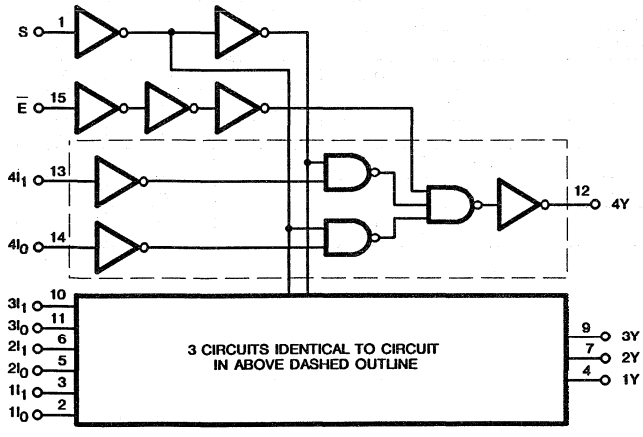


Figure 1 - Logic Diagram.

TRUTH TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUT
E	S	I_0	I_1	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

12 LOGIC CIRCUITS

File Number **2464**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0V or V_{DD}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{DD} -0.4V	-7.2	-	-6.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{DD} -0.1	-	V_{DD} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	V_{DD}/2	-	V_{DD}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}	-	±0.5	-	±7	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF

* Guaranteed but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF

CHARACTERISTICS		V_{DD} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PHL}	4.5	-	26	-	30	ns
Data to Output	t_{PLH}	4.5	-	20	-	24	ns
Propagation Delay	t_{PHL}	4.5	-	22	-	25	ns
Enable to Output	t_{PLH}	4.5	-	22	-	25	ns
Propagation Delay	t_{PHL}	4.5	-	31	-	37	ns
Select to Output	t_{PLH}	4.5	-	25	-	29	ns

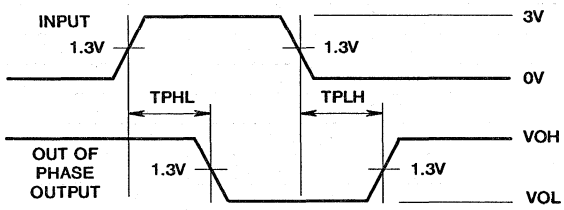


Figure 2 - Timing diagram.

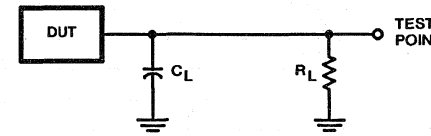


Figure 3 - Load Circuit.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of radiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0V or V_{DD}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{DD} -0.1	-	V_{DD} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.3	V
Input High Voltage	V_{IH}	-	V_{DD}/2	-	V_{DD}/2	-	V
Input Leakage Current	I_{IL}	V_{IN} = 0V or V_{DD}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF

CHARACTERISTICS		V_{DD} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PHL}	4.5	-	30	-	38	ns
Data to Output	t_{PLH}	4.5	-	24	-	30	ns
Propagation Delay	t_{PHL}	4.5	-	25	-	31	ns
Enable to Output	t_{PLH}	4.5	-	25	-	31	ns
Propagation Delay	t_{PHL}	4.5	-	37	-	47	ns
Select to Output	t_{PLH}	4.5	-	29	-	36	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS157MS	4, 7, 9, 12	1, 2, 3, 4, 5, 6, 8, 10, 11, 13, 14, 15	16	4, 7, 9, 12	8	1, 2, 3, 4, 5, 6, 10, 11, 13, 14, 15
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS157MS	-	8, 15	4, 7, 9, 12	16	2, 3, 5, 6, 10 11, 13, 14	1

NOTE: Each pin except 8 and 16 shall have a resistor of 10k ±5% for and 1k ±5% for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT	DELTA LIMIT
I_{DD}	40µA	+12µA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

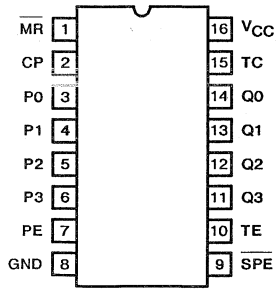
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
4, 7, 9, 12	8	1, 2, 3, 4, 5, 6, 7, 10, 11, 13, 14, 15, 16

NOTE: Each pin except 8 and 16 shall have a resistor of 680Ω - 47kΩ.

HCTS160MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Synchronous Counter
BCD Decade Counter, Asynchronous Reset

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay (CP - Qn) = 18ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Synchronous counting and loading*
- *Asynchronous reset*
- *Look-ahead carry for high speed counting*
- *Two count enable inputs for n-bit cascading*

The HCTS160MS is a high speed presettable BCD decade synchronous counter that features an asynchronous reset and look-ahead carry logic. Counting and parallel presetting are accomplished synchronously with the low-to-high transition of the clock. A low level on the synchronous parallel enable input, $\overline{SPE}$, disables counting and allows data at the preset inputs, P0 - P3, to be loaded into the counter. The counter is reset by a low on the master reset input, $\overline{MR}$. Two count enables, PE and TE, are provided for n-bit cascading. TE also controls the terminal count output, TC. The terminal count output indicates a maximum count for one clock pulse and is used to enable the next cascaded stage to count.

The HCTS160MS is presently supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) or a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8 max., V_{IH} = V_{DD}/2 min.
  CMOS Input Current Level
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

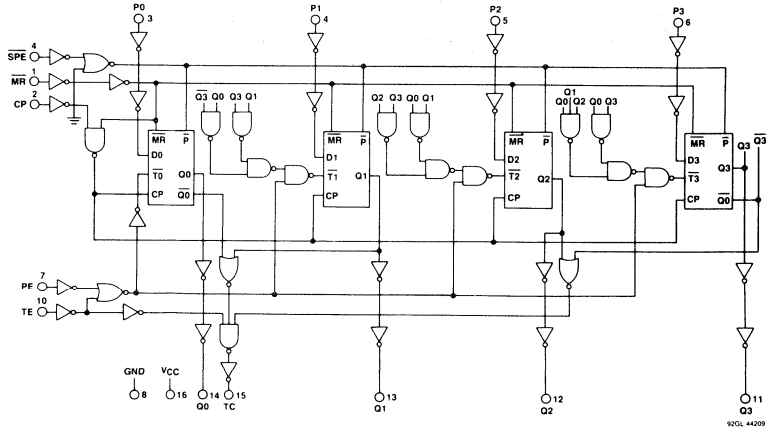


Figure 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

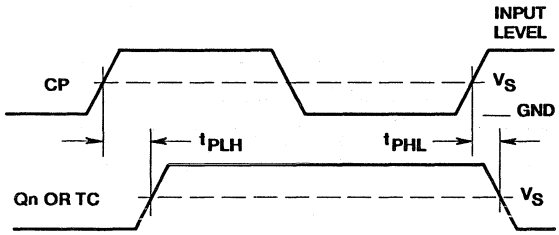
STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0V or V_{DD}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{DD} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{DD} -0.1	-	V_{DD} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	V_{DD}/2	-	V_{DD}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	TBE	-	TBE	pF

*Guaranteed but not tested.
**Typical Value. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	23	-	26	ns
CP to Qn	t_{PHL}	4.5	-	26	-	30	ns
CP to TC	t_{PLH}	4.5	-	24	-	28	ns
	t_{PHL}	4.5	-	28	-	32	ns
TE to TC	t_{PLH}	4.5	-	18	-	20	ns
	t_{PHL}	4.5	-	27	-	29	ns
MR to Qn, TC	t_{PHL}	4.5	-	46	-	51	ns
	t_{PHL}						



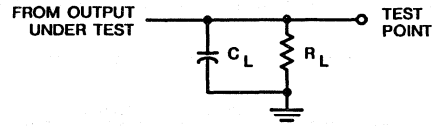


Figure 3 - Load Circuit.

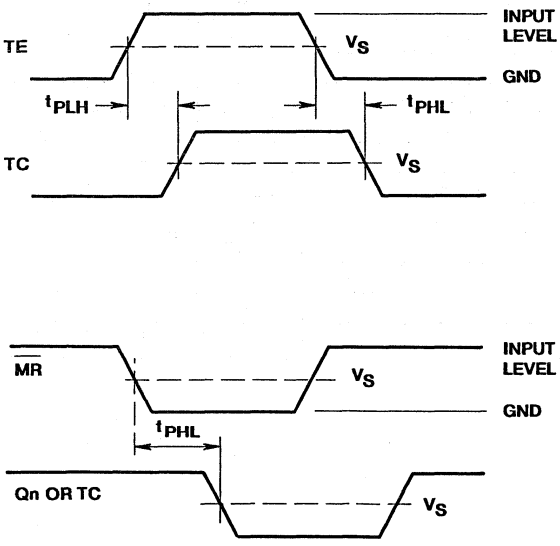
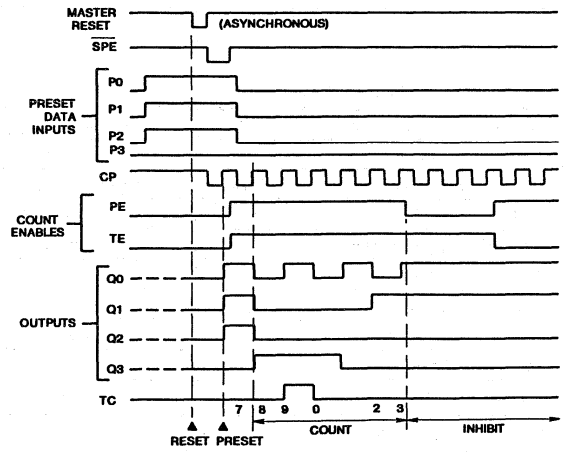


Figure 2 - Timing Waveforms.



Sequence illustrated in waveforms
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, zero, one and two.
4. Inhibit.

Figure 4 - Timing Diagram.

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	Pn	Qn	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	⎍	X	X	l	l	L	L
	H	⎍	X	X	l	h	H	(a)
Count	H	⎍	h	h	h(c)	X	count	(a)
Inhibit	H	X	l(b)	X	h(c)	X	qn	(a)
	H	X	X	l(b)	h(c)	X	qn	L

H = High Voltage (Steady State)
L = Low Voltage (Steady State)
h = High Voltage level one setup time prior to the Low-to-High clock transition.
l = Low Voltage level one setup time prior to the Low-to-High clock transition.
X = Don't care.
q = Lower-case letters indicate the state of the referenced output prior to the Low-to-High clock transition.
⎍ = Low-to-High clock transition.

NOTES:

(a) The TC output is High when TE is High and the counter is at Terminal Count (HHHH).

(b) The High-to-Low transition of PE or TE should only occur while CP is High for conventional operation.

(c) The Low-to-High transition of SPE should only occur while CP is High for conventional operation.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, $V_{DD} = 5V \pm 10\%$

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0V or V_{DD}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{DD}$ -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50μA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{DD} -0.1	-	V_{DD} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.3	V
Input High Voltage	V_{IH}	-	$V_{DD}/2$	-	$V_{DD}/2$	-	V
Input Leakage Current	I_{IL}	V_{IN} = 0V or V_{DD}	-	±5	-	±5	μA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS			V_{DD} (V)	LIMITS				UNITS
				200k Rads (Si)		1M Rads (Si)		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delay		t_{PLH}	4.5	-	26	-	33	ns
	CP to Qn	t_{PHL}	4.5	-	30	-	38	ns
	CP to TC	t_{PLH}	4.5	-	28	-	35	ns
		t_{PHL}	4.5	-	32	-	40	ns
	TE to TC	t_{PLH}	4.5	-	20	-	25	ns
		t_{PHL}	4.5	-	29	-	37	ns
	MR to Qn	tPHL	4.5	-	51	-	64	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS160MS	11, 12, 13, 14, 15	1, 2, 3, 4, 5, 6, 7, 8, 9, 10	16	11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6, 7, 9, 10, 16

Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS160MS	-	4, 6, 8	11, 12, 13, 13, 14, 15	1, 3, 5, 7, 9, 10, 16	2	-

NOTE: Each pin except 7 and 14 shall have a resistor of 10kΩ ±5% for static and 1kΩ ±5% for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{DD}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
ii	Initial Electrical Tests	Interim Electrical Tests II
iii	Initial Electrical Tests	Interim Electrical Tests III

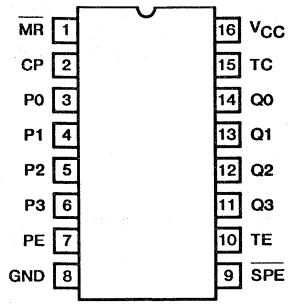
TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6, 7, 9, 10, 16

NOTE: Each pin except 7 and 14 shall have a resistor of 680Ω - 47kΩ.

HCS161MS

Advance Information



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Presettable Counter 4-Bit Binary Counter, Asynchronous Reset

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2×10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 18ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Synchronous counting and loading*
- *Asynchronous reset*
- *Look-ahead carry for high speed counting*
- *Two count enable inputs for n-bit cascading*

The HCS161MS high-reliability high-speed presettable four-bit binary synchronous counter features asynchronous reset and look-ahead carry logic. The HCTS161 has an active-low master reset to zero, $\overline{MR}$. A low level at the synchronous parallel enable, $\overline{SPE}$, disables counting and allows data at the preset inputs (P0 - P3) to load the counter. The data is latched to the outputs on the positive edge of the clock input, CP. The HCTS161 has two count enable pins, PE and TE. TE also controls the terminal count output, TC. The terminal count output indicates a maximum count for one clock pulse and is used to enable the next cascaded stage to count.

This device uses advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and HC/HCT while providing radiation hardness. The HCS161MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL- or CMOS-compatible inputs.

The HCS161MS is supplied in a 16-lead ceramic flatpack package (K suffix) or a 16-lead dual-in-line weld-seal ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to TTL logic ICs*
- *HCS types:*
  4.5 to 5.5V operation
  CMOS LSTTL Input Logic Compatibility
  V_{IL} = 0.3 V_{CC} max., V_{IH} = 0.7 V_{CC} min.
  CMOS Input Current Levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

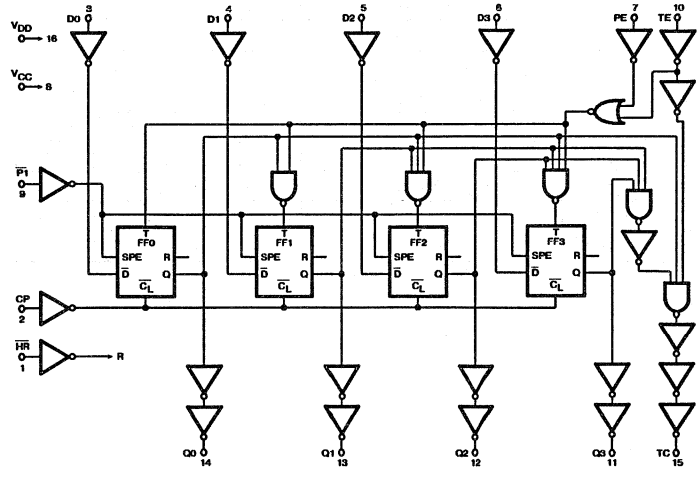


Fig. 1 - Logic Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE INPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	36	-	56	pF

* Guaranteed but not tested.
** Typical value. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	33	-	38	ns
CP to Qn	t_{PHL}	4.5	-	34	-	39	ns
CP to TC	t_{PHL}	4.5	-	35	-	40	ns
	t_{PHL}	4.5	-	37	-	42	ns
TE to TC	t_{PLH}	4.5	-	23	-	26	ns
	t_{PHL}	4.5	-	23	-	26	ns
$\overline{MR}$ to Qn	t_{PHL}	4.5	-	39	-	44	ns
$\overline{MR}$ to TC	t_{PHL}	4.5	-	44	-	50	ns

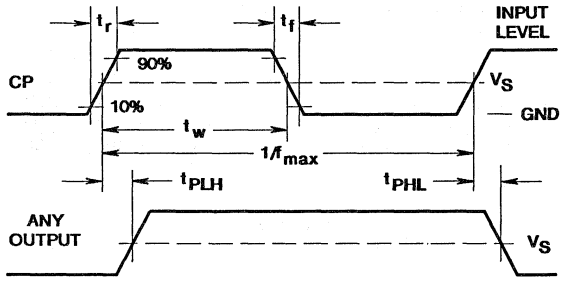


Fig. 2 - Timing waveforms

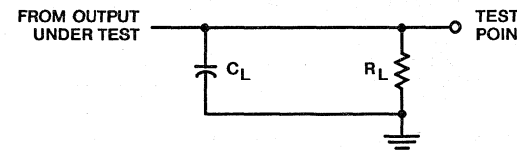
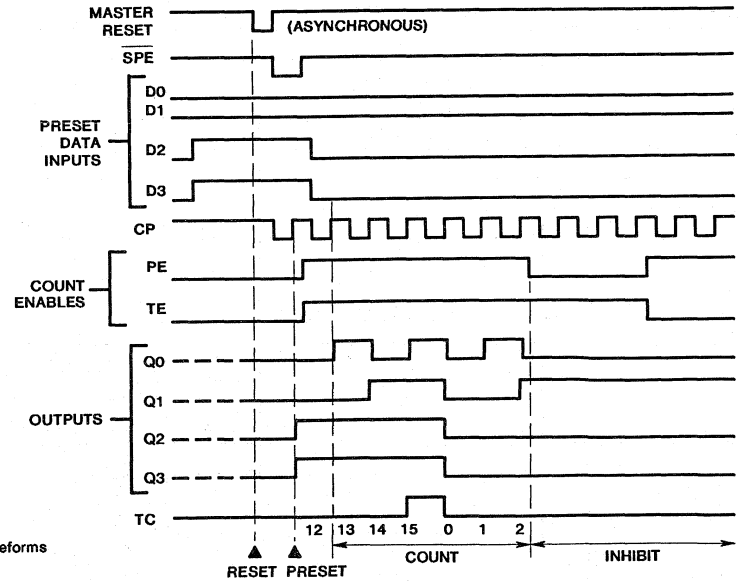


Fig. 3 - Load circuit



Sequence illustrated in waveforms
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

Fig. 4 - Timing waveforms

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	Pn	Qn	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	⎍	X	X	l	l	L	L
	H	⎍	X	X	l	h	H	(a)
Count	H	⎍	h	h	h(c)	X	count	(a)
Inhibit	H	X	l(b)	X	h(c)	X	qn	(a)
	H	X	X	l(b)	h(c)	X	qn	L

H = High Voltage (Steady State)
L = Low Voltage (Steady State)
h = High Voltage level one setup time prior to the Low-to-High clock transition.
l = Low Voltage level one setup time prior to the Low-to-High clock transition.
X = Don't care.
q = Lower-case letters indicate the state of the referenced output prior to the Low-to-High clock transition.
⎍ = Low-to-High clock transition.

NOTES:
(a) The TC output is High when TE is High and the counter is at Terminal Count (HHHH).
(b) The High-to-Low transition of PE or TE should only occur while CP is High for conventional operation.
(c) The Low-to-High transition of $\overline{SPE}$ should only occur while CP is High for conventional operation.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of radiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	1.35	-	0.12 V_{CC}	V
Input High Voltage	V_{IH}	-	3.15	-	3.15	-	V
Input Leakage Current	I_{IL}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS			V_{CC} (V)	LIMITS				UNITS
				200k Rads (Si)		1M Rads (Si)		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delay		t_{PLH}	4.5	-	39	-	50	ns
	CP to Qn	t_{PHL}	4.5	-	39	-	50	ns
	CP to TC	t_{PLH}	4.5	-	43	-	53	ns
		t_{PHL}	4.5	-	43	-	53	ns
	TE to TC	t_{PLH}	4.5	-	27	-	33	ns
		t_{PHL}	4.5	-	27	-	33	ns
	$\overline{MR}$ to Qn	tPHL	4.5	-	51	-	63	ns
	$\overline{MR}$ to TC	t_{PHL}	4.5	-	45	-	56	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS161MS	11, 12, 13, 14, 15	1, 2, 3, 4, 5, 6, 7, 8, 9 10	16	11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6 7, 9, 10, 16
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS161MS	-	4, 6, 8	11, 12, 13, 14, 15	1, 3, 5, 7, 9, 10, 16	2	-

NOTE: Each pin except 8 and 16 shall have a resistor of 10kΩ ±5% for static and 1kΩ ±5% for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

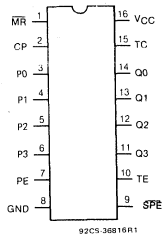
OPEN	GROUND	V_{CC} = 5V
11, 12, 13, 14, 15	8	1, 2, 4, 5, 6, 7, 9, 10, 16

NOTE: Each pin except 8 and 16 shall have a resistor of 680Ω - 47kΩ.

HCTS161MS

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Presettable Counter 4-Bit Binary Counter, Asynchronous Reset

Aerospace Class S Screening



TERMINAL ASSIGNMENT

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 18ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Synchronous counting and loading*
- *Asynchronous reset*
- *Look-ahead carry for high speed counting*
- *Two count enable inputs for n-bit cascading*

The HCTS161MS high-reliability high-speed presettable four-bit binary synchronous counter features asynchronous reset and look-ahead carry logic. The HCTS161 has an active-low master reset to zero, MR. A low level at the synchronous parallel enable, SPE, disables counting and allows data at the preset inputs (P0 - P3) to load the counter. The data is latched to the outputs on the positive edge of the clock input, CP. The HCTS161 has two count enable pins, PE and TE. TE also controls the terminal count output, TC. The terminal count output indicates a maximum count for one clock pulse and is used to enable the next cascaded stage to count.

This device uses advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and HC/HCT while providing radiation hardness. The HCTS161MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL- or CMOS-compatible inputs.

The HCTS161MS is supplied in a 16-lead ceramic flatpack package (K suffix) or a 16-lead dual-in-line weld-seal ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to TTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8 max., V_{IH} = V_{CC}/2 min.
  CMOS Input Current Levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max. ..... +265°C

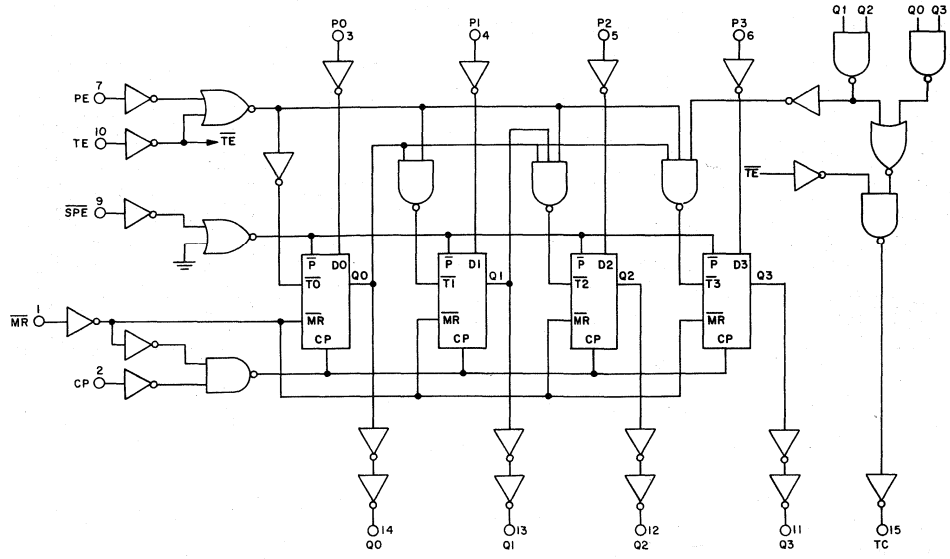


Fig. 1 - Logic diagram.

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C/+125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	40	—	750	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	4.8	—	4	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-4.8	—	-4	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1	—	V_{CC}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.8	—	0.8	
Input High Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±0.5	—	±5	μA
Input Capacitance	C_{IN}•	—	—	10	—	10	pF
Power Dissipation Capacitance	C_{PD}••	—	—	42	—	70	

• Guaranteed but not tested.

•• Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C/+125°C MIN.	LIMITS -55°C/+125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	—	23	—	28	ns
CP to Qn	t_{PHL}		—	31	—	36	
CP to TC	t_{PLH}		—	25	—	30	
	t_{PHL}		—	32	—	37	
TE to TC	t_{PLH}		—	15	—	18	
	t_{PHL}		—	22	—	25	
$\overline{MR}$ to Qn	t_{PHL}		—	34	—	39	
$\overline{MR}$ to TC	t_{PHL}		—	36	—	41	

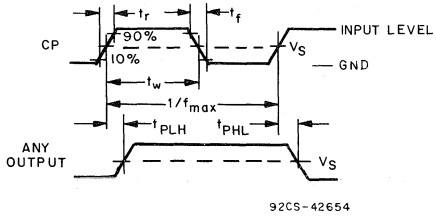


Fig. 2 - Timing waveforms.

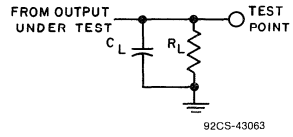


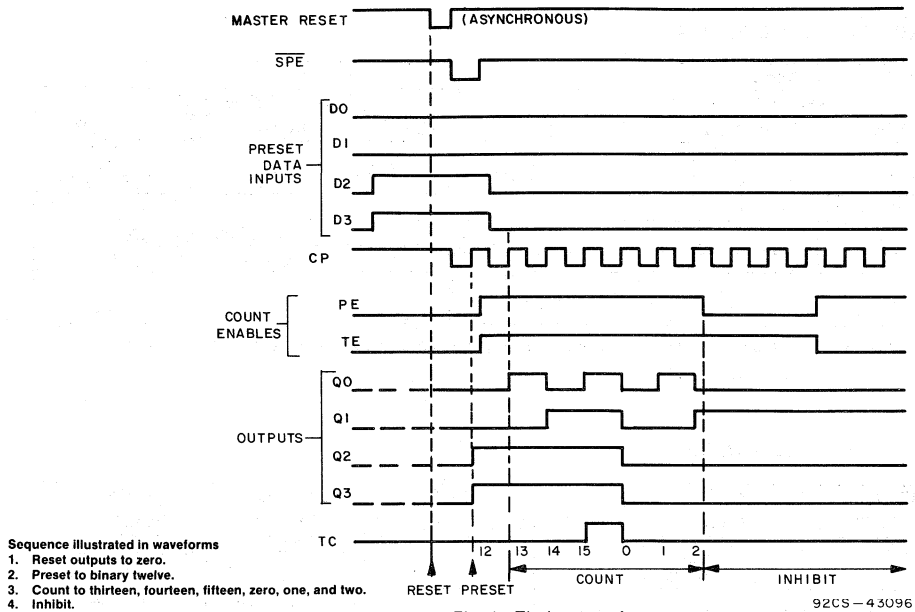
Fig. 3 - Load circuit.

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS $\overline{MR}$	CP	PE	TE	$\overline{SPE}$	Pn	OUTPUTS Qn	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↗	X	X	l	l	L	L
	H	↗	X	X	l	h	H	(a)
Count	H	↗	h	h	h(c)	X	count	(a)
Inhibit	H	X	l(b)	X	h(c)	X	qn	(a)
	H	X	X	l(b)	h(c)	X	qn	L

H = HIGH-voltage-level steady state.
L = LOW-voltage-level steady state.
h = HIGH-voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW-voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
q = Lower-case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↗ = LOW-to-HIGH clock transition.

NOTES:
(a) The TC output is HIGH when TE is HIGH and the counter is at Terminal Count (HHHH).
(b) The HIGH-to-LOW transition of PE or TE should only occur while CP is HIGH for conventional operation.
(c) The LOW-to-HIGH transition of $\overline{SPE}$ should only occur while CP is HIGH for conventional operation.



Sequence illustrated in waveforms
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

Fig. 4 - Timing waveforms.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION† PERFORMANCE At T_A = +25°C

†Radiation measurements are made on 4 samples/wafer. The limits shown are for within 1 hour of radiating.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.75	—	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	4	—	4	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-4	—	-4	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1	—	V_{CC}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.8	—	0.3	
Input High Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IL}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA

SWITCHING CHARACTERISTICS, t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rad (Si) MIN.	LIMITS 1M Rad (Si) MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	—	28	—	31	ns
CP to Qn	t_{PHL}		—	36	—	39	
CP to TC	t_{PLH}		—	30	—	33	
	t_{PHL}		—	37	—	40	
TE to TC	t_{PLH}		—	18	—	21	
	t_{PHL}		—	25	—	28	
$\overline{MR}$ to Qn	t_{PHL}		—	39	—	42	
$\overline{MR}$ to TC	t_{PHL}		—	41	—	44	

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCTS161MS	11, 12, 13, 14, 15	1, 2, 3, 4, 5, 6, 7, 8, 9, 10	16	11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6, 7, 9, 10, 16
Dynamic Burn-In Test-Circuit Connections						
TYPE	OPEN	GROUND	½ V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR	
					50 kHz	25 kHz
HCTS161MS	—	4, 6, 8	11, 12, 13, 14, 15	1, 3, 5, 7, 9, 10, 16	2	—

NOTE: Each pin except 8 and 16 shall have a resistor of 10kΩ ±5% for static burn-in and 1kΩ ±5% for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40 μA	+12 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value

*All measurements will not exceed the absolute limit.

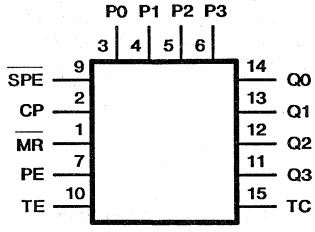
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6, 7, 9, 10, 16

NOTE:
Each pin except 8 and 16 shall have a resistor of 680 Ω - 47 kΩ.

HCTS163MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS, Sync Presettable Counter

Aerospace Class S Screening

Radiation Features:

- *Radiation Hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

The HCTS163MS is a radiation-hardened synchronous presettable counter that feature lookahead carry logic for use in high-speed couting application. The HCTS163MS is a binary counter, and is reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the neagative to positive transition of the clock.

The HCTS163MS is supplied in a 16 lead weld seal ceramic flatpack package (K suffix) or a 16 lead dual-in-line ceramic package (D suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL input logic compatibility
  V_{IL} = 0.8V max., V_{IH} = 2.0V min.
  CMOS input current levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

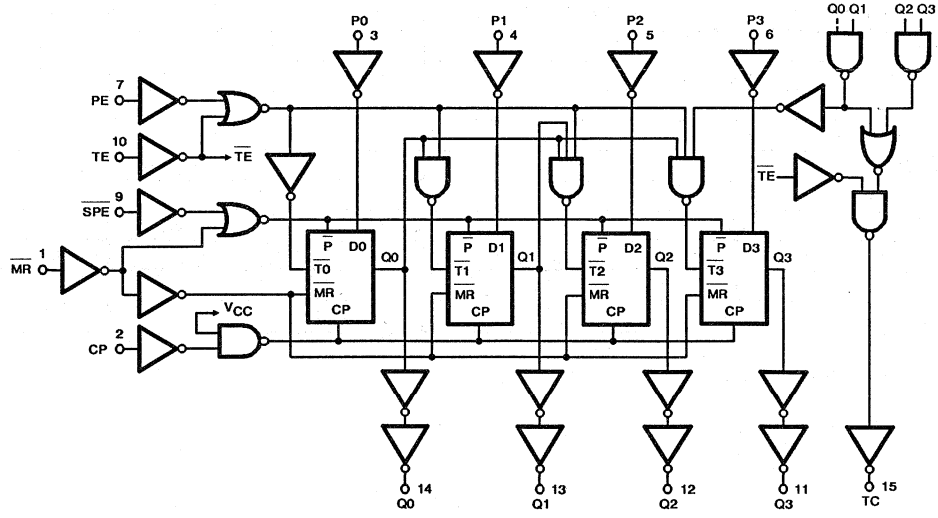


Figure 1 - Logic Diagram.

File Number **2480**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{DD} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	V_{CC}/2	-	V_{CC}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissapation Capacitance	C_{PD}**	-	-	52	-	117	pF

* Guaranteed but not tested.
** Typical value. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
CP to Qn	$t_{PHL/LH}$ Regular Count	4.5	-	25	-	29	ns
CP to TC	t_{PHL}, t_{PLH}	4.5	-	28	-	32	ns
CP to Qn	$t_{PHL/LH}$ Parallel Load	4.5	-	25	-	29	ns
CP to TC	t_{PLH}	4.5	-	28	-	33	ns
TE to TC	t_{PHL}	4.5	-	23	-	29	ns

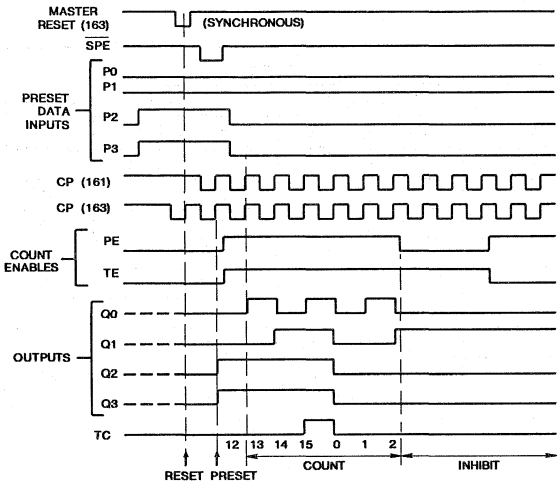


Figure 2 - Timing diagram.

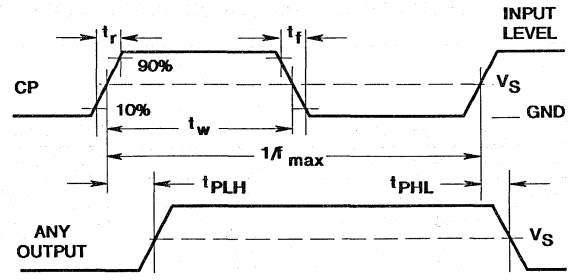


Figure 3 - Load Circuit.

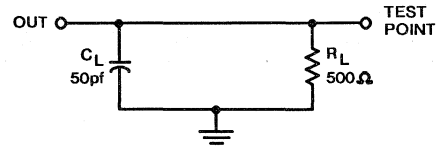


Figure 4 - Load circuit for t_{PHL}, t_{PLH}.

Input Level	V_{CC}
Switching Voltage, V_S	$V_{CC}/2$

TRUTH TABLE

OPERATING MODE	INPUTS $\overline{MR}$	CP	PE	TE	$\overline{SPE}$	Pn	OUTPUTS Qn	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	⎍	X	X	l	l	L	L
	H	⎍	X	X	l	h	H	(a)
Count	H	⎍	h	h	h(c)	X	count	(a)
Inhibit	H	X	l(b)	X	h(c)	X	qn	(a)
	H	X	X	l(b)	h(c)	X	qn	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't Care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
⎍ = LOW-to-HIGH clock transition.

NOTES:
(a) The TC output is HIGH when TE is HIGH and the counter is at Terminal Count (HHHH).
(b) The HIGH-to-LOW transition of PE or TE should only occur while CP is HIGH for conventional operation.
(c) The LOW-to-HIGH transition of $\overline{SPE}$ or MR should only occur while CP is HIGH for conventional operation.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.3	V
Input High Voltage	V_{IH}	-	V_{CC}/2	-	V_{CC}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
CP to Qn	t_{PHL}, t_{PLH} Regular Count	4.5	-	29	-	36	ns
CP to TC	t_{PHL}, t_{PLH}	4.5	-	32	-	40	ns
CP to Qn	t_{PHL}, t_{PLH} Parallel Load	4.5	-	29	-	29	ns
CP to TC	t_{PHL}, t_{PLH}	4.5	-	33	-	33	ns
TE to TC	t_{PHL}, t_{PLH}	4.5	-	29	-	29	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS163MS	11, 12, 13, 14, 15	1, 2, 3, 4, 5, 6, 7, 8, 9, 10	16	11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6, 7, 9, 10, 16

Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS163MS	-	4, 6, 8	11, 12, 13, 14, 15	1, 3, 5, 7, 9, 10	2	-

NOTE: Each pin except V_{CC} and Ground shall have a resistor (10k ± 5% for static and 1k ± 5% for dynamic).

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT	DELTA LIMIT
I_{CC}	40µA	+12µA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

*All measurements will not exceed the absolute limit.

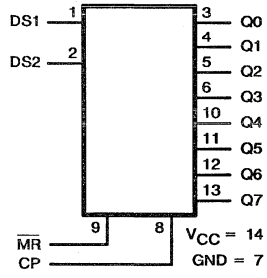
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
11, 12, 13, 14, 15	8	1, 2, 3, 4, 5, 6, 7, 10, 16,

NOTE: Each pin except V_{CC} and Ground will have a resistor of 47kΩ.

HCS164MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS 8-Bit Serial-In/Parallel-Out Shift Register

Aerospace Class S Screening

Type Features:
- *Buffered Inputs*
- *Asynchronous Master Reset*
- *Typical f_{MAX} = 60MHz @ V_{CC} = 5V, C_L = 50pF, T_A = 25°C*

The HCS164MS is an 8-bit serial-in parallel-out shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CP). A LOW on the Master Reset (MR) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided, either one can be used as a Data Enable control.

The HCS164MS utilizes advanced CMOS/SOS technology to achieve high-speed operation and is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with CMOS input compatibility.

The HCS164MS is supplied in a 14-lead weld-seal ceramic flatpack package (K suffix) or a 14-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus driver outputs - 10 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types:*
  4.5 to 5.5V operation
  CMOS Input Logic Compatibility
  V_{IL} = 0.3 V_{CC} max., V_{IH} = 0.7 V_{CC} min.
  CMOS Input Current Levels
  $I_I \leq 5mA$ @ V_{OL}, V_{OH}

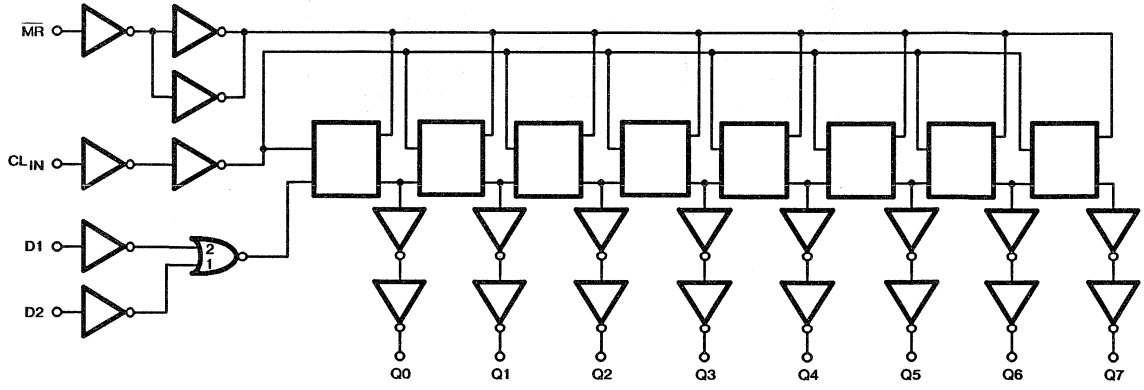


Figure 1 - Logic diagram.

TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	DS1	DS2	Q0	Q1 - Q7
Reset (Clear)	L	X	X	X	L	L-L
Shift	H	⎍	l	l	L	$q_0 - q_6$
	H	⎍	l	h	L	$q_0 - q_6$
	H	⎍	h	l	L	$q_0 - q_6$
	H	⎍	h	h	H	$q_0 - q_6$

H = High Voltage Level

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

L = Low Voltage Level

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

q = Lower case letters indicate the state of the reference input (or output) one setup time prior to the LOW-to-HIGH clock transition

X = Don't Care

⎍ = Transition from Low to High Level

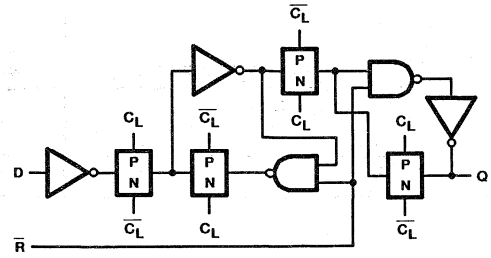


Figure 2 - Flip-Flop Detail.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

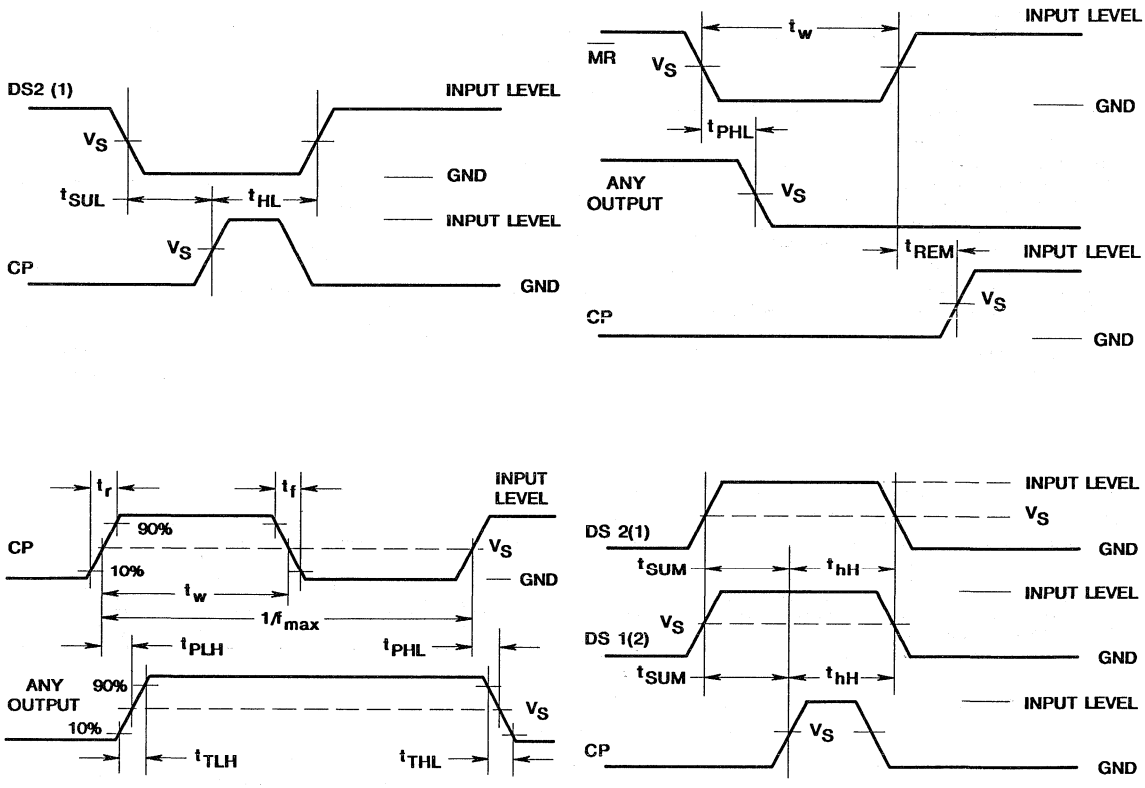
STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1 V	-	V_{CC} -0.1 V	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	90	-	110	pF

*Guaranteed but not tested.
**Typical value. Characterized but not tested.

SWITCHING CHARACTERISTICS, V_{CC} = 4.5V, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	-	32	-	37	ns
CP to Qn	t_{PHL}	-	32	-	37	ns
$\overline{MR}$ to Qn	t_{PHL}	-	32	-	37	ns



	HCS164MS
Input Level	V_{CC}
Switching Voltage, V_S	50% V_{CC}

Figure 3. Transition times, propagation delay times, setup, hold times, and removal times.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC}$ -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.12 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, V_{CC} = 4.5V, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		LIMITS				UNITS
		200k Rads (Si)		1M Rads (Si)		
		MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	-	37	-	47	ns
CP to Qn	t_{PHL}	-	37	-	47	ns
$\overline{MR}$ to Qn	t_{PHL}	-	37	-	47	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS164MS	3, 4, 5, 6, 7, 10, 11, 12, 13	1, 2, 7, 8, 9	14	3, 4, 5, 6, 10, 11, 12, 13	7	1, 2, 8, 9, 14
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS164MS	-	7	3, 4, 5, 6, 10, 11, 12, 13	9, 14	8	1, 2

NOTE: Each pin except 7 and 14 shall have a resistor of 1kΩ (Dynamic) or 10kΩ (Static).

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

*All measurements will not exceed the absolute limit.

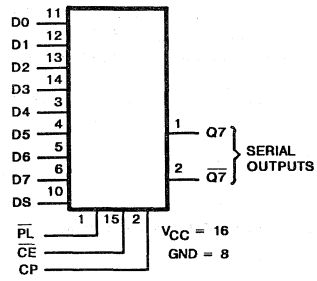
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
3, 4, 5, 6, 10, 11, 12, 13	7	1, 2, 8, 9, 14

NOTE: Each pin except 7 and 14 shall have a resistor of 680Ω - 47kΩ.

HCS165MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS, 8-Bit Parallel-In/ Serial-Out Shift Register

Aerospace Class S Screening

Radiation Features:

- *Radiation Hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2×10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

The HCS165MS is a radiation-hardened 8-bit parallel-in and serial-out register with complementary serial outputs and an asynchronous parallel load input. Because the clock and clock enable inputs are a gated OR structure, their pin assignments are arbitary.

The HCS165MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation-hardened, high-speed, CMOS/SOS logic family with either TTL or CMOS input compatibility.

The HCS165MS is supplied in a 16 lead weld seal ceramic flatpack package (K suffix) or a 16 lead dual-in-line ceramic package (D suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types:*
  4.5 to 5.5V operation
  CMOS input logic compatibility
  V_{IL} = 0.3 V_{CC} max., V_{IH} = 0.7 V_{CC} min.
  CMOS input current levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

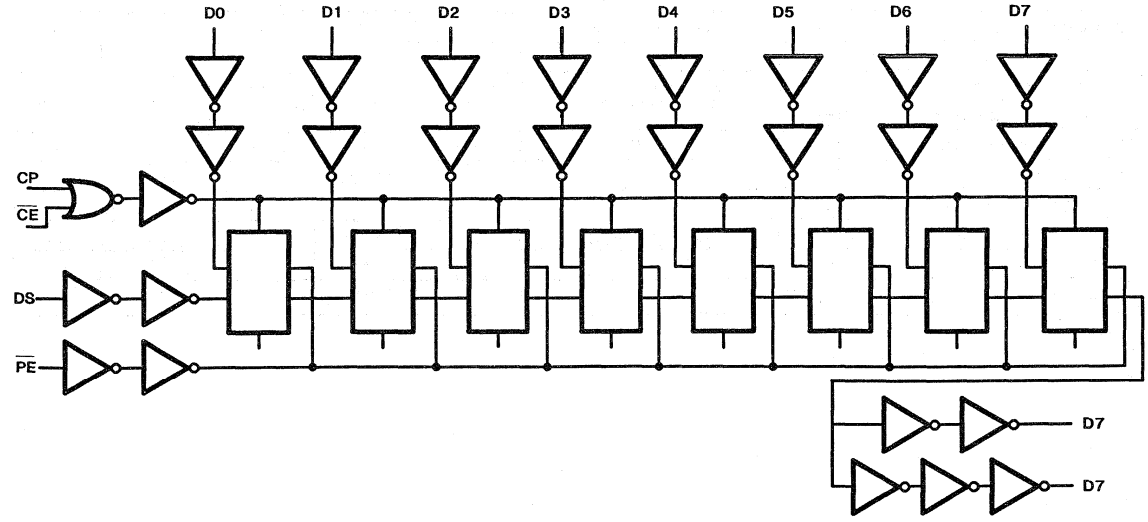


Figure 1 - Logic Diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	5	-	5	pF
Power Dissipation Capacitance	C_{PD}**	-	-	27	-	37	pF

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
CP or $\overline{CE}$ to Q7 or $\overline{Q7}$	t_{PLH}, t_{PHL}	4.5	-	35	-	41	ns
$\overline{PE}$ to Q7 or $\overline{Q7}$	t_{PLH}, t_{PHL}	4.5	-	40	-	46	
D7 to $\overline{Q7}$	t_{PLH}, t_{PHL}	4.5	-	27	-	31	
D7 to Q7	t_{PLH}, t_{PHL}	4.5	-	29	-	35	ns

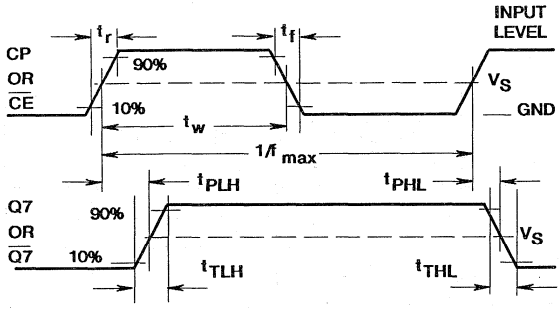


Figure 2 - Serial-shift mode.

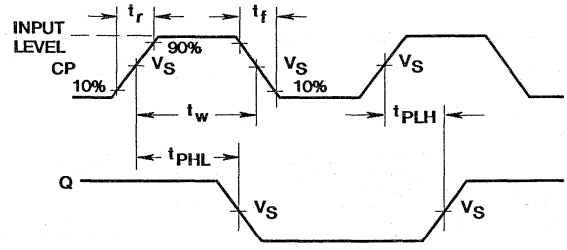


Figure 3 - Parallel-load mode.

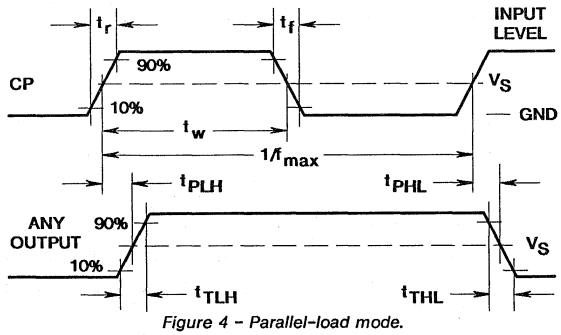


Figure 4 - Parallel-load mode.

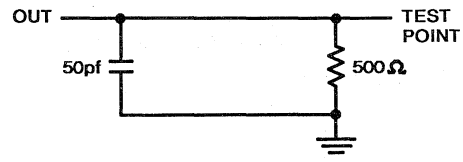


Figure 5 - Load circuit.

Input Level	V_{CC}
Switching Voltage, V_S	$V_{CC}/2$

TRUTH TABLE

OPERATING MODES	INPUTS $\overline{PL}$	$\overline{CE}$	CP	DS	D0 - D7	Q_n REGISTER Q0	Q1 - Q6	OUTPUTS Q7	$\overline{Q7}$
Parallel Load	L	X	X	X	L	L	L-L	L	H
	L	X	X	X	H	H	H-H	H	L
Serial Shift	H	L	⎍	l	X	L	Q_0 - Q_5	Q_6	Q_6
	H	L	⎍	h	X	H	Q_0 - Q_5	Q_6	Q_6
Hold "Do Nothing"	H	H	X	X	X	Q_0	Q_1 - Q_6	Q_7	Q_7

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
Q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't Care
⎍ = LOW-to-HIGH clock transition.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.12 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
CP or $\overline{CE}$ to Q7 or $\overline{Q7}$	t_{PLH}, t_{PHL}	4.5	-	41	-	52	ns
$\overline{PE}$ to Q7 or $\overline{Q7}$	t_{PLH}, t_{PHL}	4.5	-	46	-	58	ns
D7 to Q7	t_{PLH}, t_{PHL}	4.5	-	31	-	39	ns
D7 to $\overline{Q7}$	t_{PLH}, t_{PHL}	4.5	-	35	-	44	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS165MS	7, 9	1, 2, 3, 4, 5, 6, 8, 10 - 15	16	7, 9	8	1, 2, 3, 4, 5, 6, 10 - 16

Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCS165MS	-	3 - 6, 8 11 - 15	7, 9	1, 16	2	10

NOTE: Each pin except V_{CC} and Ground will have a resistor (10k ± 5% for static and 1k ± 5% for dynamic).

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	38µA	+12µA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

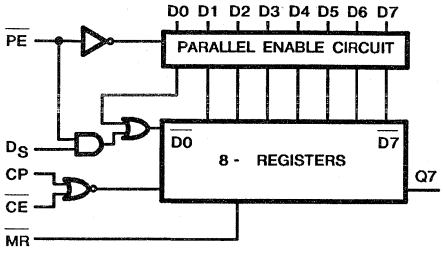
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
7, 9	8	1, 2, 3, 4, 5, 6, 10, 11, 12, 13, 14, 15, 16

NOTE: Each pin except V_{CC} and Ground will have a resistor of 680kΩ to 47kΩ.

HCS166MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS 8 Bit Parallel-In/Serial Out Shift Register

Aerospace Class S Screening

Radiation Features:

- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

The HCS1661MS is a radiation hardened 8-bit parallel or serial-in shift register that fully synchronous werial or parallel data entry and an asychronous master reset. Because the clock and clock enable inputs are a gated OR structure, their pin assignments are arbritary.

The HCS166MS utilized advanced CMOS/SOS technology to achieve high-speed operationdiation hardness. This device is a member of radiation hardened, high-speed, CMOS/SOS logic family with either TTL or CMOS input compatibility.

The HCS166MS is supplied in a 16 lead weld seal ceramic flatpack (K suffix) or a dual-in-line ceramic package (D suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL ICs*
- *DC operating voltage range: 4.5 to 5.5V*
- *HCS types:*
  CMOS LSTTL Input Logic Compatibility
  V_{IL} = 0.3 V_{CC} max., V_{IH} = 0.7 V_{CC} min.
  CMOS Input Current Level
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

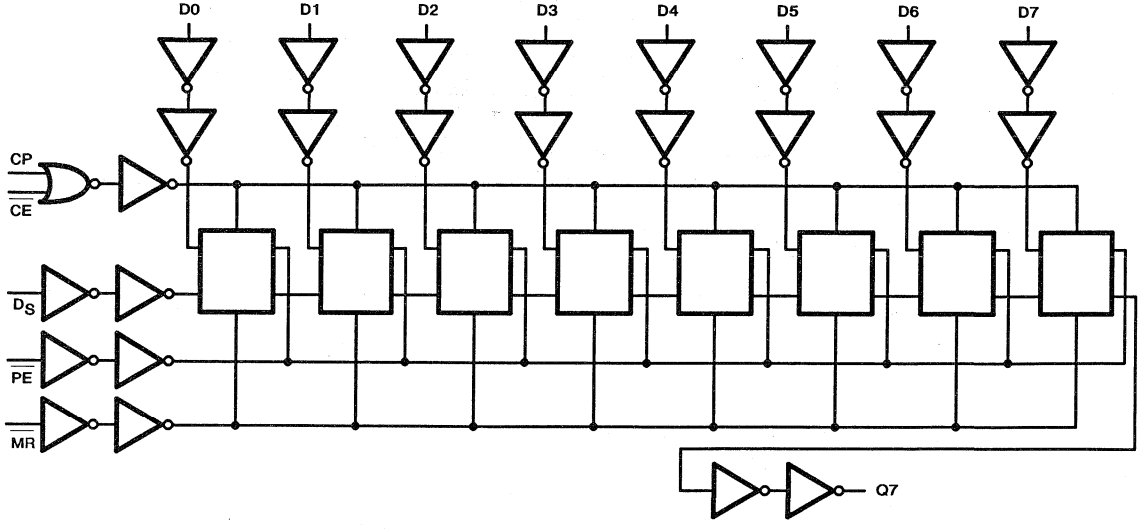


Figure 1 - Logic Diagram

File Number **2482**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE INPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	43	-	54	pF

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF

CHARACTERISTICS		V_{DD} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
CP or $\overline{CE}$ to Q7	t_{PLH}, t_{PHL}	4.5	-	32	-	37	ns
$\overline{MR}$ to Q7	t_{PLH}	4.5	-	31	-	36	ns

TIMING DIAGRAM

Input Level	V_{CC}
Switching Voltage, V_S	$V_{CC}/2$

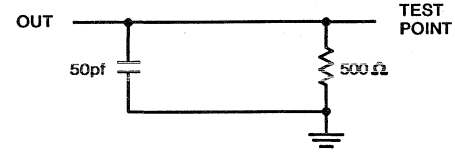


Figure 2 - Load circuit for t_{PHL}, t_{PLH}

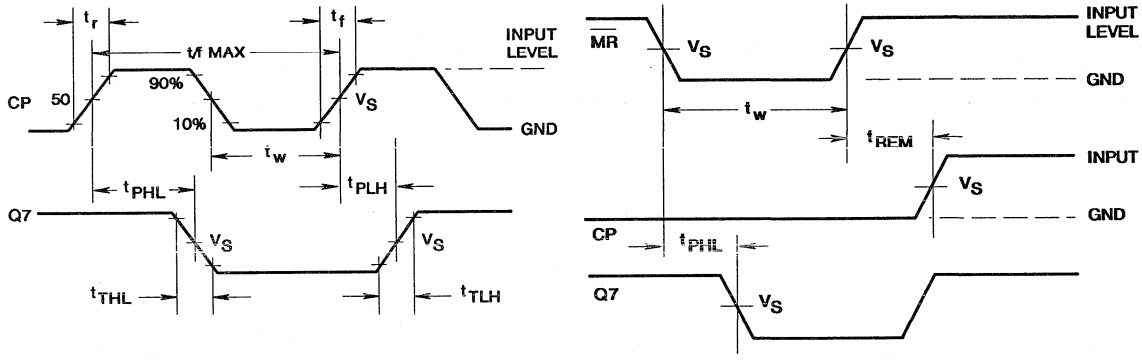


Figure 3 - Timing waveforms

TRUTH TABLE

INPUTS						INTERNAL Q STATES		OUTPUT
MASTER RESET	PARALLEL ENABLE	CLOCK ENABLE	CLOCK	SERIAL	PARALLEL D0 D7	Q0	Q1	Q7
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q00	Q10	Q0
H	L	L	∫	X	a...h	a	b	h
H	H	L	∫	H	X	H	Q0n	Q6n
H	H	L	∫	L	X	L	Q0n	Q6n
H	X	H	∫	X	X	Q00	Q10	Q70

H = High level (steady state).
L = Low level (steady state).
X = Irrelevant (any input, including transitions).
∫ = Transition from low to high level.

a . . . h = The level of steady-state input at inputs D0 thru D7, respectively.
Q00, Q10, Q70 = The level of Q0, Q1, or Q7, respectively, before the indicated steady-state input conditions were established.
Q0n, Q6n = The level of Q0 or Q6, respectively, before the most recent transition of the clock.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of radiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	.12 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IL}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
CP or $\overline{CE}$ to Q7	t_{PLH}, t_{PHL}	4.5	-	37.0	-	47	ns
$\overline{MR}$ to Q7	t_{PHL}	4.5	-	36.0	-	45	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC}	OPEN	GROUND	V_{CC} (6V)
HCS166MS	13	1-12, 14, 15	16	13	8	1-7, 9-12, 14-16
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	V_{CC}	$V_{CC}/2$	50kHz	25kHz
HCS166MS	-	2, 4, 6, 8, 10, 12	3, 5, 9, 11, 14-16	13	7	1

NOTE: Each pin except V_{CC} and GND shall have a resistor (10K ±5% for Static and 1K ±5% for Dynamic).

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	38μA	+1>μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

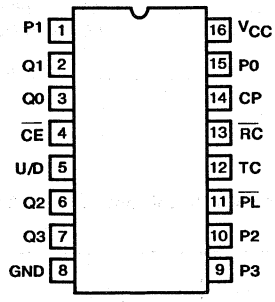
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
iii	iniiiai Eiectricai Tests	interim Eiectricai Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
13	8	1-7, 9-12, 14-16

NOTE: Each pin except V_{CC} and GND shall have a resistor of 680Ω - 47kΩ.

HCTS190MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Synchronous Counter Presettable Up/Down BCD Decade Counter, Asynchronous Reset

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2×10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay (CP – Qn) = 19ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Synchronous counting and asynchronous loading*
- *Two outputs for n-bit cascading*
- *Look ahead carry for high-speed counting*

The HCTS190MS is a asynchronously presettable BCD Decade synchronous counter. Presetting the counter to the number on the preset data inputs (P0 - P3) is accomplished by a low on the Parallel Load input ($\overline{PL}$). Counting occurs when ($\overline{PL}$) is high, Count Enable ($\overline{CE}$) is low, and the Up/Down ($\overline{U}$/D) input is either low for up-counting or high for down-counting. The counter is incremented or decremented synchronously with the low-to-high transition of the clock.

When an overflow or underflow of the counter occurs, the Terminal Count output (TC), which is low during counting, goes high and remains high for one clock cycle. This output can be used for look-ahead carry in high speed cascading. the TC output also initiates the Ripple Clock output (RC) which, normally high, goes low and remains low for the low-level portion of the clock pulse. These counters can be cascaded using the Ripple Carry output.

If the decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one or two counts.

The HCTS190MS is presently supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) and in a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL input logic compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{DD}/2 min.
  CMOS input compatibility
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS				FUNCTION
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Asynchronous Preset
H	H	X	X	No Change

File Number 2474

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0V or V_{DD}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{DD} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{DD} -0.1	-	V_{DD} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	V_{DD}0.3	-	V_{DD}0.3	V
Input High Voltage	V_{IH}	-	V_{DD}0.7	-	V_{DD}0.7	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissapation Capacitance	C_{PD}*	-	-	TBE	-	TBE	pF

* Guaranteed but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{DD} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	25	-	29	ns
$\overline{PL}$ to Qn	t_{PHL}	4.5	-	30	-	35	ns
Propagation Delay	t_{PLH}	4.5	-	23	-	28	ns
Pn to Qn	t_{PHL}	4.5	-	29	-	33	ns
Propagation Delay	t_{PLH}	4.5	-	26	-	30	ns
CP to Qn	t_{PHL}	4.5	-	25	-	28	ns
Propagation Delay	t_{PLH}	4.5	-	21	-	23	ns
CP to $\overline{RC}$	t_{PHL}	4.5	-	19	-	21	ns
Propagation Delay	t_{PLH}	4.5	-	35	-	41	ns
CP to TC	t_{PHL}	4.5	-	34	-	39	ns
Propagation Delay	t_{PLH}	4.5	-	29	-	32	ns
$\overline{U}$/D to $\overline{RC}$	t_{PHL}	4.5	-	30	-	34	ns
Propagation Delay	t_{PLH}	4.5	-	31	-	35	ns
$\overline{U}$/D to TC	t_{PHL}	4.5	-	25	-	29	ns
Propagation Delay	t_{PLH}	4.5	-	20	-	22	ns
$\overline{CE}$ to $\overline{RC}$	t_{PHL}	4.5	-	18	-	20	ns

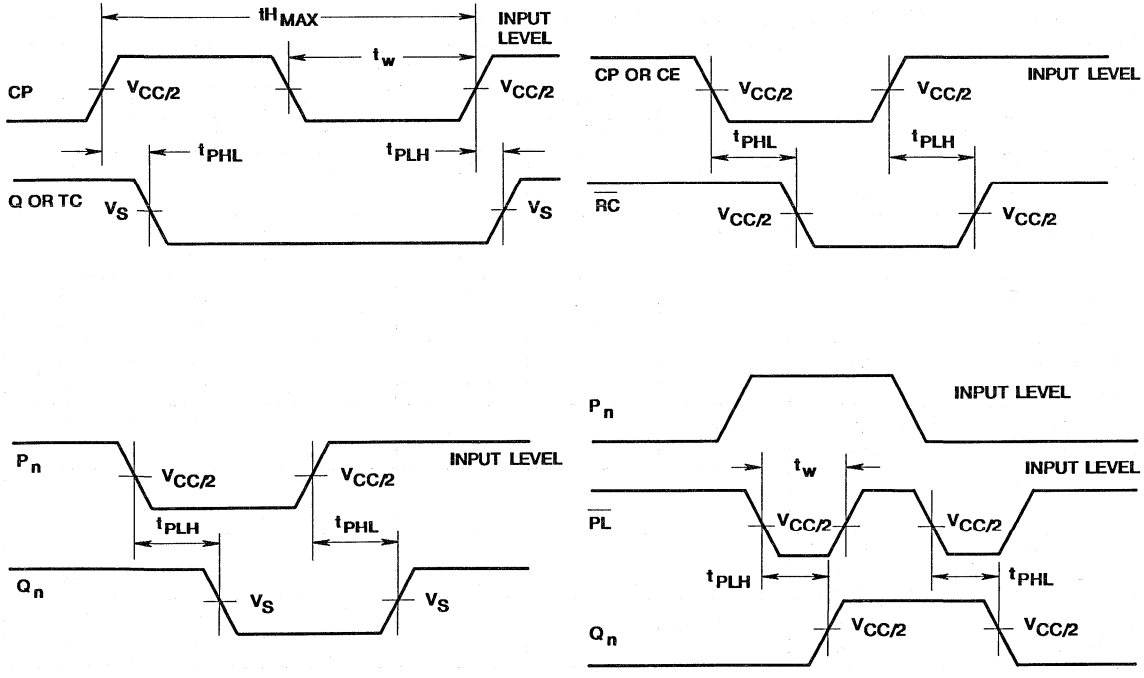


Figure 1 - Timing Waveforms.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0V or V_{DD}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{DD} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	V_{CC} 0.3	-	V_{CC} 0.12	V
Input High Voltage	V_{IH}	-	V_{CC}0.7	-	V_{CC}0.7	-	V
Input Leakage Current	I_{IL}	V_{IN} = 0V or V_{DD}	-	±5.0	-	±5.0	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{DD} (V)	LIMITS				UNITS
			200k RADS(Si)		1M RADS(Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	-	29	-	37	ns
$\overline{PL}$ to Qn	t_{PHL}	4.5	-	35	-	44	ns
Propagation Delay	t_{PLH}	4.5	-	28	-	35	ns
Pn to Qn	t_{PHL}	4.5	-	33	-	42	ns
Propagation Delay	t_{PLH}	4.5	-	30	-	38	ns
CP to Qn	t_{PHL}	4.5	-	28	-	35	ns
Propagation Delay	t_{PLH}	4.5	-	23	-	29	ns
CP to $\overline{RC}$	t_{PHL}	4.5	-	21	-	27	ns
Propagation Delay	t_{PLH}	4.5	-	41	-	52	ns
CP to TC	t_{PHL}	4.5	-	39	-	49	ns
Propagation Delay	t_{PLH}	4.5	-	32	-	40	ns
$\overline{U}$/D to $\overline{RC}$	t_{PHL}	4.5	-	34	-	43	ns
Propagation Delay	t_{PLH}	4.5	-	35	-	44	ns
$\overline{U}$/D to TC	t_{PHL}	4.5	-	29	-	37	ns
Propagation Delay	t_{PLH}	4.5	-	22	-	28	ns
$\overline{CE}$ to $\overline{RC}$	t_{PHL}	4.5	-	20	-	25	ns

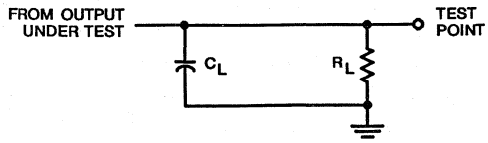
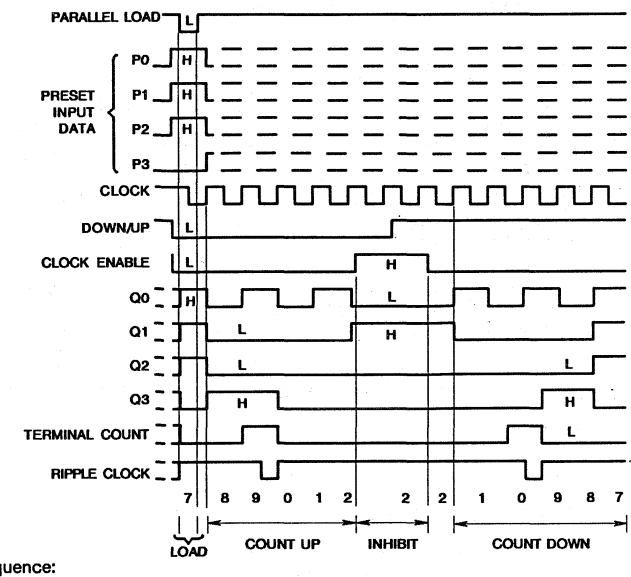


Figure 2 - Load Circuit.



Sequence:
1. Load (Preset) to BCD seven
2. Count up to eight, nine, zero, one and two
3. Inhibit
4. Count down to one, zero, nine, eight, and seven

Figure 3 - Timing Diagram.

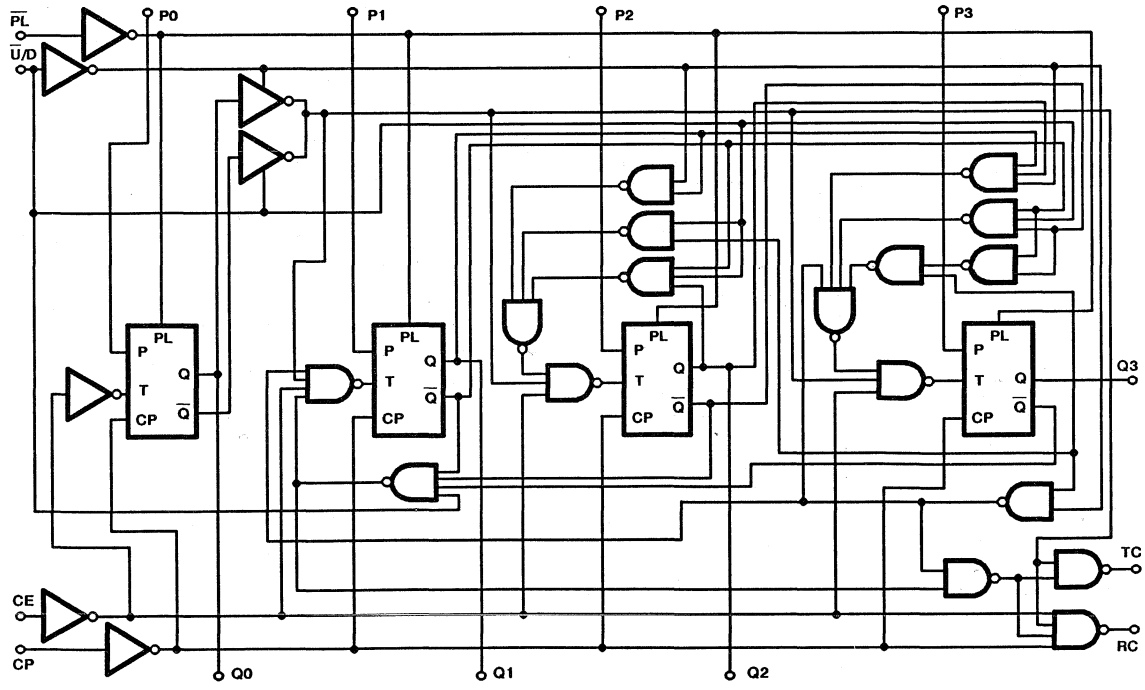


Figure 4 - Logic Diagram.

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS190MS	2, 3, 6, 7 12, 13	1, 4, 5, 8, 9, 10, 11, 14, 15	16	2, 3, 6, 7 12, 13	8	1, 4, 5, 9, 10 11, 14, 15, 16

Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCS190MS	-	1, 4, 5, 8, 9, 10, 15	2, 3, 6, 7, 12, 13	11, 16	14	-

NOTE: Each pin except 7 and 14 shall have a resistor of 10kΩ ±5% static and 1kΩ ±5% for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT	DELTA LIMIT
I_{DD}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

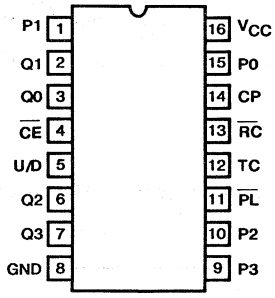
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
2, 3, 6, 7, 12, 13	8	1, 4, 5, 9, 10, 11, 14, 15, 16

NOTE: Each pin except 7 and 14 shall have a resistor of 680Ω - 47kΩ.

HCTS190MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Synchronous Counter Presettable Up/Down BCD Decade Counter, Asynchronous Reset

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2×10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay (CP – Qn) = 19ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Synchronous counting and asynchronous loading*
- *Two outputs for n-bit cascading*
- *Look ahead carry for high-speed counting*

The HCTS190MS is a asynchronously presettable BCD Decade synchronous counter. Presetting the counter to the number on the preset data inputs (P0 – P3) is accomplished by a low on the Parallel Load input (PL). Counting occurs when (PL) is high, Count Enable (CE) is low, and the Up/Down (U/D) input is either low for up-counting or high for down-counting. The counter is incremented or decremented synchronously with the low-to-high transition of the clock.

When an overflow or underflow of the counter occurs, the Terminal Count output (TC), which is low during counting, goes high and remains high for one clock cycle. This output can be used for look-ahead carry in high speed cascading. the TC output also initiates the Ripple Clock output (RC) which, normally high, goes low and remains low for the low-level portion of the clock pulse. These counters can be cascaded using the Ripple Carry output.

If the decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one or two counts.

The HCTS190MS is presently supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) and in a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs – 10 LSTTL loads
- *Wide operating-temperature range: –55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL input logic compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{DD}/2 min.
  CMOS input compatibility
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS				FUNCTION
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Asynchronous Preset
H	H	X	X	No Change

12 LOGIC CIRCUITS

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0V or V_{DD}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.8	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{DD} -0.4V	-4.8	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{DD} -0.1	-	V_{DD} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	V_{DD}/2	-	V_{DD}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissapation Capacitance	C_{PD}**	-	-	TBE	-	TBE	pF

* Characterized but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{DD} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	23	-	27	ns
$\overline{PL}$ to Qn	t_{PHL}	4.5	-	32	-	37	ns
Propagation Delay	t_{PLH}	4.5	-	20	-	24	ns
Pn to Qn	t_{PHL}	4.5	-	30	-	35	ns
Propagation Delay	t_{PLH}	4.5	-	19	-	23	ns
CP to Qn	t_{PHL}	4.5	-	23	-	26	ns
Propagation Delay	t_{PLH}	4.5	-	13	-	16	ns
CP to RC	t_{PHL}	4.5	-	21	-	24	ns
Propagation Delay	t_{PLH}	4.5	-	28	-	33	ns
CP to TC	t_{PHL}	4.5	-	30	-	35	ns
Propagation Delay	t_{PLH}	4.5	-	26	-	30	ns
$\overline{U}$/D to RC	t_{PHL}	4.5	-	27	-	32	ns
Propagation Delay	t_{PLH}	4.5	-	23	-	27	ns
$\overline{U}$/D to TC	t_{PHL}	4.5	-	28	-	31	ns
Propagation Delay	t_{PLH}	4.5	-	15	-	17	ns
$\overline{CE}$ to RC	t_{PHL}	4.5	-	23	-	26	ns

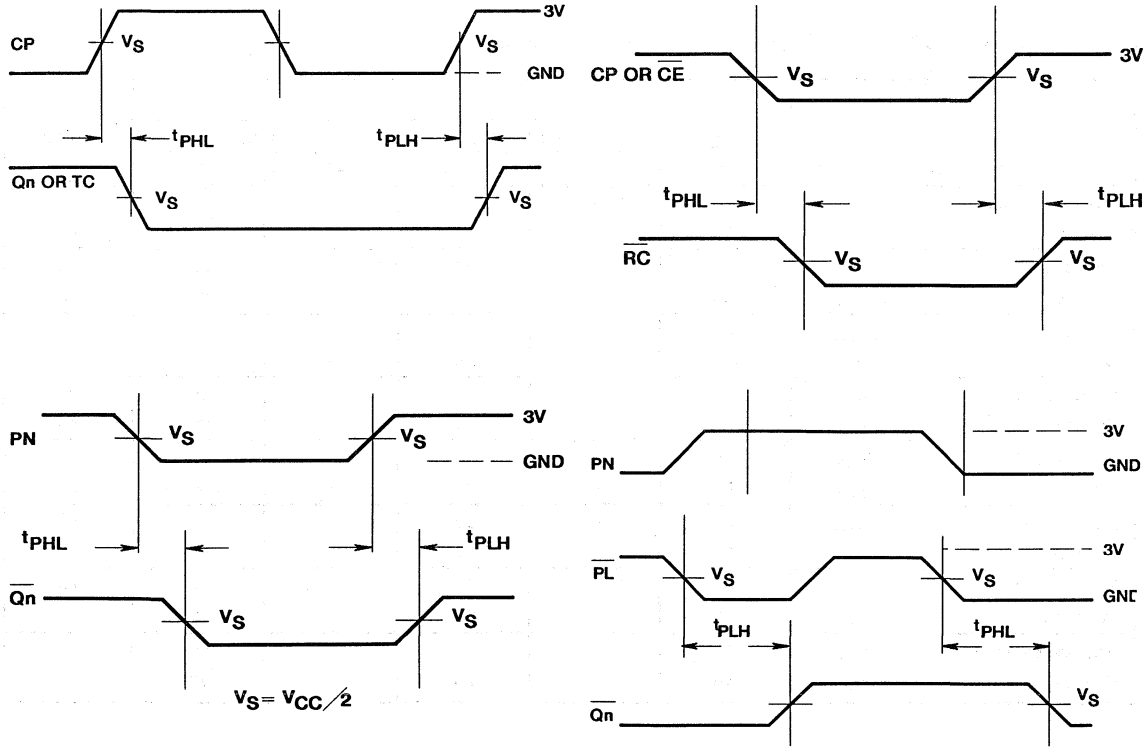


Figure 1 - Timing Waveforms.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN} = 0V or V_{CC}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	4.0	-	4.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-4.0	-	-4.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.3	V
Input High Voltage	V_{IH}	-	V_{CC}/2	-	V_{CC}/2	-	V
Input Leakage Current	I_{IL}	V_{IN} = 0V or V_{CC}	-	±5.0	-	±5.0	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{DD} (V)	LIMITS				UNITS
			200k RADS(Si)		1M RADS(Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	-	27	-	34	ns
PL to Qn	t_{PHL}	4.5	-	37	-	47	ns
Propagation Delay	t_{PLH}	4.5	-	24	-	30	ns
Pn to Qn	t_{PHL}	4.5	-	35	-	44	ns
Propagation Delay	t_{PLH}	4.5	-	23	-	29	ns
CP to Qn	t_{PHL}	4.5	-	26	-	33	ns
Propagation Delay	t_{PLH}	4.5	-	16	-	20	ns
CP to RC	t_{PHL}	4.5	-	24	-	30	ns
Propagation Delay	t_{PLH}	4.5	-	33	-	42	ns
CP to TC	t_{PHL}	4.5	-	35	-	44	ns
Propagation Delay	t_{PLH}	4.5	-	30	-	38	ns
U/D to RC	t_{PHL}	4.5	-	32	-	40	ns
Propagation Delay	t_{PLH}	4.5	-	27	-	34	ns
U/D to TC	t_{PHL}	4.5	-	31	-	39	ns
Propagation Delay	t_{PLH}	4.5	-	17	-	22	ns
CE to RC	t_{PHL}	4.5	-	26	-	33	ns

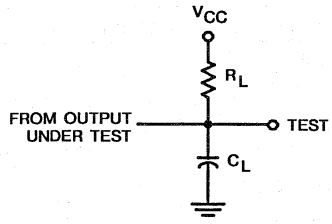
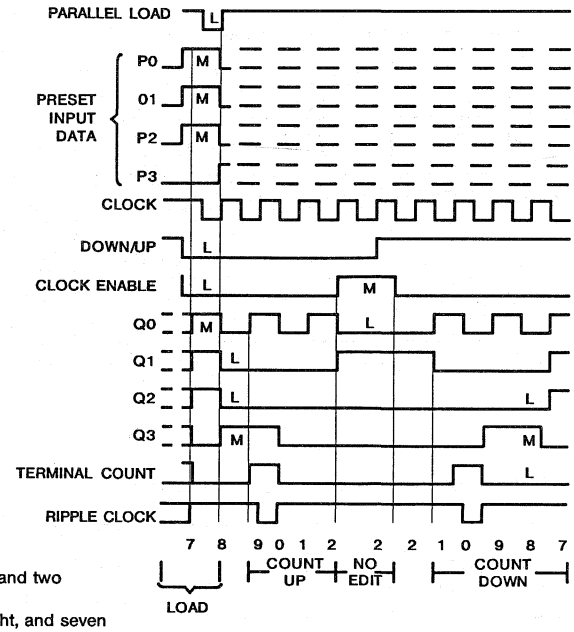


Figure 2 - Load Circuit.



Sequence:
1. Load (Preset) to BCD seven
2. Count up to eight, nine, zero, one and two
3. Inhibit
4. Count down to one, zero, nine, eight, and seven

Figure 3 - Timing Diagram.

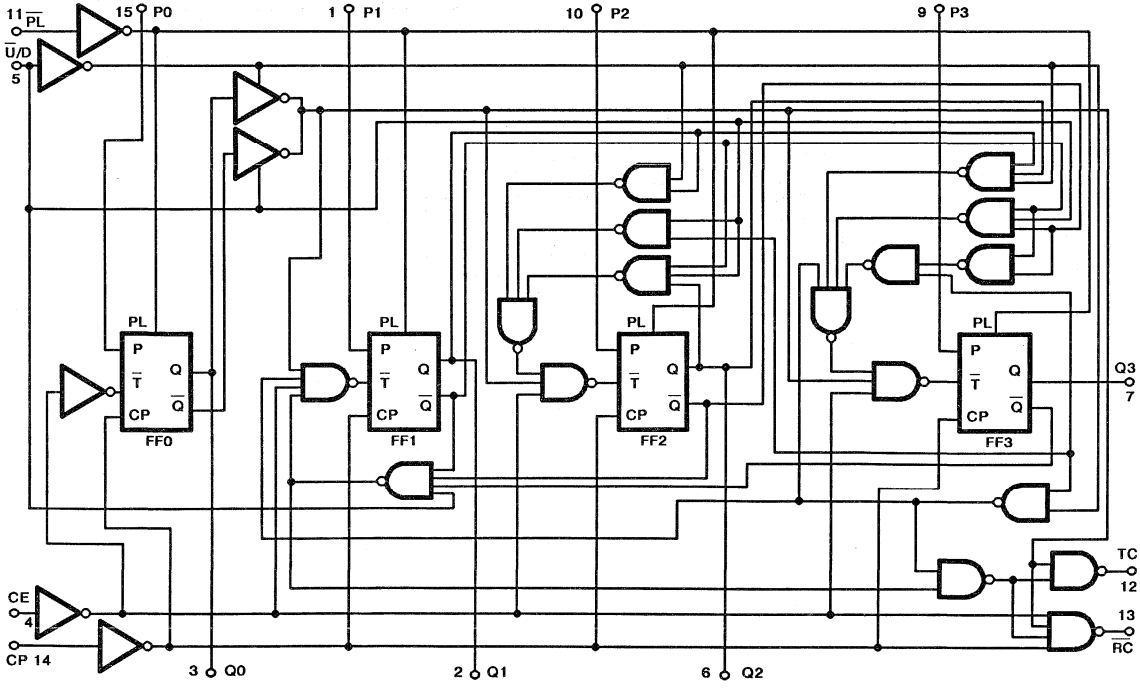


Figure 4 - Logic Diagram.

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS190MS	2, 3, 6, 7 12, 13	1, 4, 5, 8, 9, 10, 11, 14, 15	16	2, 3, 6, 7 12, 13	8	1, 4, 5, 9, 10 11, 14, 15, 16

Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS190MS	-	1, 4, 5, 8, 9, 10, 15	2, 3, 6, 7, 12, 13	11, 16	14	-

NOTE: Each pin except 7 and 14 shall have a resistor of 10KΩ ±5% for static and 1kΩ for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT	DELTA LIMIT
I_{DD}	38µA	+12µA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

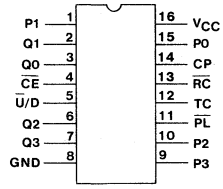
OPEN	GROUND	V_{CC} = 5V
2, 3, 6, 7, 12, 13	8	1, 4, 5, 9, 10, 11, 14, 15, 16

NOTE: Each pin except 7 and 14 shall have a resistor of 680Ω - 47kΩ.

HCTS191MS

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Synchronous Counter, Presettable Up/Down 4-Bit Counter, Asynchronous Reset

Aerospace Class S Screening



TERMINAL ASSIGNMENT

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2×10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay (CP – Qn) = 21ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Synchronous counting and asynchronous loading*
- *Two outputs for n-bit cascading*
- *Look-ahead carry for high-speed counting*

The HCTS191MS is a radiation-hardened asynchronously presettable 4-bit binary up/down synchronous counter. Presetting the counter to the number on the preset data inputs (P0 – P3) is accomplished by a low asynchronous parallel load input ($\overline{PL}$). Counting occurs when $\overline{PL}$ is high, Count Enable ($\overline{CE}$) is low, and the Up/Down ($\overline{U}/D$) input is either low for up-counting or high for down-counting. The counter is incremented or decremented synchronously with the low-to-high transition of the clock.

When an overflow or underflow of the counter occurs, the Terminal Count output (TC), which is low during counting, goes high and remains high for one clock cycle. This output can be used for look-ahead carry in high-speed cascading. The TC output also initiates the Ripple Clock output ($\overline{RC}$) which, normally high, goes low and remains low for the low-level portion of the clock pulse. This counter can be cascaded using the Ripple Carry output.

The HCTS191MS utilizes advanced CMOS/SOS technology to achieve high-speed operation and is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL or CMOS input compatibility.

The HCTS191MS is supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) or a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus driver outputs – 10 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{CC}/2 min.
  CMOS Input Current Levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS				FUNCTION
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Asyn. Preset
H	H	X	X	No Change

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH CLOCK (CP) Transition

NOTE: $\overline{U}/D$ or $\overline{CE}$ should be changed only when CLOCK (CP) is HIGH.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100° C ..... 500 mW
For T_A = +100 to +125° C ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

OPERATING CONDITIONS at T_A = -55° C to +125° C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25° C		-55° C/+125° C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	40	—	750	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	4.8	—	4	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-4.8	—	-4	—	
Low-Level Output Voltage	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Low-Level Input Voltage	V_{IL}	—	—	0.8	—	0.8	
High-Level Input Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±0.5	—	±5	μA
Input Capacitance	C_{IN}*	—	—	10	—	10	pF
Power Dissipation Capacitance	C_{PD}**	—	—	36	—	56	

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

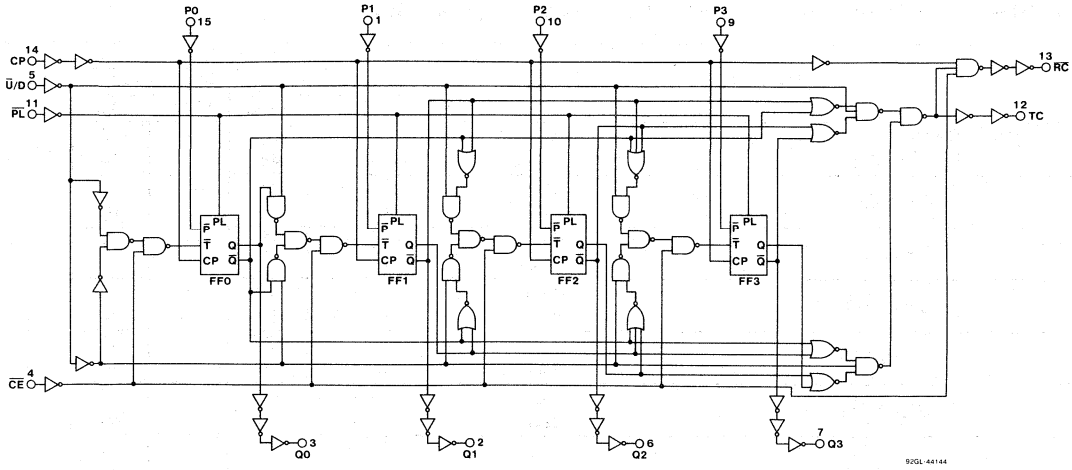


Fig. 1 - Logic diagram.

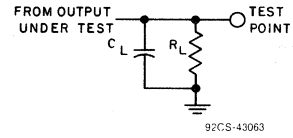
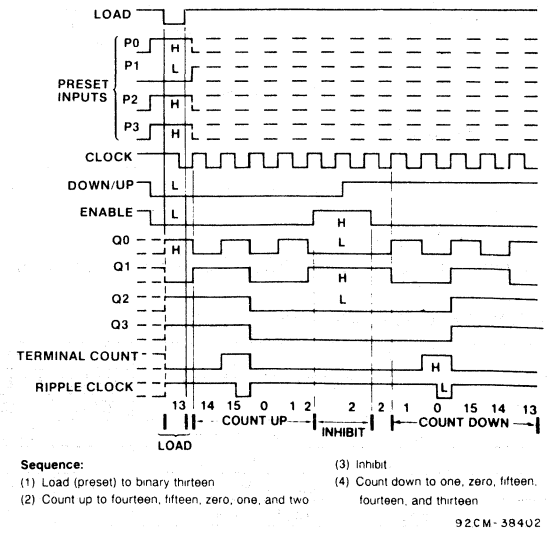


Fig. 2 - Load circuit.



Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

Fig. 3 - Timing diagram-typical load, count, and inhibit sequences.

SWITCHING CHARACTERISTICS, V_{CC} = 4.5 V, t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		LIMITS				UNITS
		+25° C		-55° C/+125° C		
		MIN.	MAX.	MIN.	MAX.	
Propagation Delay $\overline{PL}$ to Qn	t_{PLH}	—	34	—	37	ns
	t_{PHL}	—	44	—	49	
Pn to Qn	t_{PLH}	—	27	—	31	
	t_{PHL}	—	39	—	45	
CP to Qn	t_{PLH}	—	26	—	30	
	t_{PHL}	—	29	—	33	
CP to $\overline{RC}$	t_{PLH}	—	20	—	23	
	t_{PHL}	—	32	—	34	
CP to TC	t_{PLH}	—	37	—	42	
	t_{PHL}	—	40	—	46	
$\overline{U}$/D to $\overline{RC}$	t_{PLH}	—	42	—	45	
	t_{PHL}	—	38	—	43	
$\overline{U}$/D to TC	t_{PLH}	—	34	—	38	
	t_{PHL}	—	42	—	45	
$\overline{CE}$ to $\overline{RC}$	t_{PLH}	—	22	—	25	
	t_{PHL}	—	35	—	38	

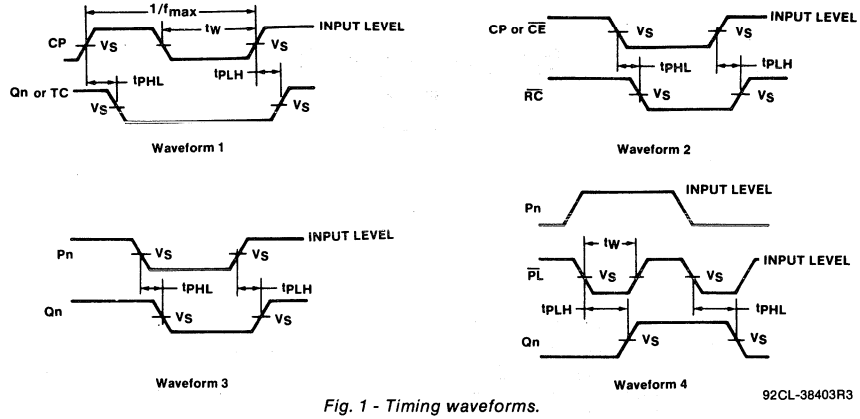


Fig. 1 - Timing waveforms.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... ≥ 10^{12} rads (Si)/s
Transient Upset ..... ≥ 10^{10} rads (Si)/s, 20-ns pulse

POST-RADIATION PERFORMANCE at T_A = +25° C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rad (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.75	—	2	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	4	—	4	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-4	—	-4	—	
Low-Level Output Voltage	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Low-Level Input Voltage	V_{IL}	—	—	0.8	—	0.3	
High-Level Input Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA

• Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Propagation Delay $\overline{PL}$ to Qn	t_{PLH}	4.5	-	37	-	47	ns
	t_{PHL}	4.5	-	49	-	62	ns
Pn to Qn	t_{PLH}	4.5	-	31	-	39	ns
	t_{PHL}	4.5	-	45	-	57	ns
CP to Qn	t_{PLH}	4.5	-	30	-	38	ns
	t_{PHL}	4.5	-	33	-	42	ns
CP to $\overline{RC}$	t_{PLH}	4.5	-	23	-	29	ns
	t_{PHL}	4.5	-	34	-	43	ns
CP to TC	t_{PLH}	4.5	-	42	-	53	ns
	t_{PHL}	4.5	-	46	-	58	ns
$\overline{U}$/D to $\overline{RC}$	t_{PLH}	4.5	-	45	-	57	ns
	t_{PHL}	4.5	-	43	-	54	ns
$\overline{U}$/D to TC	t_{PLH}	4.5	-	38	-	48	ns
	t_{PHL}	4.5	-	45	-	57	ns
$\overline{CE}$ to $\overline{RC}$	t_{PLH}	4.5	-	25	-	32	ns
	t_{PHL}	4.5	-	38	-	48	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections

TYPE	STATIC BURN-IN I OPEN	STATIC BURN-IN I GROUND	STATIC BURN-IN I V_{CC} (6V)	STATIC BURN-IN II OPEN	STATIC BURN-IN II GROUND	STATIC BURN-IN II V_{CC} (6V)
HCTS191MS	2, 3, 6, 7, 12, 13	1, 4, 5, 8, 9, 10, 11, 14, 15	16	2, 3, 6, 7, 12, 13	8	1, 4, 5, 9, 10, 11, 14, 16

Dynamic Burn-in Test-Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	OSCILLATOR 50kHz	OSCILLATOR 25kHz
HCTS191MS	-	1, 4, 5, 8, 9 10, 15	2, 3, 6, 7, 12, 13	11, 16	14	-

NOTE: Each pin except 7 and 14 shall have a resistor of 680Ω - 47kΩ.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

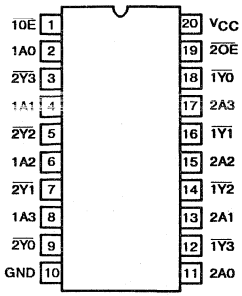
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
2, 3, 6, 7, 12, 13	8	1, 4, 5, 9, 10, 11, 14, 16

NOTE: Each pin except 7 and 14 shall have a resistor of 680Ω - 47kΩ.

HCTS240MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Octal Buffer/Line Driver, 3-State

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-State outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCTS240MS is an inverting octal buffer/line driver with two active-low output enables. This device uses the Harris advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and HC/HCT while providing radiation hardness. The HCTS240MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL- or CMOS-compatible inputs.

The HCTS240MS is supplied in a 20-lead weld-seal ceramic flatpack package (K suffix) and in a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus-driver outputs - 15 LSTTL loads
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL input logic compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{CC}/2 min.
  CMOS input current levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	H
L	H	L
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

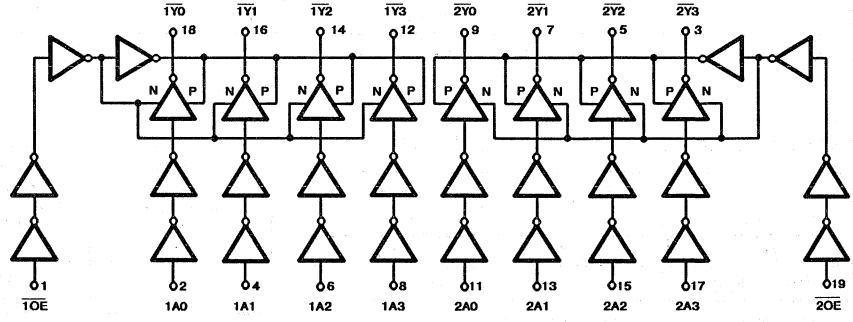


Figure 1 - Logic diagram.

File Number **2105**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, Output (I/O) = $-0.5V < V_O < V_{CC} + 0.5V$ ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6.0	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC} - 0.4V$	-7.2	-	-6.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	$V_{CC}/2$	-	$V_{CC}/2$	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±1	-	±50	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Output Capacitance	C_{OUT}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	35	-	60	pF

* Guaranteed but not tested.
** Typical value. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	15	-	20	ns
	t_{PHL}	4.5	-	15	-	20	ns
Enable to Output	t_{PZL}	4.5	-	20	-	25	ns
	t_{PZH}	4.5	-	20	-	25	ns
Disable to Output	t_{PLZ}	4.5	-	25	-	35	ns
	t_{PHZ}	4.5	-	25	-	35	ns

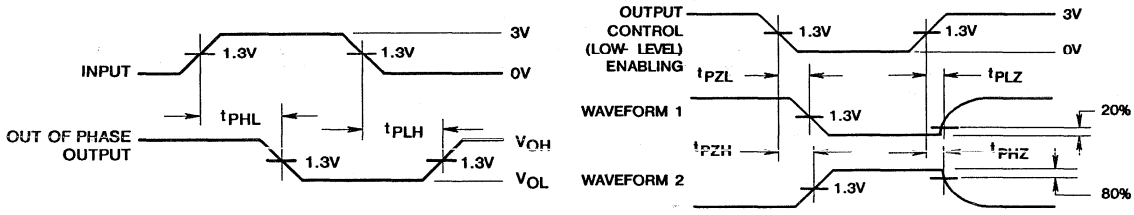


Figure 2 - Timing diagrams.

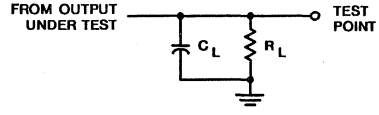


Figure 3 - Load circuit for t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}.

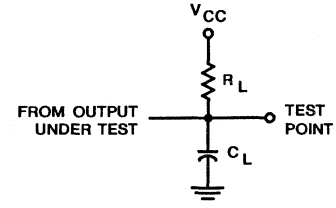


Figure 4 - Load circuit for t_{PZL}, t_{PLZ}.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of radiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.3	V
Input High Voltage	V_{IH}	-	$V_{CC}/2$	-	$V_{CC}/2$	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±50	-	±100	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	-	20	-	25	ns
	t_{PHL}	4.5	-	20	-	25	ns
Enable to Output	t_{PZL}	4.5	-	25	-	32	ns
	t_{PZH}	4.5	-	25	-	32	ns
Disable to Output	t_{PLZ}	4.5	-	35	-	44	ns
	t_{PHZ}	4.5	-	35	-	44	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS240MS	3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	20	3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11 13, 15, 17, 19, 20

Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS240MS	-	1, 10, 19	3, 5, 7, 9, 12, 14, 16, 18	20	2, 4, 6, 8, 11 13, 15, 17	-

NOTE: Each pin except 10 and 20 shall have a resistor of 10kΩ ±5% for static and 680Ω for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value
I_{OZL}	-1μA	-200nA
I_{OZH}	+1μA	+200nA

* All measurements will not exceed the absolute limit.

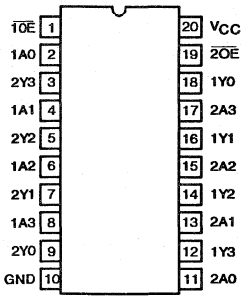
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11, 13 15, 17, 19, 20

NOTE: Each pin except 10 and 20 shall have a resistor of 680Ω - 47kΩ.

HCS244MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Octal Buffer/Line Driver, 3-State

Aerospace Class S Screening

Radiation Features:

- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:

- *Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-State outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCS244MS is an non-inverting octal buffer/line driver with two active-low output enables. The HCS244MS is a radiation-hardened CMOS/SOS octal buffer with CMOS-compatible inputs.

The HCS244MS is supplied in a 20-lead weld-seal flatpack package (K suffix) and in a 20-lead dual-in-line ceramic package (D suffix).

Family Features:

- *Fanout (over temperature range): Bus-driver outputs - 15 LSTTL loads*
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types: High noise immunity: N_{IL} = 20%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5V*

TRUTH TABLE

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

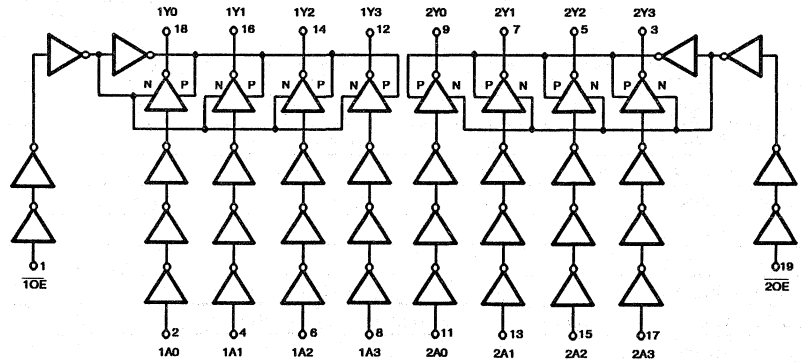


Figure 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, Output (I/O) = $-0.5V < V_O < V_{DD} + 0.5V$ ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6.0	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC}$ -0.4V	-7.2	-	-6.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 VCC	-	0.3 VCC	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±1	-	±50	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Output Capacitance	C_{OUT}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	30	-	30	pF

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	21	-	25	ns
	t_{PHL}	4.5	-	21	-	25	ns
Enable to Output	t_{PZL}	4.5	-	25	-	30	ns
	t_{PZH}	4.5	-	20	-	24	ns
Disable to Output	t_{PLZ}	4.5	-	25	-	30	ns
	t_{PHZ}	4.5	-	25	-	30	ns

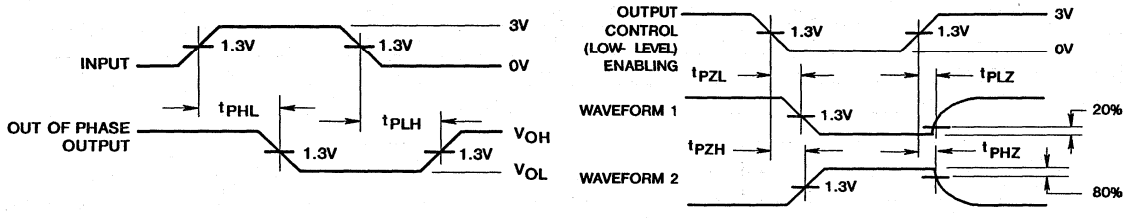


Figure 2 - Timing diagrams.

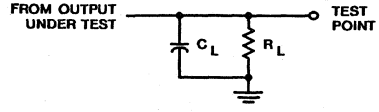


Figure 3 - Load circuit for t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}.

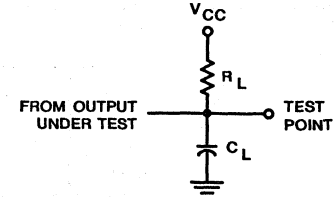


Figure 4 - Load circuit for t_{PZL}, t_{PLZ}.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of radiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.12 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±50	-	±100	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	-	25	-	32	ns
	t_{PHL}	4.5	-	25	-	32	ns
Enable to Output	t_{PZL}	4.5	-	30	-	38	ns
	t_{PZH}	4.5	-	24	-	30	ns
Disable to Output	t_{PLZ}	4.5	-	30	-	38	ns
	t_{PHZ}	4.5	-	30	-	38	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS244MS	3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	20	3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11 13, 15, 17, 19, 20
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCS244MS	-	1, 10, 19	3, 5, 7, 9, 12, 14, 16, 18	20	2, 4, 6, 8, 11 13, 15, 17	-

NOTE: Each pin except 10 and 20 shall have a resistor of 10kΩ for static and 680Ω for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value
I_{OZL}	-1μA	-200nA
I_{OZH}	+1μA	+200nA

* All measurements will not exceed the absolute limit.

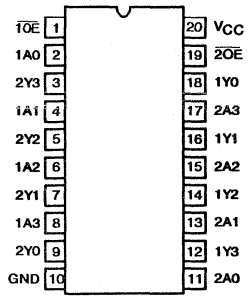
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11, 13 15, 17, 19, 20

NOTE: Each pin except 10 and 20 shall have a resistor of 680Ω - 47kΩ.

HCTS244MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Octal Buffer/Line Driver, 3-State

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 18ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-State outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCTS244MS is an non-inverting octal buffer/line driver with two active-low output enables. The HCTS244MS is a radiation-hardened CMOS/SOS octal buffer with TTL-compatible inputs.

The HCTS244MS is supplied in a 20-lead weld-seal flatpack package (K suffix) and in a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range): Bus-driver outputs - 15 LSTTL loads*
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types: 4.5 to 5.5V operation LSTTL input logic compatibility: V_{IL} = 0.8V max., V_{IH} = V_{CC}/2 min. CMOS input compatibility: $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}*

TRUTH TABLE

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z =High Impedance

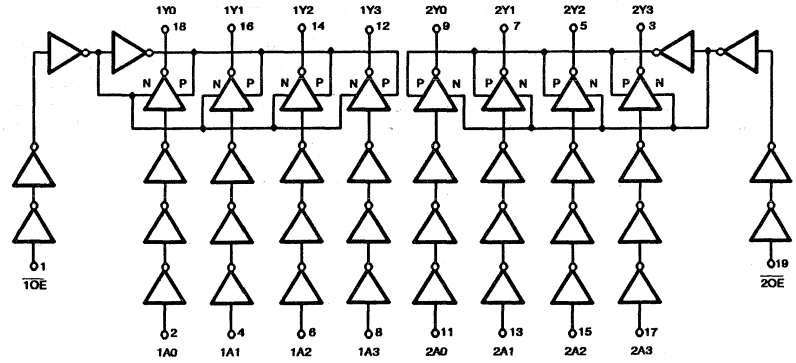


Figure 1 - Logic diagram.

File Number **2133**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, Output (I/O) = $-0.5V < V_O < V_{DD} + 0.5V$ ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6.0	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC} - 0.4V$	-7.2	-	-6.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	$V_{CC}/2$	-	$V_{CC}/2$	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±1	-	±50	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Output Capacitance	C_{OUT}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	30	-	30	pF

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	17	-	20	ns
	t_{PHL}	4.5	-	23	-	26	ns
Enable to Output	t_{PZL}	4.5	-	28	-	32	ns
	t_{PZH}	4.5	-	22	-	25	ns
Disable to Output	t_{PLZ}	4.5	-	22	-	25	ns
	t_{PHZ}	4.5	-	22	-	25	ns

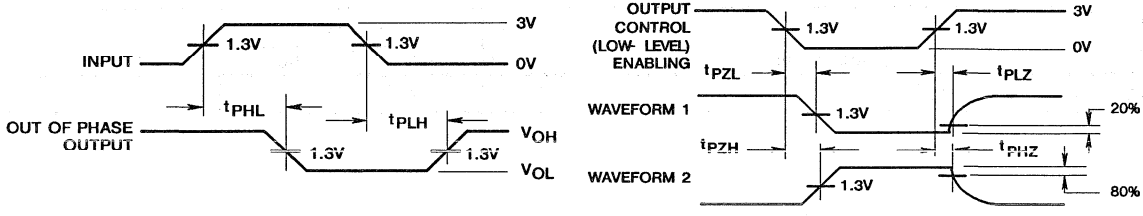


Fig. 2 - Timing diagrams

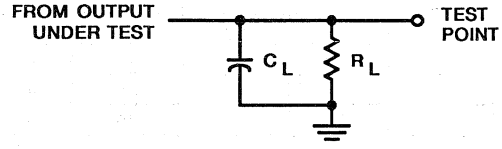


Fig. 3 - Load circuit for t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}.

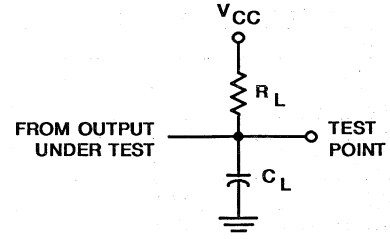


Fig. 4 - Load circuit for t_{PZL}, t_{PLZ}.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of radiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.3	V
Input High Voltage	V_{IH}	-	$V_{CC}/2$	-	$V_{CC}/2$	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±50	-	±100	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	-	20	-	25	ns
	t_{PHL}	4.5	-	26	-	33	ns
Enable to Output	t_{PZL}	4.5	-	32	-	40	ns
	t_{PZH}	4.5	-	25	-	35	ns
Disable to Output	t_{PLZ}	4.5	-	25	-	32	ns
	t_{PHZ}	4.5	-	25	-	32	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS244MS	3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	20	3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11 13, 15, 17, 19, 20

Dynamic Burn-In Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS244MS	-	1, 10, 19	3, 5, 7, 9, 12, 14, 16, 18	20	2, 4, 6, 8, 11 13, 15, 17	-

NOTE: Each pin except 10 and 20 shall have a resistor of 10kΩ ±5% for static and 680Ω for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value
I_{OZL}	-1μA	-200nA
I_{OZH}	+1μA	+200nA

* All measurements will not exceed the absolute limit.

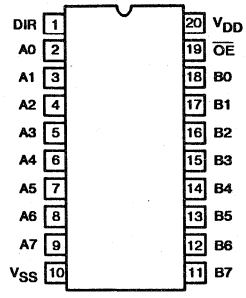
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11, 13 15, 17, 19, 20

NOTE:
Each pin except 10 and 20 shall have a resistor of 680Ω - 47kΩ.

HCS245MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Octal Transceiver

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-State outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCS245MS is a non-inverting high-speed octal bidirectional 3-state transceiver intended for two-way asynchronous communication between data buses. The HCS245MS allows data transmission from the A bus to the B bus or from the B bus to the A bus. The logic level at the direction input (DIR) determines the data direction. The output enable input (OE) puts the I/O port in the high-impedance state when high.

The HCS245MS is supplied in a 20-lead weld-seal flat pack package (K suffix) and a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus driver outputs - 15 LSTTL loads
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types:*
  4.5 to 5.5V operation
  High noise immunity:
  V_{IL} = 0.3 V_{CC} max., V_{IH} = 0.7 V_{CC} min.
  CMOS input current levels
  I_I < 5μA @ V_{OL}, V_{OH}

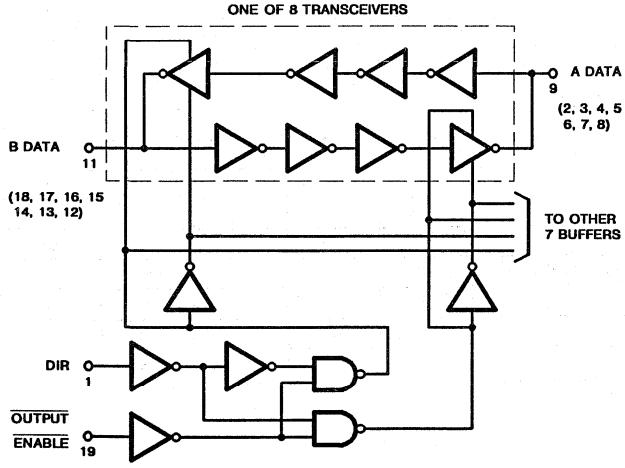


Fig. 1 - Logic diagram.

TRUTH TABLE		
CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

H = high level, L = low level, X = irrelevant

To prevent excess currents in the High-Z (Isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

12 LOGIC CIRCUITS

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR.
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-7.2	-	-6	-	mA
Low-Level Output Voltage	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Low-Level Output Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
High-Level Input Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±1	-	±50	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Output Capacitance	C_{OUT}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}*	-	-	45	-	45	pF

* Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	19	-	23	ns
	t_{PHL}	4.5	-	19	-	23	ns
Enable to Output	t_{PZL}	4.5	-	26	-	30	ns
	t_{PZH}	4.5	-	26	-	30	ns
Disable to Output	t_{PLZ}	4.5	-	28	-	33	ns
	t_{PHZ}	4.5	-	28	-	33	ns

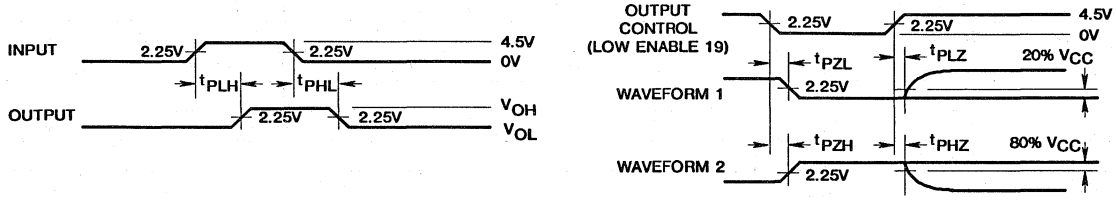


Fig. 2 - Timing diagrams

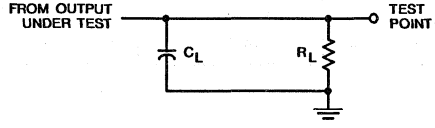


Fig. 3 - Load circuit for t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}.

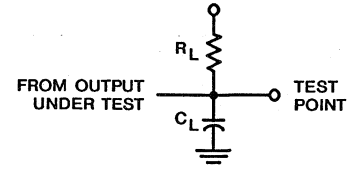


Fig. 4 - Load circuit for t_{PZL}, t_{PLZ}.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6	-	5	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6	-	-5	-	mA
Low-Level Output Voltage	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.12 V_{CC}	V
High-Level Input Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA
Output Leakage Current	I_{OZ}	V_{OUT} = 0V or V_{CC}	-	±50	-	±100	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	-	23	-	28	ns
	t_{PHL}	4.5	-	23	-	28	ns
Enable to Output	t_{PZL}	4.5	-	30	-	36	ns
	t_{PZH}	4.5	-	30	-	36	ns
Disable to Output	t_{PLZ}	4.5	-	33	-	33	ns
t_{PHZ}	4.5	- 33 -	33	ns			

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS245MS	2-9	1, 10-19	20	-	10	1-9, 11-18, 19, 20
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (6V)	V_{CC} (6V)	50kHz	25kHz
HCS245MS	-	10	11-18	1, 20	2-9	19

NOTE: Each pin except 10 and 20 shall have a resistor of 10kΩ ±5% for static and 680Ω ±5% for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value
I_{OZL}	-1μA	-200nA
I_{OZH}	+1μA	+200nA

* All measurements will not exceed the absolute limit.

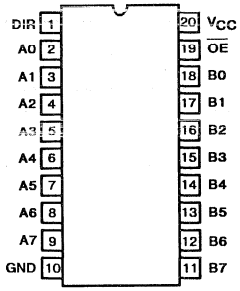
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
-	10	1-9, 11-18, 19, 20

NOTE:
Each pin except 10 and 20 shall have a resistor of 680Ω - 47kΩ.

HCTS245MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Octal Transceiver

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-State outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCTS245MS is a high-reliability radiation-hardened CMOS/SOS non-inverting 3-state octal transceiver intended for two-way asynchronous communication between data buses. The HCTS245MS allows data transmission from the A bus to the B bus or from the B bus to the A bus. The logic level at the direction input (DIR) determines the data direction. When the output enable input ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state.

This device uses the Harris advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and HC/HCT while providing radiation hardness. The HCTS245MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL- or CMOS-compatible inputs.

The HCTS245MS is supplied in a 20-lead ceramic flatpack package (K suffix) and in a 20-lead dual-in-line weld-seal side-brazed ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus driver outputs - 15 LSTTL loads
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to TTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL input logic compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{CC}/2 min.
  CMOS input current levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

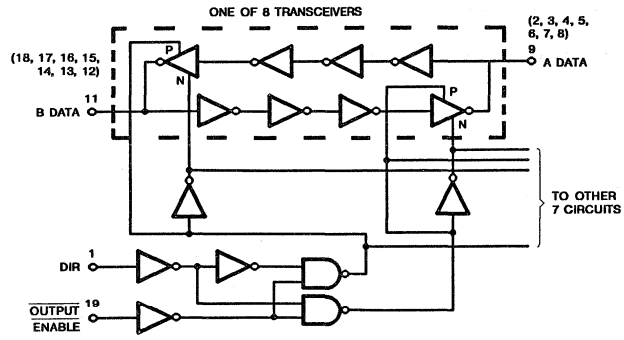


Fig. 1 - Logic diagram.

TRUTH TABLE		
CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

H = high level, L = low level, X = irrelevant

To prevent excess currents in the High-Z (Isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

File Number **2360**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, Output (I/O) = $-0.5V < V_O < V_{CC} + 0.5V$ ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC} - 0.4V$	-7.2	-	-6	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	$V_{CC}/2$	-	$V_{CC}/2$	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±1	-	±50	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Output Capacitance	C_{OUT}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	45	-	45	pF

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	18	-	21	ns
	t_{PHL}	4.5	-	21	-	24	ns
Enable to Output	t_{PZL}	4.5	-	28	-	33	ns
	t_{PZH}	4.5	-	26	-	31	ns
Disable to Output	t_{PLZ}	4.5	-	28	-	33	ns
	t_{PHZ}	4.5	-	28	-	33	ns

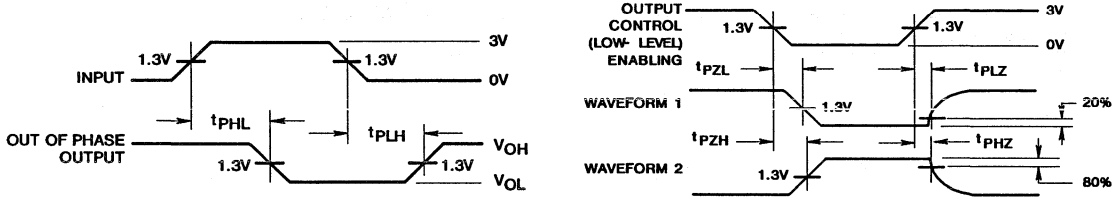


Fig. 2 - Timing diagrams

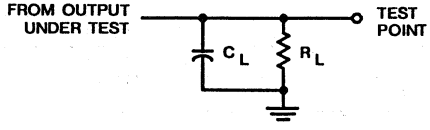


Fig. 3 - Load circuit for t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}.

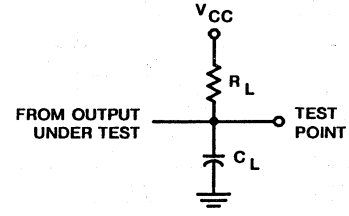


Fig. 4 - Load circuit for t_{PZL}, t_{PLZ}.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6	-	6	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6	-	-6	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.3	V
Input High Voltage	V_{IH}	-	$V_{CC}/2$	-	$V_{CC}/2$	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±50	-	±100	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	-	21	-	26	ns
	t_{PHL}	4.5	-	24	-	30	ns
Enable to Output	t_{PZL}	4.5	-	33	-	39	ns
	t_{PZH}	4.5	-	31	-	37	ns
Disable to Output	t_{PLZ}	4.5	-	33	-	33	ns
	t_{PHZ}	4.5	-	33	-	33	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS245MS	2-9	1, 10-19	20	-	10	1-9, 11-18, 19, 20
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS245MS	-	10	11-18	1, 20	2-9	19

NOTE: Each pin except 10, 20 and those designated as open shall have a resistor of 10kΩ ±5% for static and 680Ω ± 5% for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value
I_{OZL}	-1μA	-200nA
I_{OZH}	+1μA	+200nA

* All measurements will not exceed the absolute limit.

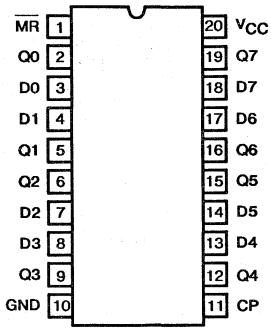
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
-	10	1-9, 11-18, 19, 20

NOTE:
Each pin except 10 and 20 shall have a resistor of 680Ω - 47kΩ.

HCS273MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Octal D Flip-Flop With Master Reset.

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 17ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCS273MS Octal D flip-flop with reset is positive edge triggered. This device utilizes advanced CMOS/SOS technology to achieve high-speed operation similar to LSTTL and QMOS while providing radiation hardness. The HCTS273MS is a member of a family of radiation-hardened, high speed, CMOS/SOS logic devices with either TTL or CMOS compatible.

The HCS273MS is presently supplied in a 20-lead weld-seal ceramic flatpack package (K suffix) or a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8 max., V_{IH} = V_{CC}/2 min.
  CMOS Input Current Levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

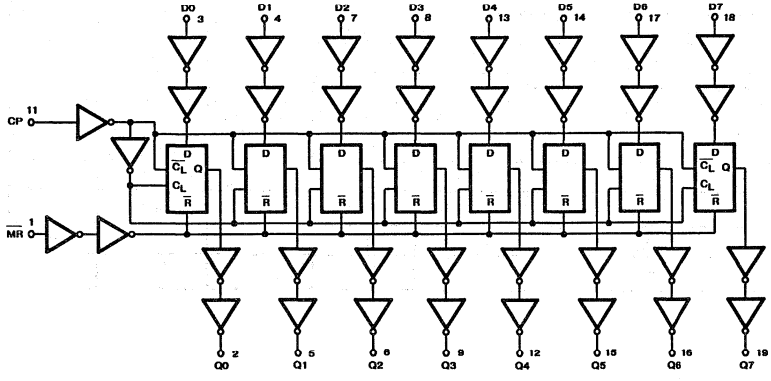


Figure 1 - Logic diagram.

TRUTH TABLE

INPUTS			OUTPUT
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Qo

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↑ = Transition from Low to High Level
NOTE: Qo = the level of Q established by the last low to high transition of the clock

12 LOGIC CIRCUITS

File Number **2475**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, Output (I/O) = $-0.5V < V_O < V_{DD} + 0.5V$ ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6.0	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC}$ -0.4V	-7.2	-	-6.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µ
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	TBE	-	TBE	pF

* Guaranteed but not tested.

**Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS			V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay		t_{PLH}	4.5	-	19	-	22	ns
	CP to Q	t_{PHL}	4.5	-	23	-	27	
	MR to Q	t_{PHL}	4.5	-	25	-	29	

	HCS
Input Level	V_{CC}
Switching Voltage, V_S	50% V_{CC}

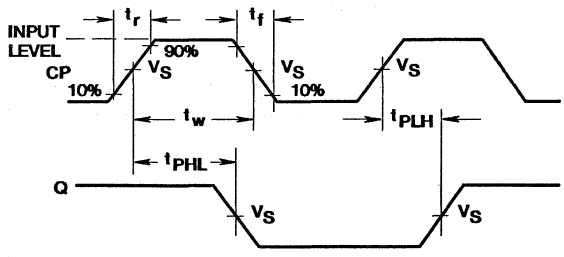


Figure 2 - Clock to output delays and clock pulse width.

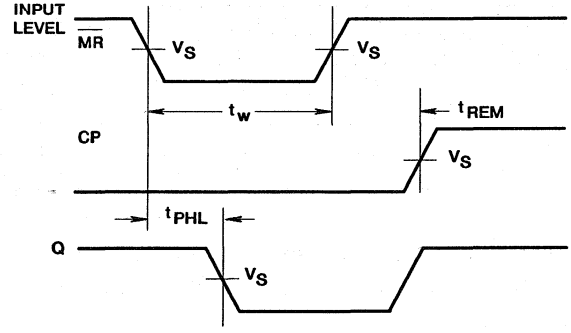


Figure 3 - Master reset pulse width. Master reset to output delay and master reset to clock recovery time.

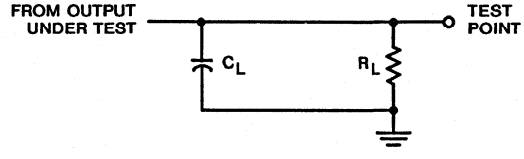


Figure 4 - Load circuit for t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = 125°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of radiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.12 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF

CHARACTERISTICS			V_{CC} (V)	LIMITS				UNITS
				200k Rads (Si)		1M Rads (Si)		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delay		t_{PLH}	4.5	-	22	-	28	ns
	CP to Q	t_{PHL}	4.5	-	27	-	34	
	MR to Q	t_{PHL}	4.5	-	29	-	37	

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS273MS	2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	20	2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20
Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCS273MS	-	10	2, 5, 6, 9, 12, 15, 16, 19	1, 20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTE: Each pin except 10 and 20 shall have a resistor of 10kΩ ± 5% for Static and 680V ± 5% Dynamic Burn-In.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{DD}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

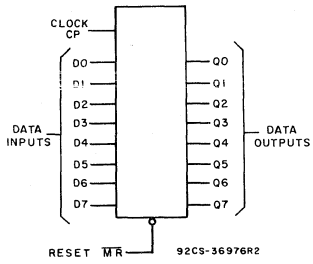
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

NOTE: Each pin except 10 and 20 shall have a resistor of 680Ω - 47kΩ.

HCTS273MS



FUNCTIONAL DIAGRAM

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Octal D Flip-Flop with Master Reset.

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Positive-edge triggering*
- *Typical propagation delay = 17ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs*

The HCTS273MS octal D flip-flop with reset is positive edge triggered. This device utilizes advanced CMOS/SOS technology to achieve high-speed operation similiar to LSTTL and QMOS while providing radiation-hardness. The HCTS273MS is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs.

The HCTS273MS is presently supplied in a 20-lead weld-seal ceramic flatpack package (K suffix) or a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8 max., V_{IH} = V_{DD}/2 min.
  CMOS Input Compatibility
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

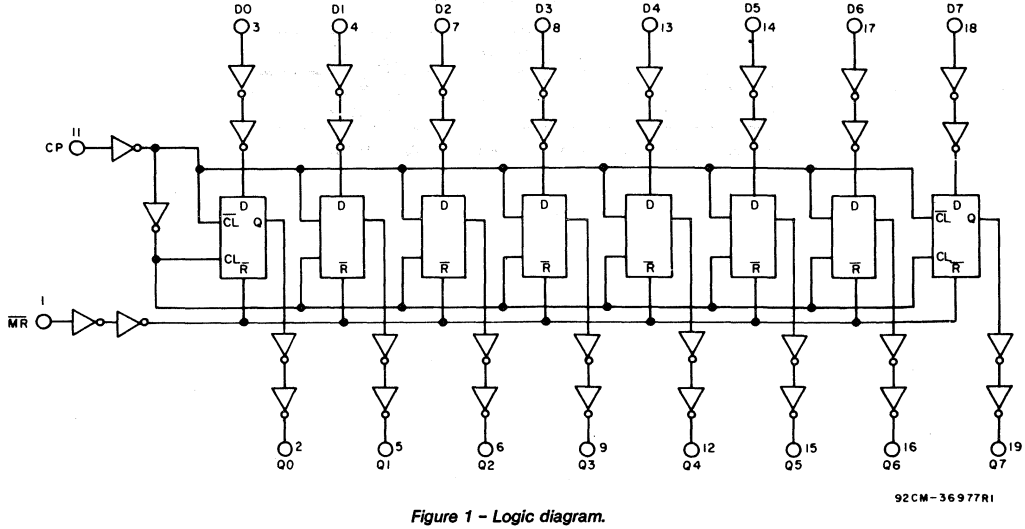


Figure 1 - Logic diagram.

File Number **2274**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100° C ..... 500 mW
For T_A = +100 to +125° C ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125° C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

OPERATING CONDITIONS at T_A = -55° C to +125° C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25° C		-55° C/+125° C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	40	—	750	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	7.2	—	6	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-7.2	—	-6	—	
Low-Level Output Voltage	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Low-Level Input Voltage	V_{IL}	—	—	0.8	—	0.8	
High-Level Input Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±0.5	—	±5	μA
Input Capacitance	C_{IN}*	—	—	10	—	10	pF
Power Dissipation Capacitance	C_{PD}*	—	—	40	—	40	

*Characterized but not tested.

TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Q
L	X	X	L
H	↗	H	H
H	↗	L	L
H	L	X	Q0

H = High level (steady state).
L = Low level (steady state).
X = Irrelevant
↗ = Transition from LOW-to-HIGH level.
Q0 = The level of Q established by the last LOW-to-HIGH transition of the CLOCK.

SWITCHING CHARACTERISTICS, V_{CC} = 4.5 V, t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		LIMITS				UNITS
		+25°C		-55°C/+125°C		
		MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	—	19	—	22	ns
CP to Q	t_{PHL}	—	23	—	27	
$\overline{MR}$ to Q	t_{PHL}	—	25	—	29	

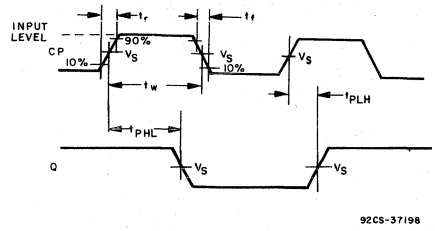


Fig. 2 - Clock to output delays and clock pulse width.

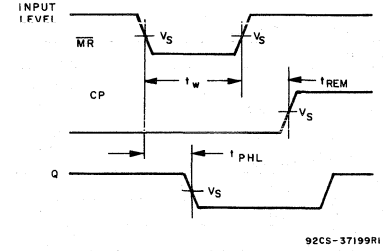


Fig. 3 - Master reset pulse width. Master reset to output delay and master reset to clock recovery time.

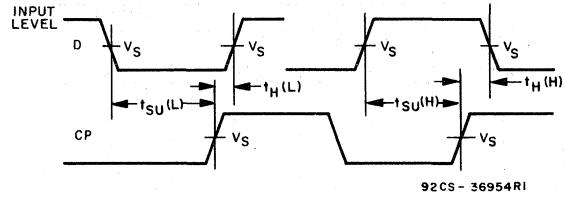


Fig. 4 - Data setup and hold times.

	HCTS
Input Level	3 V
Switching Voltage, V_S	1.3 V

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20-ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rad (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.75	—	2	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	6	—	5	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-6	—	-5	—	
Low-Level Output Voltage	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Low-Level Input Voltage	V_{IL}	—	—	0.8	—	0.3	
High-Level Input Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA

•Guaranteed but not tested.

SWITCHING CHARACTERISTICS, V_{CC} = 4.5 V, t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		LIMITS				UNITS
		200k Rads (Si)		1M Rad (Si)		
		MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	—	22	—	28	ns
CP to Q	t_{PHL}	—	27	—	34	
$\overline{MR}$ to Q	t_{PHL}	—	29	—	37	

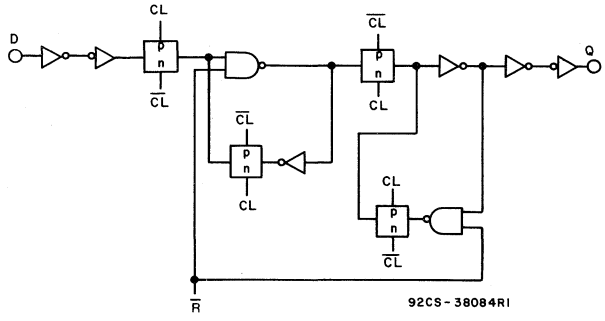
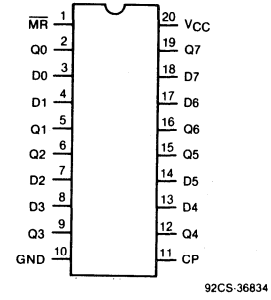


Fig. 5 - Flip-flop detail.



TERMINAL ASSIGNMENT

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCTS273MS	2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	20	2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

Dynamic Burn-In Test-Circuit Connections						
TYPE	OPEN	GROUND	½ V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR	
					50 kHz	25 kHz
HCTS273MS	—	10	2, 5, 6, 9, 12, 15, 16, 19	1, 20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTE: Each pin except 10 and 20 shall have a resistor of 680 Ω - 47 kΩ.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40 μA	+12 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value

*All measurements will not exceed the absolute limit.

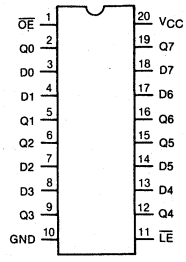
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

NOTE:
Each pin except 10 and 20 shall have a resistor of 680 Ω - 47 kΩ.

HCS373MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Octal Transparent Latch, 3-State

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 12ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-state outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCS373MS is a radiation-hardened octal transparent 3-state latch with an active-low output enable. The HCS373MS utilizes advanced CMOS/SOS technology. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The HCS373MS is supplied in a 20-lead weld-seal flatpack package (K suffix) or a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to TTL logic ICs*
- *HCS types:*
  High noise immunity:
  V_{IL} max. = 30% of V_{CC}
  V_{IL} min. = 70% of V_{CC}

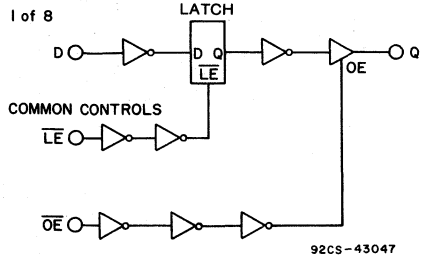


Figure 1 - Logic Diagram.

TRUTH TABLE

$\overline{OE}$ OUTPUT ENABLE	$\overline{LE}$ LATCH ENABLE	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance State
l = Low voltage level prior to the high-to-low latch enable transition
h = High voltage level prior to the high-to-low latch enable transition

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, Output (I/O) - $-0.5\ V < V_O < V_{DD} + 0.5\ V$ ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C/+125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	40	—	750	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	7.2	—	6	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-7.2	—	-6	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1	—	V_{CC}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.3 V_{CC}	—	0.3 V_{CC}	
Input High Voltage	V_{IH}	—	0.7 V_{CC}	—	0.7 V_{CC}	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±0.5	—	±5	μA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0 V or V_{CC}	—	±1	—	±50	
Input Capacitance	C_{IN}*	—	—	10	—	10	pF
Output Capacitance	C_{OUT}*	—	—	10	—	10	
Power Dissipation Capacitance	C_{PD}**	—	—	38	—	38	

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	20	-	24	ns
Data to Qn	t_{PHL}	4.5	-	20	-	24	ns
LE to Qn	t_{PLH}	4.5	-	24	-	29	ns
	t_{PHL}	4.5	-	24	-	29	ns
Enable to Output	t_{PZL}	4.5	-	25	-	31	ns
	t_{PZH}	4.5	-	20	-	24	ns
Disable to Output	t_{PLZ}	4.5	-	25	-	30	ns
	t_{PHZ}	4.5	-	25	-	30	ns

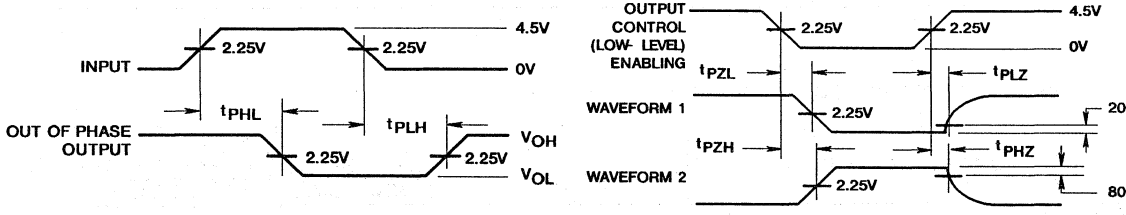


Figure 2 - Timing diagrams.

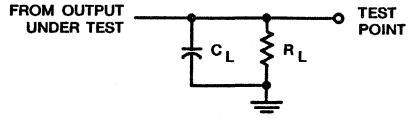


Figure 3 - Load circuit for t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}.

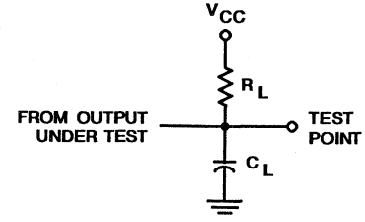


Figure 4 - Load circuit for t_{PZL}, t_{PLZ}.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION† PERFORMANCE at T_A = +25°C

†Radiation measurements are made on 4 samples/wafer. The limits shown are for within 1 hour of radiating.

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.75	—	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	6	—	5	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-6	—	-5	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1	—	V_{CC}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.3 V_{CC}	—	0.12V_{CC}	
Input High Voltage	V_{IH}	—	0.7 V_{CC}	—	0.7 V_{CC}		
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0 V or V_{CC}	—	±50	—	±100	

SWITCHING CHARACTERISTICS, t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:	t_{PLH}	4.5	—	24	—	29	ns
Data to Qn	t_{PHL}	4.5	—	24	—	29	
$\overline{LE}$ to Qn	t_{PLH}	4.5	—	29	—	37	
	t_{PHL}	4.5	—	29	—	37	
Enable to Output	t_{PZL}	4.5	—	31	—	39	
	t_{PZH}	4.5	—	24	—	30	
Disable to Output	t_{PLZ}	4.5	—	30	—	38	
	t_{PHZ}	4.5	—	30	—	38	

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCS373MS	2, 5, 6, 9 12, 15, 16, 19	1, 3, 4, 7, 8 10, 11, 13, 14 17, 18	20	2, 5, 6, 9 12, 15, 16, 19	10	1, 3, 4, 7, 8 11, 13, 14, 17 18, 20
Dynamic Burn-In Test-Circuit Connections						
TYPE	OPEN	GROUND	½ V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR	
					50 kHz	25 kHz
HCS373MS	—	1, 10	2, 5, 6, 9 12, 15, 16, 19	20	11	3, 4, 7, 8 13, 14, 17, 18

NOTE: Each pin except 10 and 20 and those designated as open shall have a resistor of 10kΩ ±5% for static and 680kΩ ±5% dynamic.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40 μA	+12 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value
I_{OZL} I_{OZH}	-1 μA +1 μA	-200 nA +200 nA

*All measurements will not exceed the absolute limit.

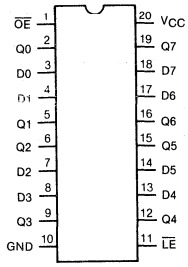
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Test I
II	Initial Electrical Tests	Interim Electrical Test II
III	Initial Electrical Tests	Interim Electrical Test III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
2, 5, 6, 9 12, 15, 16, 19	10	1, 3, 4, 7 8, 11, 13, 14 17, 18, 20

NOTE:
Each pin except 10, 20 and those designated as open shall have a resistor of 680 Ω - 47 kΩ.

HCTS373MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Octal Transparent Latch, 3-State

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2×10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 17ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-state outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCTS373MS is a radiation-hardened octal transparent 3-state latch with an active-low output enable. The HCTS373MS utilizes advanced CMOS/SOS technology. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The HCTS373MS is supplied in a 20-lead weld-seal flatpack package (K suffix) and a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to TTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{CC}/2 min.
  CMOS Input Current Levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

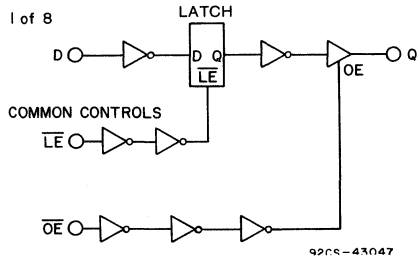


Figure 1 - Logic Diagram.

TRUTH TABLE

$\overline{\text{OUTPUT ENABLE}}$	$\overline{\text{LATCH ENABLE}}$	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance State
l = Low voltage level prior to the high-to-low latch enable transition
h = High voltage level prior to the high-to-low latch enable transition

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, Output (I/O) = $-0.5\ V < V_O < V_{DD} + 0.5\ V$ ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V

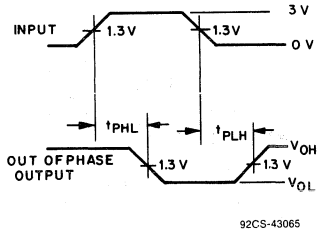
STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C/+125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	40	—	750	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	7.2	—	6	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-7.2	—	-6	—	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1	—	V_{CC}-0.1	—	V
Input Low Voltage	V_{IL}	—	—	0.8	—	0.8	V
Input High Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	V
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±0.5	—	±5	μA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0 V or V_{CC}	—	±1	—	±50	μA
Input Capacitance	C_{IN}*	—	—	10	—	10	pF
Output Capacitance	C_{OUT}*	—	—	10	—	10	pF
Power Dissipation Capacitance	C_{PD}**	—	—	38	—	38	pF

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delays: Data to Qn	t_{PLH}	4.5	—	19	—	24	ns
	t_{PHL}	4.5	—	26	—	30	
$\overline{LE}$ to Qn	t_{PLH}	4.5	—	27	—	30	
	t_{PHL}	4.5	—	30	—	34	
Enable to Output	t_{PZL}	4.5	—	32	—	36	
	t_{PZH}	4.5	—	26	—	29	
Disable to Output	t_{PLZ}	4.5	—	22	—	25	
	t_{PHZ}	4.5	—	22	—	25	



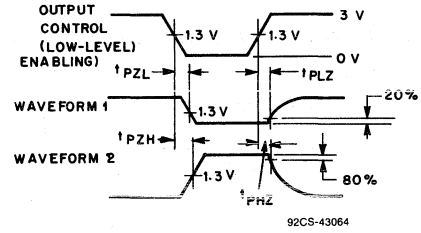


Fig. 2 - Timing diagrams.

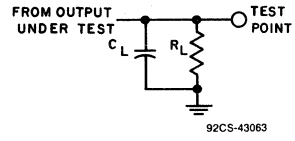


Fig. 3 - Load circuit for t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}.

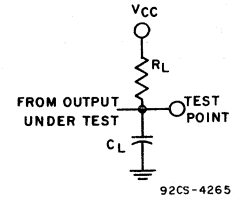


Fig. 4 - Load circuit for t_{PZL}, t_{PLZ}.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION† PERFORMANCE at T_A = +25°C

†Radiation measurements are made on 4 samples/wafer. The limits shown are for within 1 hour of radiating.

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.75	—	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	6	—	5	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-6	—	-5	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1	—	V_{CC}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.8	—	0.4	
Input High Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0 V or V_{CC}	—	±50	—	±100	

SWITCHING CHARACTERISTICS, t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:	t_{PLH}	4.5	—	24	—	30	ns
Data to Qn	t_{PHL}	4.5	—	30	—	38	
$\overline{LE}$ to Qn	t_{PLH}	4.5	—	30	—	38	
	t_{PHL}	4.5	—	34	—	43	
Enable to Output	t_{PZL}	4.5	—	36	—	45	
	t_{PZH}	4.5	—	29	—	37	
Disable to Output	t_{PLZ}	4.5	—	25	—	32	
	t_{PHZ}	4.5	—	25	—	32	

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCTS373MS	2, 5, 6, 9 12, 15, 16, 19	1, 3, 4, 7, 8 10, 11, 13, 14 17, 18	20	2, 5, 6, 9 12, 15, 16, 19	10	1, 3, 4, 7, 8 11, 13, 14, 17 18, 20

Dynamic Burn-In Test-Circuit Connections						
TYPE	OPEN	GROUND	½ V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR	
					50 kHz	25 kHz
HCTS373MS	—	1, 10	2, 5, 6, 9 12, 15, 16, 19	20	11	3, 4, 7, 8 13, 14, 17, 18

NOTE: Each pin except 10 and 20 and those designated as open shall have a resistor of 10kΩ ±5% for static and 680kΩ ±5% dynamic.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40 μA	+12 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value
I_{OZL}	-1 μA	-200 nA
I_{OZH}	+1 μA	+200 nA

*All measurements will not exceed the absolute limit.

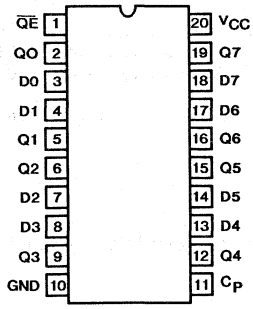
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests iii

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
2, 5, 6, 9 12, 15, 16, 19	10	1, 3, 4, 7 8, 11, 13, 14 17, 18, 20

NOTE:
Each pin except 10, 20 and those designated as open shall have a resistor of 680 Ω - 47 kΩ.

HCS374MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Octal D-Type Flip-Flop Positive Edge Trigger, 3-State

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 18ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-State outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCS374MS is a radiation-hardened non-inverting octal D-type, positive-edge triggered flip-flop with tristatable outputs. The HCS374MS utilizes advanced CMOS/SOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). Data is also transferred to the outputs during this transition. The output enable ($\overline{OE}$) controls the 3-state outputs and is independant of the register operation. When the output enable is high, the outputs are in the high-impedance state.

The HCS374MS is supplied in a 20-lead weld-seal flatpack package (K suffix) or a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to TTL logic ICs*
- *HCS types:*
  High Noise Immunity
  V_{IL} = 30% V_{CC}
  V_{IH} = 70% V_{CC}

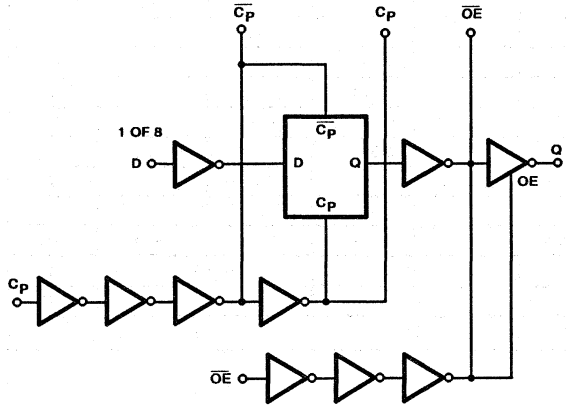


Figure 1 - Logic diagram.

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	CP	Dn	Qn
L	↑	H	H
L	↑	L	L
L	X	X	Q0
H	X	X	Z

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
Z = High Impedance
↑ = Transition from Low to High Level

NOTE: Q0 = the level of Q before the indicated input conditions were established.

File Number 2470

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, Output (I/O) = $-0.5V < V_O < V_{CC} + 0.5V$ ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

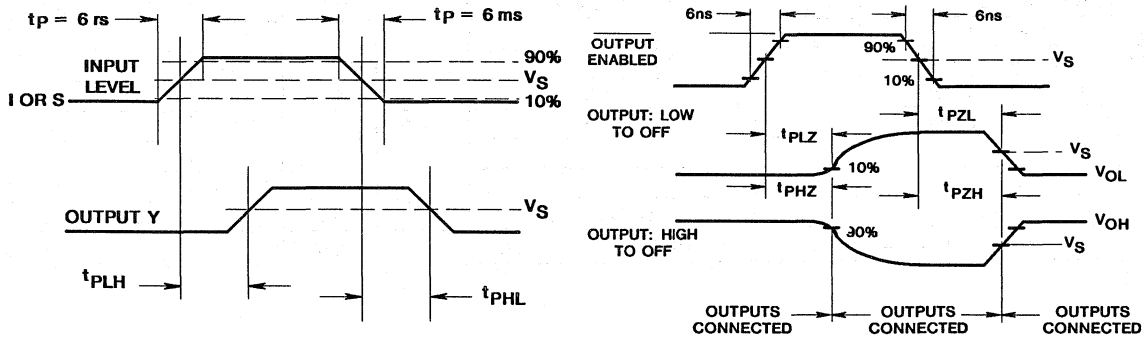
STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6.0	-	mA
Output (Source) Current	I_{OH}	$V_{OUT} = V_{CC} - 0.4V$	-7.2	-	-6.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 VCC	-	0.3 VCC	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±1	-	±50	µA
Input Capacitance	C_{IN}*	-	10		10		pF
Output Capacitance	C_{OUT}*	-	10		10		pF
Power Dissipation Capacitance	C_{PD}**	-	7		23		pF

* Characterized but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	22	-	26	ns
Clock to Q	t_{PHL}	4.5	-	22	-	26	ns
Enable to Output	t_{PZL}	4.5	-	20	-	23	ns
	t_{PZH}	4.5	-	20	-	23	ns
Disable to Output	t_{PLZ}	4.5	-	20	-	22	ns
	t_{PHZ}	4.5	-	18	-	20	ns



Input Level	V_{CC}
Switching Voltage, V_S	50% V_{CC}

Figure 2 - Transition and propagation delay times.

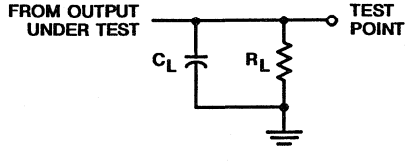


Figure 3 - Load circuit for tPLH, tPHL, tPZH, tPHZ.

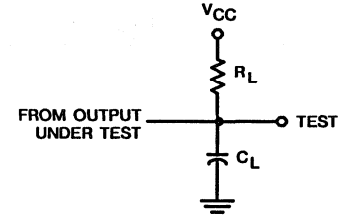


Figure 4 - Load circuit for tPZL, tPLZ.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s

POST-RADIATION † PERFORMANCE at $T_A = +25^oC$

† Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of radiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.12 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0V or V_{CC}	-	±50	-	±100	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS 200k Rads (Si) MIN.	LIMITS 200k Rads (Si) MAX.	LIMITS 1M Rads (Si) MIN.	LIMITS 1M Rads (Si) MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	26	-	33	ns
	t_{PHL}	4.5	-	26	-	33	ns
Enable to Output	t_{PZL}	4.5	-	23	-	29	ns
	t_{PZH}	4.5	-	20	-	25	ns
Disable to Output	t_{PLZ}	4.5	-	22	-	28	ns
	t_{PHZ}	4.5	-	20	-	25	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS374MS	2, 5, 6, 9, 12, 15, 16, 18	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	20	2, 5, 7, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11 13, 14, 17, 18, 20

Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCS374MS	-	1, 10	2, 5, 6, 9, 12, 15, 16, 19	20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTE: Each pin except 10, 20 and those designated as open shall have a resistor of 10kΩ ±5% for static and 680Ω ±5% for dynamic.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value
I_{OZL}	-1μA	-200nA
I_{OZH}	+1μA	+200nA

* All measurements will not exceed the absolute limit.

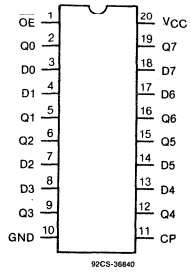
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13 14, 17, 18, 20

NOTE: Each pin except 10, 20 and those designated as open shall have a resistor of 680Ω - 47kΩ.

HCTS374MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Octal D-Type Flip-Flop Positive Edge Trigger, 3-State

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 18ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-State outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCTS374MS is a radiation-hardened non-inverting octal D-type, positive-edge triggered flip-flop with tristatable outputs. The HCTS374MS utilizes advanced CMOS/SOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). Data is also transferred to the outputs during this transition. The output enable (OE) controls the 3-state outputs and is independant of the register operation. When the output enable is high, the outputs are in the high-impedance state.

The HCTS374MS is supplied in a 20-lead weld-seal flatpack package (K suffix) or a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to TTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{CC}/2 min.
  CMOS Input Current Levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

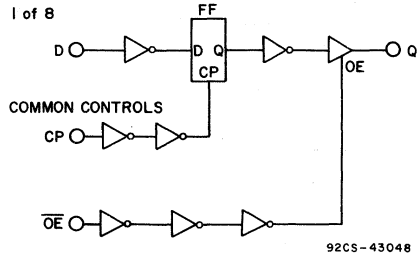


Figure 1 - Logic diagram.

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	CP	Dn	Qn
L	⎍	H	H
L	⎍	L	L
L	L	X	Q0
H	X	X	Z

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
Z = High Impedance
⎍ = Transition from Low to High Level

NOTE: Q0 = the level of Q before the indicated input conditions were established.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, Output (I/O) = -0.5V < V_O < V_{DD} +0.5V ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR K PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C

For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V

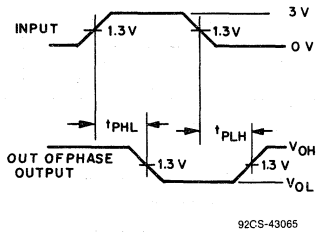
STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C/+125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	40	—	750	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	7.2	—	6.0	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4 V	-7.2	—	-6.0	—	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	V
Input Low Voltage	V_{IL}	—	—	0.8	—	0.8	V
Input High Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	V
Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{CC}	—	±0.5	—	±5	μA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0 V or V_{CC}	—	±1	—	±50	μA
Input Capacitance	C_{IN} •	—	—	10	—	10	pF
Output Capacitance	C_{OUT} •	—	—	10	—	10	pF
Power Dissipation Capacitance	C_{PD} ••	—	—	40	—	40	pF

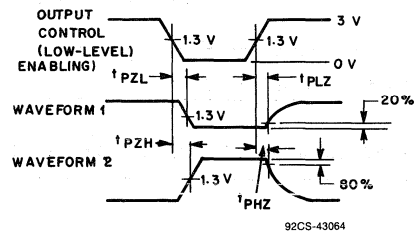
• Guaranteed but not tested.
•• Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS t_r, t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		V_{CC}	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5 V	—	27	—	31	ns
Clock to Q	t_{PHL}	4.5 V	—	31	—	35	
Enable to Output	t_{PZL}	4.5 V	—	32	—	36	
	t_{PZH}	4.5 V	—	26	—	29	
Disable to Output	t_{PLZ}	4.5 V	—	22	—	25	
	t_{PHZ}	4.5 V	—	22	—	25	



(a)



(b)

Fig. 2 - Timing diagrams.

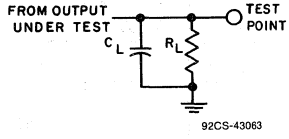


Fig. 3 - Load circuit for t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}.

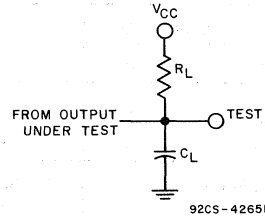


Fig. 4 - Load circuit for t_{PZL}, t_{PLZ}.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ Rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ Rads (Si)/s

POST-RADIATION † PERFORMANCE at T_A = +25°C

† Radiation measurements are made on 4 samples/wafer. The limits shown are for within 1 hour of radiating.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k RADS (Si)		1M RADS (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.75	—	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	6.0	—	5.0	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4 V	-6.0	—	-5.0	—	
Output Voltage, Low Level	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1	—	
Input Low Voltage	V_{IL}	—	—	0.8	—	0.4	
Input High Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA
3-State Output Leakage Current	I_{OZ}	Applied Voltages = 0 V or V_{CC}	—	±50	—	±100	

SWITCHING CHARACTERISTICS t_r, t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		V_{CC}	LIMITS				UNITS
			200k RADS (Si)		1M RADS (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5 V	—	31	—	39	ns
Clock to Q	t_{PHL}	4.5 V	—	35	—	44	
Enable to Output	t_{PZL}	4.5 V	—	36	—	45	
	t_{PZH}	4.5 V	—	29	—	37	
Disable to Output	t_{PLZ}	4.5 V	—	25	—	32	
	t_{PHZ}	4.5 V	—	25	—	32	

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCTS374MS	2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	20	2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

Dynamic Burn-In Test-Circuit Connections						
TYPE	OPEN	GROUND	1/2 V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR 50 kHz	OSCILLATOR 25 kHz
HCTS374MS	—	1, 10	2, 5, 6, 9, 12, 15, 16, 19	20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTE: Each pin except 10 and 20 and those designated as open shall have a resistor of 10kΩ ±5% for static and 680kΩ ±5% dynamic.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT *	DELTA LIMIT
I_{CC}	40 μA	+12 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value
I_{OZL}	-1 μA	-200 nA
I_{OZH}	+1 μA	+200 nA

DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

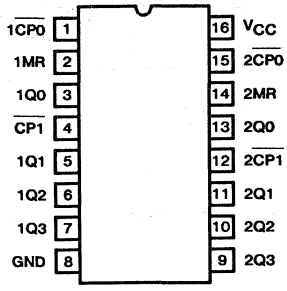
* All measurements will not exceed the absolute limit.

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

Note: Each pin except 10, 20 and those designated as open shall have a resistor of 680 Ω - 47 kΩ.

HCTS390MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Dual Decade Ripple Counter

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 20ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *Buffered inputs*

The HCTS390MS is a dual decade ripple counter. The HCTS390 utilizes advanced CMOS/SOS technology to chieve high-speed operation similar to LSTTL and QMOS while providing radiation-hardeness. The HCTS390 is a member of a family of radiation-hardened, high speed, CMOS/SOS logic devices with either TTL or CMOS compatible inputs which are available.

The HCTS390MS is presently supplied in a 16-lead weld-seal ceramic flatpack package (K suffix) and in a 16-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus-driver outputs - 15 LSTTL loads
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL input logic compatibility
  V_{IL} = 0.8V max., V_{IH} = V_{DD}/2 min.
  CMOS input current levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS		ACTION
CP	MR	
⎍	L	No Change
⎍	L	Count
H	H	All Qs Low

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
⎍ = LOW-to-HIGH ϕ transition
⎍ = HIGH-to-LOW ϕ transition

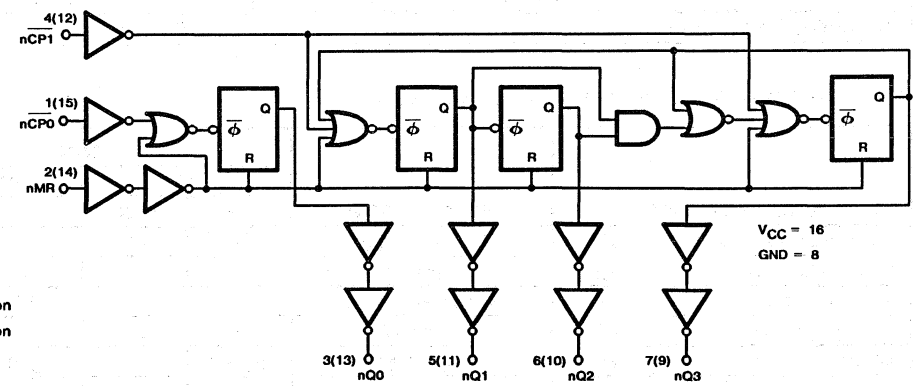


Figure 1 - Logic Diagram.

BCD COUNTER SEQUENCE FOR ½ THE "390"

COUNT	OUTPUTS Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output nQ0 connected to nCP1 with counter input on nCP0.

BI-QUINARY COUNT SEQUENCE FOR ½ THE "390"

COUNT	OUTPUTS Q0	Q1	Q2	Q3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

NOTE: Output nQ3 connected to nCP0 with counter input on nCP1.

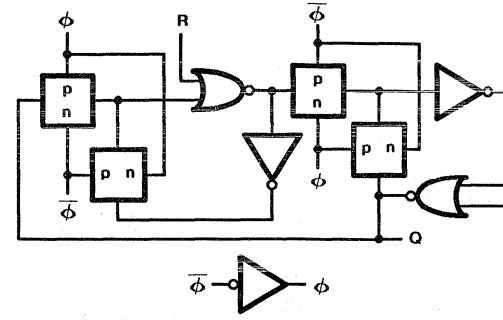


Figure 2 - Flip-flop logic detail.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS MIN.	MAX.	UNITS
DC Operating-Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS +25°C MIN.	+25°C MAX.	-55°C to +125°C MIN.	-55°C to +125°C MAX.	UNITS
Quiescent Device Current	I_{DD}	V_{IN} = 0V or V_{DD}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-7.2	-	-6.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{DD} -0.1	-	V_{DD} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.8	-	0.8	V
Input High Voltage	V_{IH}	-	V_{DD}/2	-	V_{DD}/2	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}*	-	-	TBE	-	TBE	pF

* Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF

CHARACTERISTICS		V_{DD} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PHL}	4.5	-	19	-	24	ns
nCP0 to nQ0	t_{PLH}	4.5	-	18	-	23	ns
Propagation Delay	t_{PHL}	4.5	-	26	-	32	ns
nCP1 to nQ1	t_{PLH}	4.5	-	26	-	32	ns
Propagation Delay	t_{PHL}	4.5	-	31	-	38	ns
nCP1 to nQ2	t_{PLH}	4.5	-	30	-	37	ns
Propagation Delay	t_{PHL}	4.5	-	26	-	32	ns
nCP1 to nQ3	t_{PLH}	4.5	-	26	-	32	ns
Propagation Delay*	t_{PHL}	4.5	-	50	-	62	ns
nCP0 to nQ2 †	t_{PLH}	4.5	-	48	-	60	ns
Propagation Delay MR to Qn	t_{PHL}	4.5	-	20	-	26	ns
Input Capacitance*	Ci	-	-	10	-	-	pF

*Guaranteed, but not tested.
† nQ0 tied to nCP1

POST RADIATION LIMITS, t_r, t_f = 3ns, C_L = 50pF

CHARACTERISTICS		V_{DD} (V)	LIMITS POST 200k MIN.	LIMITS POST 200k MAX.	LIMITS POST 1M MIN.	LIMITS POST 1M MAX.	UNITS
Propagation Delay	t_{PHL}	4.5	-	24	-	30	ns
nCP0 to nQ0	t_{PLH}	4.5	-	23	-	29	ns
Propagation Delay	t_{PHL}	4.5	-	32	-	40	ns
nCP1 to nQ1	t_{PLH}	4.5	-	32	-	40	ns
Propagation Delay	t_{PHL}	4.5	-	38	-	48	ns
nCP1 to nQ2	t_{PLH}	4.5	-	37	-	46	ns
Propagation Delay	t_{PHL}	4.5	-	32	-	40	ns
nCP1 to nQ3	t_{PLH}	4.5	-	32	-	40	ns
Propagation Delay*	t_{PHL}	4.5	-	62	-	78	ns
nCP0 to nQ2 †	t_{PLH}	4.5	-	60	-	74	ns
Propagation Delay MR to Qn	t_{PHL}	4.5	-	26	-	33	ns
Input Capacitance*	Ci	-	-	10	-	-	pF

*Guaranteed, but not tested.
† nQ0 tied to nCP1

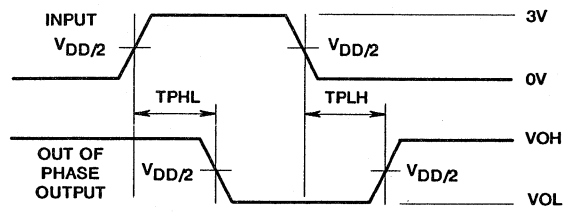


Figure 3 - Timing waveform.

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCTS390MS	3, 5, 6, 7	1, 2, 4, 8, 10, 12, 14, 15	16	3, 5, 6, 7 9, 10, 11, 13	8	1, 2, 4, 12 14, 15, 16

Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCTS390MS	-	8	3, 5, 6, 7, 9, 10, 11, 13	2, 14, 16	1, 4, 12, 15	-

NOTE: Each pin except 8 and 16 shall have a resistor of 10kΩ ±5% for static and 680Ω ±5% for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{DD}	40μA	+12μA
I_{OL} and I_{OH}	-	-15% of 0 hr. value

* All measurements will not exceed the absolute limit.

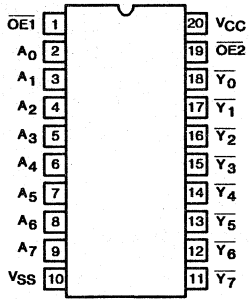
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
3, 5, 6, 7, 9, 10, 11, 13	8	1, 2, 4, 12, 14, 15, 16

NOTE: Each pin except 8 and 16 shall have a resistor of 680Ω - 47kΩ.

HCTS540MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS Inverting Octal Buffer/Line Driver, 3-State

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 18ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-State outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCTS540MS is a radiation hardened non-inverting octal buffer/line driver with two active low output enables. The output enable pins, $\overline{OE1}$ and $\overline{OE2}$ control the 3-state outputs. If either $\overline{OE1}$ or $\overline{OE2}$ is HIGH the outputs will be in the high impedance state. For data output both $\overline{OE1}$ and $\overline{OE2}$ must be LOW.

The HCTS540MS is supplied in a 20-lead weld-seal flatpack package (K suffix) or a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus Driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibility
  V_{IL} = 0.8 max., V_{IH} = V_{CC}/2 min.
  CMOS Input Current Levels
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

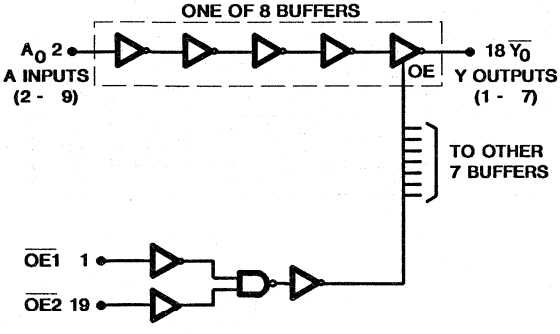


Figure 1 - Logic Diagram.

TRUTH TABLE

$\overline{OE1}$	$\overline{OE2}$	A_n	OUTPUT
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100° C ..... 500 mW
For T_A = +100 to +125° C ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

OPERATING CONDITIONS at T_A = -55° C to +125° C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25° C		-55° C/+125° C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	40	—	750	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	7.2	—	6	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-7.2	—	-6	—	
Low-Level Output Voltage	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Low-Level Input Voltage	V_{IL}	—	—	0.8	—	0.8	
High-Level Input Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±0.5	—	±5	μA
3-State Output Leakage Current	I_{OZ}	Applied V = 0 V or V_{CC}	—	±1	—	±50	
Input Capacitance	C_{IN}*	—	—	10	—	10	pF
Output Capaciitance	C_{OUT}*	—	—	10	—	10	
Power Dissipation Capacitance	C_{PD}**	—	—	30	—	30	

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Propagation Delay	t_{PLH}	4.5	-	21	-	25	ns
	t_{PHL}	4.5	-	21	-	25	ns
Enable to Output	t_{PZL}	4.5	-	30	-	35	ns
	t_{PZH}	4.5	-	26	-	30	ns
Disable to Output	t_{PLZ}	4.5	-	26	-	30	ns
	t_{PHZ}	4.5	-	26	-	30	ns

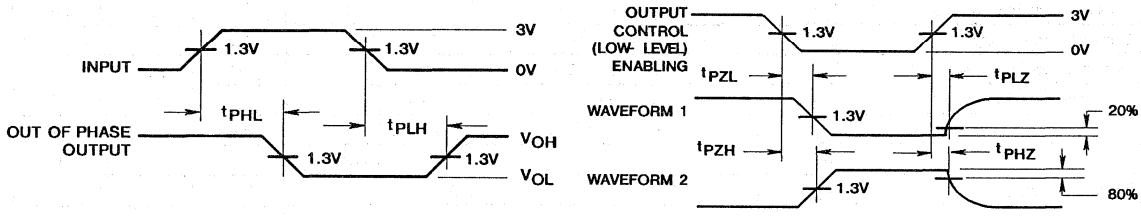


Figure 2 - Timing diagrams.

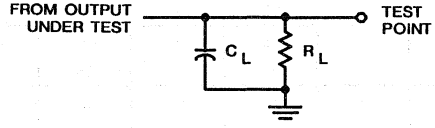


Figure 3 - Load circuit for t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}.

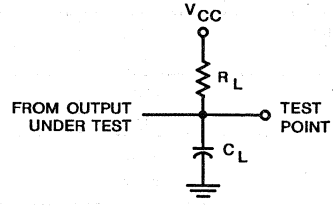


Figure 4 - Load circuit for t_{PZL}, t_{PLZ}.

INHERENT PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±5	-	±5	µA
Output Leakage Current	I_{OZ}	V_O = 0V or V_{CC}	-	±50	-	±100	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay	t_{PLH}	4.5	-	25	-	32	ns
	t_{PHL}	4.5	-	25	-	32	ns
Enable to Output	t_{PZL}	4.5	-	35	-	44	ns
	t_{PZH}	4.5	-	30	-	38	ns
Disable to Output	t_{PLZ}	4.5	-	30	-	38	ns
	t_{PHZ}	4.5	-	30	-	38	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCTS540MS	11-18	1-10,19	20	11-18	10	1-9,19,20

Dynamic Burn-In Test-Circuit Connections						
TYPE	OPEN	GROUND	½ V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR	
					50 kHz	25 kHz
HCTS540MS	—	10	11-18	20	1,19	2-9

NOTE: Each pin except 10 and 20 shall have a resistor of 10kΩ ±5% for static and 680kΩ ±5% dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40 μA	+12 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value
I_{OZL}	-1 μA	-200 nA
I_{OZH}	+1 μA	+200 nA

*All measurements will not exceed the absolute limit.

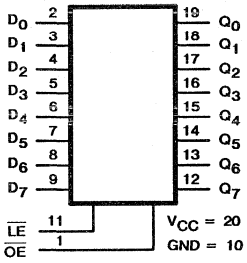
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
11-18	10	1-9,19,20

NOTE:
Each pin except 10 and 20 shall have a resistor of 680 Ω - 47 kΩ.

HCS573MS



TERMINAL ASSIGNMENT

High-Reliability Radiation-Hardened High-Speed CMOS/SOS Octal Transparent Latch 3 State Output

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

The HCS573MS is a radiation-hardened octal transparent latch with 3 state outputs. The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the 3 state outputs. When the ($\overline{OE}$) is high the outputs are in a high impedance state. The latch operation is independant of the output enable.

The HCS573MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS logic family with either TTL or CMOS input compatibility.

The HCS573MS is supplied in a 20-lead weld-seal ceramic flatpack package (K suffix) or a dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus-driver outputs - 15 LSTTL loads
- *Wide operating-temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCS types:*
  4.5V to 5.5V operation
  CMOS Input Logic Compatibility
  V_{IL} = 0.3V_{CC} max., V_{IH} = 0.7V_{CC} min.
  CMOS Input Current Level
  $I_I \leq 5\mu A$ @ V_{OL}, V_{OH}

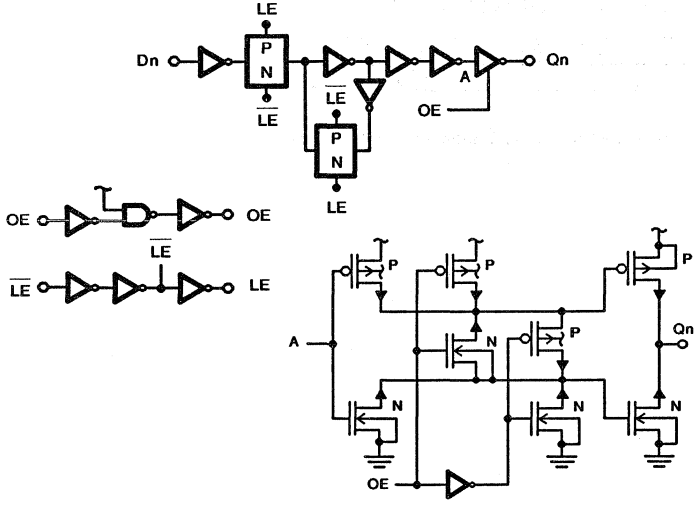


Figure 1 - Logic Diagram.

TRUTH TABLE

$\overline{\text{OUTPUT ENABLE}}$	$\overline{\text{LATCH ENABLE}}$	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

L = Low Voltage Level
H = High Voltage Level
l = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition
X = Don't Care
Z = High Impedance State

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C 500mW
For T_A = +100 to +125°C ..... Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating-Voltage Range	4.5	5.5	V

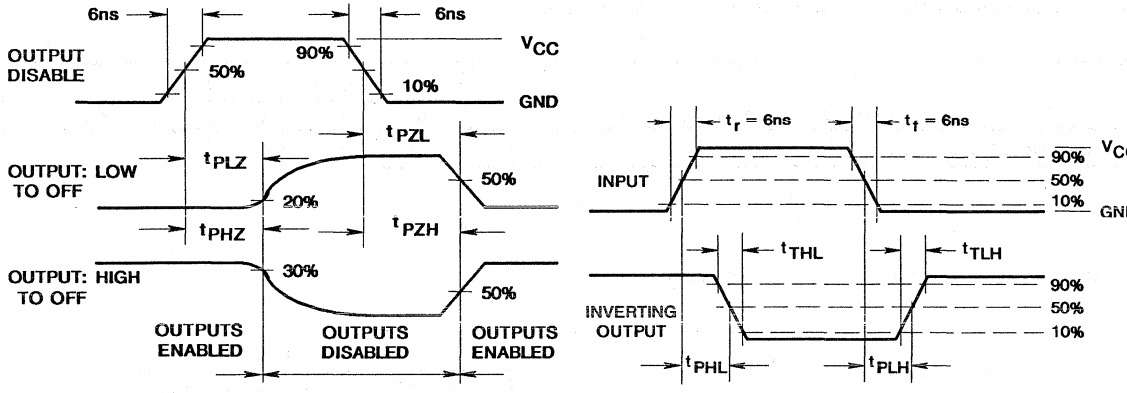
STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ± 10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			+25°C		-55°C to +125°C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	40	-	750	µA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	7.2	-	6.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-7.2	-	-6.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.3 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA
Input Capacitance	C_{IN}*	-	-	10	-	10	pF
Output Capacitance	C_{OUT}*	-	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}**	-	-	10	-	10	pF

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS -55°C to +125°C MIN.	LIMITS -55°C to +125°C MAX.	UNITS
Data to Qn Output	t_{PLH}	4.5	-	24	-	29	ns
Data to Qn Output	t_{PHL}	4.5	-	24	-	29	ns
LE to Qn Output	t_{PLH}	4.5	-	27	-	35	ns
LE to Qn Output	t_{PHL}	4.5	-	31	-	40	ns
Output Enabling Time	t_{PZL}	4.5	-	27	-	33	ns
Output Enabling Time	t_{PZH}	4.5	-	24	-	29	ns
Output Disabling Time	t_{PLZ}	4.5	-	25	-	29	ns
Output Disabling Time	t_{PHZ}	4.5	-	21	-	25	ns



Input Level	V_{CC}
Switching Voltage, V_S	$V_{CC}/2$

Figure 2 - Transition times and propagation delay times, combination logic.

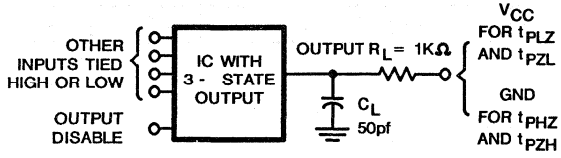


Figure 3 - Three state propagation delay test circuit.

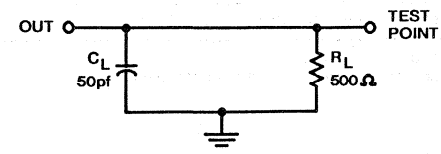


Figure 4 - Load circuit for t_{PHL}, t_{PLH}.

INHERENT RADIATION PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20ns pulse

POST-RADIATION PERFORMANCE at $T_A = +25^oC$

STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5V ±10%

CHARACTERISTICS		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0V or V_{CC}	-	0.75	-	2.0	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4V	6.0	-	5.0	-	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC} -0.4V	-6.0	-	-5.0	-	mA
Output Voltage, Low Level	V_{OL}	I_{OL} = 50µA	-	0.1	-	0.1	V
Output Voltage, High Level	V_{OH}	I_{OH} = -50 µA	V_{CC} -0.1	-	V_{CC} -0.1	-	V
Input Low Voltage	V_{IL}	-	-	0.3 V_{CC}	-	0.12 V_{CC}	V
Input High Voltage	V_{IH}	-	0.7 V_{CC}	-	0.7 V_{CC}	-	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}	-	±0.5	-	±5	µA

SWITCHING CHARACTERISTICS, t_r, t_f = 3ns, C_L = 50pF, R_L = 500Ω

CHARACTERISTICS		V_{CC} (V)	LIMITS				UNITS
			200k Rads (Si)		1M Rads (Si)		
			MIN.	MAX.	MIN.	MAX.	
Data to Qn Outputs	t_{PLH}	4.5	-	29	-	37	ns
Data to Qn Outputs	t_{PHL}	4.5	-	29	-	37	ns
LE to Qn Outputs	t_{PLH}	4.5	-	35	-	44	ns
LE to Qn Outputs	t_{PHL}	4.5	-	40	-	50	ns
Output Enabling Time	t_{PZL}	4.5	-	33	-	42	ns
Output Enabling Time	t_{PZH}	4.5	-	29	-	37	ns
Output Disabling Time	t_{PLZ}	4.5	-	29	-	37	ns
Output Disabling Time	t_{PHZ}	4.5	-	29	-	32	ns

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-in Test-Circuit Connections						
	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
HCS573MS	12, 13, 14, 15, 16, 17, 18, 19	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	20	12, 13, 14, 15, 16, 17, 18, 19	10	1, 2, 3, 4, 5, 6, 7, 8, 9, 11, 20

Dynamic Burn-in Test-Circuit Connections						
					OSCILLATOR	
TYPE	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50kHz	25kHz
HCS573MS	-	1, 10	12, 13, 14, 15, 16, 17, 18, 19	20	11	2, 3, 4, 5, 6, 7, 8, 9

NOTE: Each pin except V_{CC} and Ground will have a resistor (10k ± 5% for static and 680Ω ± 5% for dynamic).

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40µA	+12µA
I_{OL} and I_{OH}	-	-15% of 0 hr. value
I_{OZL}	-	-0.2µA of 0 hr. value
I_{OZH}	-	+0.2µA of 0 hr. value

* All measurements will not exceed the absolute limit.

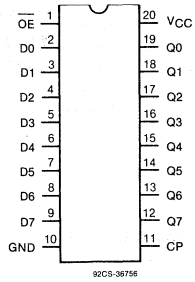
DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
ii	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5V
12, 13, 14, 15, 16, 17, 18, 19	10	1, 2, 3, 4, 5, 6, 7, 8, 9, 11, 20

NOTE: Each pin except V_{CC} and Ground will have a resistor of 47kΩ.

HCTS574MS



TERMINAL ASSIGNMENT

High-Reliability, Radiation-Hardened, High-Speed CMOS/SOS, Octal D-Type Flip-Flop, Positive Edge Trigger, 3-State

Aerospace Class S Screening

Radiation Features:
- *Radiation hardened to 200k or 1M rads (Si)*
- *Cosmic ray upset immunity typically 2 x 10^{-9} errors/bit-day*
- *Latch-up free under transient radiation*
- *Transient upset > 10^{10} rads/sec., 20ns pulse*

Type Features:
- *Typical propagation delay = 18ns @ V_{CC} = 4.5V, C_L = 50pF, T_A = 25°C*
- *3-State outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The HCTS574MS is a radiation-hardened non-inverting octal D-type flip-flop with 3-state outputs. The eight edge triggered flip-flops enter data on the LOW-to-HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When Output Enable is HIGH the outputs will be in the high-impedance state.

The HCTS574MS utilizes advanced CMOS/SOS technology to achieve high-speed operation and is a member of a family of radiation-hardened, high-speed, CMOS/SOS logic devices with TTL input compatibility.

The HCTS574MS is supplied in a 20-lead weld-seal ceramic flatpack package (K suffix) or a 20-lead dual-in-line ceramic package (D suffix).

Family Features:
- *Fanout (over temperature range):*
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range: -55 to +125°C*
- *Significant power reduction compared to LSTTL logic ICs*
- *HCTS types:*
  4.5 to 5.5V operation
  LSTTL Input Logic Compatibilty
  V_{IL} = 0.8V max., V_{IH} = V_{CC}/2 min.

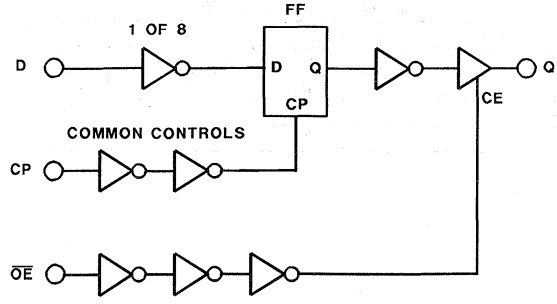


Figure 1 - Logic diagram.

TRUTH TABLE

$\overline{OE}$	CP	Dn	Qn
L	↑	H	H
L	↑	L	L
L	L	X	Q0
L	H	X	Q0
H	X	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH CLOCK (CP) Transition

NOTE: Q0 = the level of Q prior to indicated steady-state condition.

12 LOGIC CIRCUITS

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
DC DRAIN CURRENT, ANY ONE OUTPUT ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100° C ..... 500 mW
For T_A = +100 to +125° C ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR PACKAGE:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

OPERATING CONDITIONS at T_A = -55° C to +125° C. For maximum reliability, device should always be operated within the following range:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	4.5	5.5	V

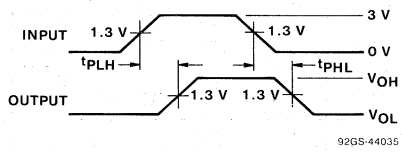
STATIC ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			+25° C		-55° C/+125° C		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	40	—	750	μA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	7.2	—	6	—	mA
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-7.2	—	-6	—	
Low-Level Output Voltage	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Low-Level Input Voltage	V_{IL}	—	—	0.8	—	0.8	
High-Level Input Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±0.5	—	±5	μA
3-State Output Leakage Current	I_{OZ}	Applied V = 0 V or V_{CC}	—	±1	—	±50	
Input Capacitance	C_{IN}*	—	—	10	—	10	pF
Output Capaciitance	C_{OUT}*	—	—	5	—	5	
Power Dissipation Capacitance	C_{PD}**	—	—	35	—	35	

* Guaranteed but not tested.
** Typical values. Characterized but not tested.

SWITCHING CHARACTERISTICS, V_{CC} = 4.5 V, t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		LIMITS				UNITS
		+25° C		-55° C/+125° C		
		MIN.	MAX.	MIN.	MAX.	
Propagation Delay: Clock to Q	t_{PLH}	—	29	—	36	ns
	t_{PHL}					
Enable to Output	t_{PZL}	—	32	—	39	
	t_{PZH}	—	27	—	32	
Disable to Output	t_{PLZ}	—	23	—	28	
	t_{PHZ}					



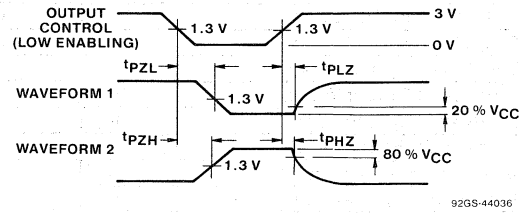


Fig. 2 - Timing waveforms.

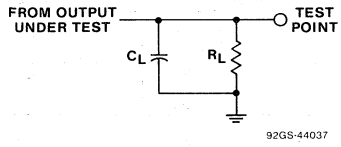


Fig. 3 - Load circuit for t_{PHL}, t_{PLH}, t_{PZH}, t_{PHZ}.

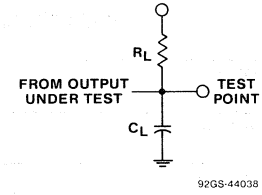


Fig. 4 - Load circuit for t_{PZL}, t_{PLZ}.

INHERENT PROPERTIES OF SOS

Latch-Up ..... Not Possible
Transient Survival ..... $\geq 10^{12}$ rads (Si)/s
Transient Upset ..... $\geq 10^{10}$ rads (Si)/s, 20-ns pulse

POST-RADIATION PERFORMANCE at T_A = +25°C

Radiation measurements are made on 4 samples per wafer. The limits shown are for within 1 hour of irradiation.

STATIC POST-RADIATION ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V ± 10%

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			200k Rads (Si)		1M Rad (Si)		
			MIN.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{CC}	V_{IN} = 0 V or V_{CC}	—	0.75	—	3.75	mA
Output (Sink) Current	I_{OL}	V_{OUT} = 0.4 V	6	—	5	—	
Output (Source) Current	I_{OH}	V_{OUT} = V_{CC}-0.4 V	-6	—	-5	—	
Low-Level Output Voltage	V_{OL}	I_{OL} = 50 μA	—	0.1	—	0.1	V
High-Level Output Voltage	V_{OH}	I_{OH} = -50 μA	V_{CC}-0.1V	—	V_{CC}-0.1V	—	
Low-Level Input Voltage	V_{IL}	—	—	0.8	—	0.3	
High-Level Input Voltage	V_{IH}	—	V_{CC}/2	—	V_{CC}/2	—	
Input Leakage Current	I_{IN}	V_{IN} = 0 V or V_{CC}	—	±5	—	±5	μA
Output Leakage Current	I_{OZ}	V_O = 0 V or V_{CC}	—	±50	—	±100	

POST-RADIATION SWITCHING CHARACTERISTICS, V_{CC} 4.5 V, t_r,t_f = 3 ns, C_L = 50 pF, R_L = 500 Ω

CHARACTERISTIC		LIMITS				UNITS
		200k Rads (Si)		1M Rad (Si)		
		MIN.	MAX.	MIN.	MAX.	
Propagation Delay: Clock to Q	t_{PLH}	—	36	—	45	ns
	t_{PHL}					
Enable to Output	t_{PZL}	—	39	—	49	
	t_{PZH}	—	32	—	40	
Disable to Output	t_{PLZ}	—	28	—	35	
	t_{PHZ}					

TABLE I - BURN-IN AND LIFE-TEST CIRCUITS

Static Burn-In Test-Circuit Connections						
TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6 V)	OPEN	GROUND	V_{CC} (6 V)
HCTS574MS	12-19	1-11	20	12-19	10	1-9, 11, 20
Dynamic Burn-In Test-Circuit Connections						
TYPE	OPEN	GROUND	½ V_{CC} (3 V)	V_{CC} (6 V)	OSCILLATOR	
					50 kHz	25 kHz
HCTS574MS	—	1, 10	12-19	20	11	2-9

NOTE: Each pin except 10 and 20 shall have a resistor of 10kΩ for static and 680Ω ±5% for dynamic burn-in.

TABLE II - DELTA LIMITS AND CALCULATIONS

PARAMETER	ABSOLUTE LIMIT*	DELTA LIMIT
I_{CC}	40 μA	+12 μA
I_{OL} and I_{OH}	—	-15% of 0 hr value
I_{OZL}	-1 μA	-200 nA
I_{OZH}	+1 μA	+200 nA

*All measurements will not exceed the absolute limit.

DELTA CALCULATION	INITIAL READING	FINAL READING
I	Initial Electrical Tests	Interim Electrical Tests I
II	Initial Electrical Tests	Interim Electrical Tests II
III	Initial Electrical Tests	Interim Electrical Tests III

TABLE III - RADIATION TEST CIRCUIT

OPEN	GROUND	V_{CC} = 5 V
12-19	10	1-9, 11, 20

NOTE:
Each pin except 10 and 20 shall have a resistor of 680 Ω - 47 kΩ.

Product Number Selection Guide

HARRIS TYPE NUMBER	CIRCUIT FUNCTION	STANDARD SCREENING	NUMBER OF PINS
CD4000B	Dual 3-Input NOR Gate Plus Inverter	/MSH, /MSR	14
CD4001B	Quad 2-Input NOR Gate	/SH, /BH, /SR, /BR	14
		/MSH, /MSR	14
CD4002B	Dual 4-Input NOR Gate	/SR, /BR	14
		/MSH, /MSR	14
CD4006B	18-Stage Static Shift Register	/MSH, /MSR	14
CD4007UB	Dual Complementary Pair Plus Inverter	/SH, /BH	14
		/MSH, /MSR	14
CD4008B	4-Bit Full Adder with Parallel Carry-Out	/SR, /BR	16
		/MSH, /MSR	16
CD4009UB	Hex Buffer/Converter (Inverting)	/MSH, /MSR	16
CD4010B	Hex Buffer/Converter (Non-Inverting)	/MSH, MSR	16
CD4011B	Quad 2-Input NAND Gate	/SH, /BH	14
		/MSH, /MSR	14
CD4012B	Dual 4-Input NAND Gate	/SH, /BH	14
		/MSH, /MSR	14
CD4013B	Dual "D" Flip-Flop with Set/Reset Capability	/SH, /BH	14
		/MSH, /MSR	14
CD4014B	8-Stage Static Shift Register	/SH, /BH	16
		/MSH, /MSR	16
CD4015B	Dual 4-Stage Static Shift Register	/SH, /SR	16
		/MSH, /MSR	16
CD4016B	Quad Bilateral Switch	/MSH, /MSR	14
CD4017B	Decade Counter/Divider	/BH, /SH	16
		/MSH, /MSR	16
CD4018B	Presettable Divide-by "N" Counter	/SH, /BH	16
		/MSH, /MSR	16
CD4019B	Quad AND/OR Select Gate	/SH, BH	16
		/MSH, /MSR	16
CD4020B	14-Stage Binary Ripple Counter	/SH, /BH	16
		/MSH, /MSR	16
CD4021B	8-Stage Static Shift Register	/SH, /BH	16
		/MSH, /MSR	16
CD4022B	Divide-by-8 Counter/Divider	/SH, /BH	16
		/MSH, /MSR	16
CD4023B	Triple 3-Input NAND Gate	/SH, /HB	14
		/MSH, /MSR	14
CD4024B	7-Stage Binary Ripple Counter	/SH, /BH	14
		/MSH, /MSR	14
CD4025B	Triple 3-Input NOR Gate	/SH, /BH	14
		/MSH, /MSR	14
CD4026B	Decade Counter/Divider	/MSH, /MSR	16
CD4027B	Dual "J-K" Flip-Flop with Set/Reset Capability	/SH, /BH	16
		/MSH, /MSR	16
CD4028B	BCD-to-Decimal Decoder	/SR, /BR	16
		/MSH, /MSR	16
CD4029B	Presettable Up/Down Counter	/MSH, /MSR	16
CD4030B	Quad Exclusive-OR Gate	/SH, /BH	14
		/MSH, /MSR	14

Product Number Selection Guide

HARRIS TYPE NUMBER	CIRCUIT FUNCTION	STANDARD SCREENING	NUMBER OF PINS
CD4031B	64-Stage Static Shift Register	/MSH, /MSR	16
CD4033B	Decade Counter/Divider	/MSH, /MSR	16
CD4034B	8-Stage Static Shift Register	/MSH, MSR	24
CD4035B	4-Stage Parallel-In/Parallel-Out Shift Register	/MSH, /MSR	24
CD4040B	12-Stage Binary Ripple Counter	/MSH, /MSR	16
CD4041UB	Quad True/Complement Buffer	/SR, /BR /MSH, /MSR	14 14
CD4042B	Quad Clocked "D" Latch	/MSH, /MSR	16
CD4043B	Quad NOR R/S Latch (3-State Outputs)	/MSH, /MSR	16
CD4044B	Quad NAND R/S Latch (3-State Outputs)	/MSH, /MSR	16
CD4046B	Micropower Phase-Locked Loop	/MSH, /MSR	16
CD4047B	Monostable/Astable Multivibrator	/MSH, /MSR	14
CD4048B	Multifunctional Expandable 8-Input Gate (3-State Output)	/MSH, /MSR	16
CD4049UB	Hex Buffer/Converter (Inverting)	/SH, /BH /MSH, /MSR	16 16
CD4050B	Hex Buffer/Converter (Non-Inverting)	/SH, /BH /MSR, /MSH	16 16
CD4051B	8-Channel Analog Multiplexer/ Demultiplexer	/MSH, /MSR	16
CD4052B	4-Channel Analog Multiplexer/ Demultiplexer	/MSR, /MSH	16
CD4053B	Analog Multiplexer/Demultiplexers - Triple 2-Channel	/MSH, /MSR	16
CD4060B	14-Stage Binary Ripple Counter/ Divider and Oscillator	/MSH, /MSR	16
CD4063B	4-Bit Magnitude Comparator	/MSR, /MSH	16
CD4066B	Quad Bilateral Switch	/SH, /BH /MSH, /MSR	14 14
CD4067B	16-Channel Analog Multiplexers/ Demultiplexers	/MSH, /MSR	24
CD4068B	8-Input NAND/AND Gate	/MSH, /MSR	
CD4069UB	Hex Inverter	/SH, /BH /MSH, /MSR	14 14
CD4070B	Quad Exclusive-OR Gate	/SH, /BH /MSH, /MSR	14 14
CD4071B	Quad 2-Input OR Gate	/SH, /BH /MSH, /MSR	14 14
CD4072B	Dual 4-Input OR Gate	/BR /MSH, /MSR	14 14
CD4073B	Triple 3-Input AND Gate	/BR /MSH, /MSR	14 14
CD4075B	Triple 3-Input OR Gate	/BH, /SH /MSH, /MSR	14 14
CD4076B	4-Bit "D" Flip-Flop (3-State Outputs)	/MSH, /MSR	16
CD4077B	Quad Exclusive-NOR Gate	/BR /MSH, /MSR	14 14
CD4078B	8-Bit NOR/OR Gate	/MSH, /MSR	14

Product Number Selection Guide

HARRIS TYPE NUMBER	CIRCUIT FUNCTION	STANDARD SCREENING	NUMBER OF PINS
CD4081B	Quad 2-Input AND Gate	/SH, /BH /MSH, /MSR	14 14
CD4082B	Dual 4-Input AND Gate	/BR /MSH, /MSR	14 14
CD4085B	Dual 2-Wide, 2-Input AND/OR/Invert (AOI) Gate	/SH, /BH /MSH, /MSR	14 14
CD4086B	Expandable 4-Wide, 2-Input AND/OR/ Invert (AOI) Gate	/SH, /BH	14
CD4089B	Binary Rate Multiplier	/MSH, /MSR	16
CD4093B	Quad 2-Input NAND Schmitt Trigger	/MSH, /MSR	14
CD4094B	8-Stage Shift-and-Store Bus Register	/MSH, /MSR	16
CD4095B	Gated "J-K" Flip-Flop (Non-Inverting)	/MSH, /MSR	14
CD4096B	Gated "J-K" Flip-Flop (Inverting) and (Non-Inverting)	/MSH, /MSR	14
CD4097B	8-Channel Analog Multiplexer/ Demultiplexer	/MSH, /MSR	24
CD4098B	Dual Monostable Multivibrator	/MSH, /MSR	16
CD4099B	8-Bit Addressable Latch	/BR /MSH, /MSR	16 16
CD4502B	Strobed Hex Inverter/Buffer	/SR, /BR /MSH, /MSR	16 16
CD4503B	Hex Buffer (Non-Inverting)	/MSH, /MSR	16
CD4504B	Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation	/MSH, /MSR	16
CD4508B	Dual 4-Bit Latch	/MSH, /MSR	24
CD4510B	Presettable 4-Bit BCD Up/Down Counter	/MSH, /MSR	16
CD4511B	BCD-to-7-Segment Latch Decoder/Driver	/MSH, /MSR	16
CD4512B	8-Channel Data Selector (3-State Output)	/MSH, /MSR	16
CD4514B	4-Bit Latch/4-to-16-Line Decoder (Outputs Low)	/MSH, /MSR	24
CD4515B	4-Bit Latch/4-to-16-Line Decoder (Outputs Low)	/MSH, /MSR	24
CD4516B	Presettable 4-Bit Binary Up/Down Counter	/MSH, /MSR	16
CD4517B	Dual 64-Bit Shift Register	/MSH, /MSR	16
CD4518B	Dual BCD Up Counter	/MSH, /MSR	16
CD4520B	Dual Binary Up Counter	/MSH, /MSR	16
CD4527B	BCD Rate Multiplier	/MSH, /MSR	16
CD4532B	8-Input Priority Encoder	/MSH, /MSR	16
CD4536B	Programmable Timer	/MSH, /MSR	16
CD4555B	Dual 1-of-4 Decoder/Demultiplexer (Outputs High)	/MSH, /MSR	16
CD4556B	Dual Binary to 1 of 4 Decoder/ Demultiplexers (Outputs Low)	/MSH, /MSR	16
CD4585B	4-Bit Magnitude Comparator	/MSH, /MSR	16
CD4724B	8-Bit Addressable Latch	/MSH, /MSR	16
CD14538B	Dual Precision Monostable Multivibrator	/MSH, /MSR	16
CD40100B	9-Bit Parity Generator/Checker	/MSH, /MSR	16
CD40101B	9-Bit Parity Generator/Checker	/MSH, /MSR	14
CD40102B	Presettable 2-Decade BCD Down Counter	/MSH, /MSR	16

Product Number Selection Guide

HARRIS TYPE NUMBER	CIRCUIT FUNCTION	STANDARD SCREENING	NUMBER OF PINS
CD40103B	Presettable 8-Bit Binary Down Counter	/MSH, /MSR	16
CD40104B	4-Bit Bidirectional Universal Shift Register	/MSH, /MSR	16
CD40105B	4-Bit x 16 Word FIFO Buffer Register	/MSH, /MSR	16
CD40106B	Hex Schmitt Trigger	/MSH, /MSR	14
CD40107B	Dual 2-Input NAND Buffer/Driver	/MSH, /MSR	14
CD40108B	4 x 4 Multiport Register	/MSH, /MSR	24
CD40109B	Quad Low-to-High Voltage Interface	/MSH, /MSR	16
CD40110B	Decade Up-Down Counter/Decoder/Latch Display Driver	/MSH, /MSR	16
CD40147B	10-Line to 4-Line BCD Priority Encoder	/MSH, /MSR	16
CD40160B	Synchronous Programmable 4-Bit Counters Decade with Asynchronous Clear	/MSH, /MSR	16
CD40162B	Synchronous Programmable 4-Bit Counters Decade with Synchronous Clear	/MSH, /MSR	16
CD40163B	Synchronous Programmable 4-Bit Counters Binary with Synchronous Clear	/MSH, /MSR	16
CD40174B	Synchronous Programmable 4-Bit Counters Binary with Synchronous Clear	/MSH, /MSR	16
CD40175B	Quad 'D'-Type Flip-Flop	/MSH, /MSR	16
CD40181B	CMOS 4-Bit Arithmetic Logic Unit	/MSH, /MSR	24
CD40182B	CMOS Look-Ahead Carry Generator	/MSH, /MSR	16
CD40192B	CMOS Look-Ahead Carry Generator	/MSH, /MSR	16
CD40193B	CMOS Presettable Up/Down Counters (Dual Clock with Reset)	/MSH, /MSR	16
CD40194B	4-Bit Bidirectional Universal Shift Register	/MSH, /MSR	16
CD40208B	4 x 4 Multiport Register	/MSH, /MSR	24
CD40257B	Quad 2-Line-to-1-Line Data Selector/ Multiplexer	/MSH, /MSR	16

CD4000B-Series Family Description and Features

The Harris high reliability CD4000B series of high voltage CMOS integrated circuits consists of a broad range of SSI, MSI-1 and MSI-2 (LSI) functions from simple gates to complex counters, registers and arithmetic circuits. Specific design features for CMOS devices and the performance advantages of CMOS technology — low power consumption, high noise immunity, high speed, high fanout, TTL and DTL logic compatibility, excellent temperature stability, and fully protected inputs and outputs — provide the logic system designer with a capability to achieve outstanding performance, high reliability, and simplified circuitry in a wide variety of equipment designs.

Features

- 100% Tested for Quiescent Current at 20V
- Maximum Input Current (Leakage) of 1μA at 18V Over Full Package Temperature Range: 100nA at 18V at +25°C
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Noise Margin (Over Full Package Temperature Range): 1V at V_{DD} = 5V; 2V at V_{DD} = 10V; 2.5V at V_{DD} = 15V
- Meets All Requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Buffered vs. Unbuffered Gates

The new industry standard established a suffix "UB" for CMOS products that meet all B-series specifications except that the logical outputs of the devices are not buffered and the V_{IL} and V_{IH} specifications are 20% and 80% of V_{DD}, respectively. The suffix "B" defines high voltage buffered output devices in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

Both buffered ("B") and unbuffered ("UB") versions of the popular Harris NOR and NAND gates are supplied to make available to designers the advantages of both. The following table briefly compares the features of the two versions.

CHARACTERISTIC	BUFFERED VERSION ("B")	UNBUFFERED VERSION ("UB")
Propagation Delay (Speed)	Moderate	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Low
Output Oscillation for Slow Inputs	Yes	No
Input Capacitance	Low	High

Harris Compliance to Mil-Std-883, Rev. C

Harris CD4000-series parts are in full compliance with Mil-Std-883C, Paragraph 1.2.1. Two different types of product are provided to meet the requirements of this paragraph, Class S and Class B.

Slash MS (__/MS) meets Class S requirements when the optional Group B conformance test is performed. Electrical tests are performed to black-dot parameters described in the Electrical Characteristics.

Slash 3A (__/3A) meets Class B requirements. Electrical tests are performed to black-dot parameters described in the Electrical Characteristics.

Harris also provides CD4000-series parts that meet the requirements of Mil-Std-883C, Paragraph 1.2.2. This family of parts has the following designation.

Slash 3 (__/3) meets most of the requirements of a Class B part as described in details presented in the table "Harris Compliance to Mil-Std-883", located in the Guide to Products and Packages section of this databook.

Harris JAN M38510 CMOS ICs

The Harris high reliability product line also provides devices that are manufactured and tested in accordance with the Mil-M-38510 (detailed and general) specification, which includes methods and procedures of the Military Standard Mil-Std-883.

SCREENING LEVELS FOR HARRIS HIGH RELIABILITY CD4000B-SERIES INTEGRATED CIRCUITS

SCREENING LEVELS†		APPLICATION	DESCRIPTION
PACKAGED DEVICES (D, F or K Suffix)			
/MS	Class S with SEM Inspection and Condition A Precap Visual Inspection	Aerospace and Missles	For devices intended for use where maintenance and replacement are difficult and reliability is imperative
/MSR	Same as /MS + Radiation Hardened to 10^5 Rads(Si)		
/MSH	Same as /MS + Radiation Hardened to 10^6 Rads(Si)		
/3A /3	Class B (Full Compliance) Class B, modified	Military and Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement can be performed but are difficult and expensive
CHIPS (H Suffix)			
/S	SEM inspection and condition A visual inspection	Aerospace and Missiles	For hybrid applications where maintenance and replacement are extremely difficult and reliability s imperative
/SR	Same as /S + radiation hardened to 10^6 Rads(Si)		
/SH	Same as /S + radiation hardened to 10^6 Rads(Si)		
/M	Condition B precap visual inspection	Military and Industrial	For general applications

† For screening details refer to Lot Screening charts.

The table below indicates the Harris screening performed on JAN S, /MS, JAN B, /3 and /3A devices. The /MS is equivalent to Mil-Std-883 Class S and the /3 and /3A are equivalent to Mil-Std-883 Class B screens to Method 5004. As shown in the Manufacturing and Conformance Testing Table the differences between a /3 and a /3A is the lead finish and pellet mounting technique. It should be noted that all CD4XXXB-Series wafers are manufactured at the JAN certified plant and any type manufactured in the U.S. is completely assembled and tested on our JAN certified line.

Total Lot Screening for Harris High Reliability CD4000B-Series ICs

Screening Test	Conditions	Method	RCA/Level		Notes
			JAN S, MS	JAN B, 3, 3A	
Wafer Acceptance Test (WAT)	—	5007	X	—	
Rad Vertification If Required	4 Chips Per Wafer	1019	X	—	
Assembly 100% Non-Dest Bond Pull	—	2023	X	—	
Pre-Cap Visual	Condition A	2010	X	—	
	Condition B	2010	—	X	
Preconditioning Stabilization Bake	Cond C	1008	X	X	
Temperature Cycle	Cond C	1010	X	X	
Centrifuge	Cond E, Y1 Only	2001	X	X	
Fine Leak	Cond B	1014	—	X	
Gross Leak	Cond C	1014	—	X	
Particle Noise Test	Cond A	2020	X	—	
Test and Burn-In Serialize	—	—	X	—	
Initial Test	—	—	X	X	1
Static Burn-In 1 24 Hrs w/Deltas	135°C Inputs at V_{SS}, Outputs Open	1015	X	—	1, 3
Static Burn-In 2 24 Hrs w/Deltas	135°C Inputs at V_{DD}, Outputs Open	1015	X	—	1, 3, 5
Dynamic Burn-In 180 Hrs w/Deltas	135°C	1015 Condition D	X	—	1, 2, 3, 5
Static Burn-in 2 120 Hrs	135°C Inputs at V_{DD}, Outputs Open	1015	—	X	1, 2, 4, 5
Final Elec DC + 25°C	—	—	X	X	
Final Elec DC + 125°C	—	—	X	X	
Final Elec DC -55°C	—	—	X	X	
Final Elec AC + 25°C	—	—	X	X	
Fine Leak	Cond B	1014	X	—	
Gross Leak	Cond C	1014	X	—	
Final Inspection X-Ray Inspection	2 Views	2012	X	—	
Group A	—	—	X	X	
100% Visual Inspect	—	2009	X	X	

Notes:

1. See individual data bulletins for electrical testing of specific types or JAN Slash Sheets as applicable.
2. Alt. time/temp regression used per method 1015.
3. PDA's for /MS is 5% cumulative for Static 1 and Static 2 and 5% for Dynamic. PDA for functional is 3%.
4. PDA for /3 and /3A is 5%, one reburn allowed at 3%.
5. PDA's are based on Group A subgroup 1.

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}) ..... -0.5V to +20V
(Voltage Referenced to V_{SS} Terminals)

Input Voltage Range, All Inputs ..... -0.5V to V_{DD} +0.5V

DC Input Current, Any One Input ..... ±10mA

Operating Temperature Range (T_A) ..... -55°C to +125°C
Package Types D, F, K, H

Storage Temperature Range (T_{STG}) ..... -65°C to +150°C

Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	28°C/W	TBD°C/W
Flatpack Package	22°C/W	TBD°C/W

Maximum Package Power Dissipation (P_D) at +125°C
For T_A = -55°C to +100°C (Package Types D, F, K) 500W
For T_A = +100°C to +125°C (Package Types D, F, K)....Derate Linearity at 12mW/°C to 200mW

Device Dissipation Per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)

Junction Temperature ..... +175°C

Recommended Operating Conditions

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

Supply Voltage Range..... 3V Min, 18V Max
(For T_A = Full Package Temperature Range)

Device Classification for Leakage Current

The table below classifies the levels of device leakage as SSI, MSI-1 and MSI-2. In order to determine the limits which apply to a specific device type, consult the standard DC electrical characteristics chart.

CLASSIFICATION ACCORDING TO CIRCUIT COMPLEXITY

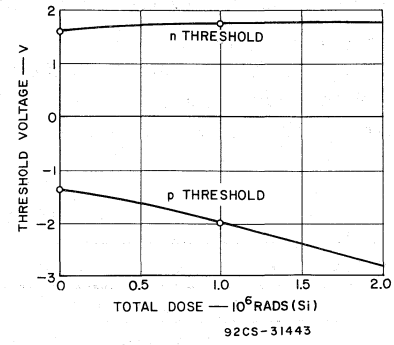
GATES/ INVERTERS (SSI)	BUFFERS/FLIP-FLOPS/ LATCHES/MULTILEVEL GATES (MSI-1)		COMPLEX LOGIC (MSI-2)		
CD4000B	CD4009UB*	CD4085B	CD4006B	CD4060B	CD4556B
CD4001B	CD4010B	CD4086B	CD4008B	CD4063B	CD4585B
CD4002B	CD4013B	CD4093B*	CD4014B	CD4067B*	CD4724B
CD4007UB	CD4019B	CD4095B	CD4015B	CD4076B	CD14538B
CD4011B	CD4027B	CD4096B	CD4017B	CD4089B	CD40100B
CD4012B	CD4030B	CD4098B	CD4018B	CD4094B	CD40101B
CD4016B*	CD4041UB*	CD4502B*	CD4020B	CD4097B*	CD40102B
CD4023B	CD4042B	CD4503B*	CD4021B	CD4099B	CD40103B
CD4025B	CD4043B	CD40106B*	CD4022B	CD4508B	CD40104B
CD4048B	CD4044B	CD40107B*	CD4024B	CD4510B	CD40105B
CD4066B*	CD4047B	CD40109B*	CD4026B	CD4511B*	CD40108B
CD4068B	CD4049UB*	CD40147B	CD4028B	CD4512B	CD40110B*
CD4069UB	CD4050B	CD40174B	CD4029B	CD4514B	CD40160B
CD4071B	CD4070B	CD40175B	CD4031B*	CD4515B	CD40161B
CD4072B	CD4077B	CD40257B	CD4033B	CD4516B	CD40162B
CD4073B			CD4034B	CD4517B	CD40163B
CD4075B			CD4035B	CD4518B	CD40181B
CD4078B			CD4040B	CD4520B	CD40182B
CD4081B			CD4046B*	CD4527B	CD40192B
CD4082B			CD4051B*	CD4532B	CD40193B
			CD4052B*	CD4536B	CD40194B
			CD4053B*	CD4555B	CD40208B

* Indicates type for which, because of design requirements, one or more static characteristics differ from the standardized data. These differences are defined in separate DC Electrical Characteristics charts.

Radiation Resistant CD4000-Series

Harris radiation hardened CD4000-series CMOS integrated circuits tested to withstand total ionizing radiation dosages of 1 x 10^5 rads (Si) — R-suffix types, and 1 x 10^6 rads (Si) — H-suffix types. These radiation tolerances are achieved by special process controls imposed during wafer fabrication.

Harris radiation hardened types may be screened to Mil-M-38510 Class S and to level /MS. The specified levels of radiation resistance are verified per Table V group E subgroup 2 of Method 5005 and tested according to Method 1019 of Mil-Std-883. Four electrically good packaged samples from each wafer, one from each quadrant, are exposed in a Cobalt 60 source for a time period corresponding to the specified total dose. The samples are then electrically tested within one hour after exposure for threshold voltage, threshold voltage delta, I_{DD} leakage current, and functionality. Propagation delay is also measured for 38510 tested product.



TYPICAL THRESHOLD VOLTAGE VARIATIONS OF HARRIS MEGARAD CD4000-SERIES CMOS INTEGRATED CIRCUITS AS A FUNCTION OF TOTAL DOSE GAMMA RADIATION

RADIATION RESISTANT CD4000-SERIES CMOS ICs

Post Radiation Test Criteria — Maximum Limits for I_{DD}, (V_{DD} = 18V for B-Series Types or 15V for A-Series Types)

TYPE	I_{DD} (MAX) µA	TYPE	I_{DD} (MAX) µA	TYPE	I_{DD} (MAX) µA	TYPE	I_{DD} (MAX) µA
CD4000	2.5	CD4040	25	CD4078	2.5	CD4555	25
CD4001	2.5	CD4041	7.5	CD4081	2.5	CD4556	25
CD4002	2.5	CD4042	7.5	CD4082	2.5	CD4585	25
CD4006	25	CD4043	7.5	CD4085	2.5	CD4724	25
CD4007	2.5	CD4044	7.5	CD4086	2.5	CD40100	25
CD4008	25	CD4046	25	CD4089	25	CD40101	25
CD4009	7.5	CD4047	25	CD4093	7.5	CD40102	25
CD4010	7.5	CD4048	7.5	CD4094	25	CD40103	25
CD4011	2.5	CD4049	7.5	CD4095	7.5	CD40104	25
CD4012	2.5	CD4050	7.5	CD4096	7.5	CD40105	25
CD4013	7.5	CD4051	25	CD4097	25	CD40106	7.5
CD4014	25	CD4052	25	CD4098	7.5	CD40107	7.5
CD4015	25	CD4053	25	CD4099	25	CD40108	25
CD4016	2.5	CD4060	25	CD4502	7.5	CD40109*	7.5
CD4017	25	CD4063	25	CD4503	7.5	CD40147	25
CD4018	25	CD4066	2.5	CD4504	7.5	CD40160	25
CD4019	7.5	CD4067	25	CD4508	25	CD40161	25
CD4020	25	CD4068	7.5	CD4510	25	CD40162	25
CD4021	25	CD4069	2.5	CD4511	25	CD40163	25
CD4022	25	CD4070	2.5	CD4512	25	CD40174	7.5
CD4023	2.5	CD4071	2.5	CD4514	25	CD40175	7.5
CD4024	25	CD4072	2.5	CD4515	25	CD40181	25
CD4025	2.5	CD4073	2.5	CD4516	25	CD40182	25
CD4026	25	CD4075	2.5	CD4517	25	CD40192	25
CD4027	7.5	CD4076	25	CD4518	25	CD40193	25
CD4028	25	CD4077	2.5	CD4520	25	CD40194	25
CD4029	25			CD4527	25	CD40208	25
CD4030	7.5			CD4532	25	CD40257	7.5
CD4031	25			CD4536	25		
CD4033	25						
CD4034	25						
CD4035	25						

Post Radiation Threshold Voltage Test Criteria (V_{DD} = 10V; I = Constant 10µA)

N Threshold = 0.2V min

*P Threshold = 3.5V max CD40109 and 40106
P Threshold = 2.8V max

ΔP Threshold = 1.0V max
ΔN Threshold = 1.0V max

Radiation Hardness Assurance Testing

CD4000-Series Total Dose Testing Procedures

- **Class S Wafer Sampling**
  - ▸ Test Four Samples (High-Rel Visual Rejects)
  - ▸ One From Each Quadrant of Wafer
  - ▸ Reject If Any One Sample Fails
- **Class B Inspection Lot Sampling**
  - ▸ LT PD = 20, 11/0
    18/1

CD4000-SERIES POST RADIATION TESTS

SYMBOL	CHARACTERISTIC	JAN LIMIT	NONJAN LIMIT	VOLTAGE
V_{TN}	N Threshold Voltage	0.3V Min	0.2V Min	10V
V_{TP}	P Threshold Voltage	2.8V Max	2.8V Max	10V
ΔV_T	Delta Threshold Voltage	1.4V Max	1.0V Max	10V
I_{SS}	Quiescent Current	100 x Max	100 x Max	18V
	CD4000B-Series	Pre-Rad Value	Pre-Rad Value	
T_{PLH}, T_{PHL}	Propagation Delay	1.35 x Max Pre-Rad Value		5V*

* Worst case test condition

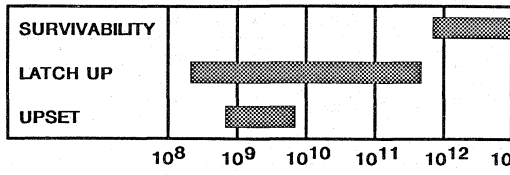
Radiation Resistant CD4000 Series

SCREENING LEVELS FOR HARRIS HIGH RELIABILITY RADIATION RESISTANT CD4000-SERIES CMOS ICs

SCREENING LEVELS		APPLICATION	DESCRIPTION
PACKAGED DEVICES (D, F, K OR J SUFFIX)			
/MSR /MSH	Class S with SEM Inspection and Condition A Precap Visual Inspection + Radiation Hardened to 10^5 Rads (Si) +Radiation Hardened to 10^6 Rads (Si)	Aerospace and Missiles	For devices intended for use where maintenance and replacement are difficult and reliability is imperative
CHIPS (H SUFFIX)			
/SR /SH	SEM Inspection and Condition A Visual Inspection + Radiation Hardened to to 10^5 Rads (Si) + Radiation Hardened to to 10^6 Rads (Si)	Aerospace and Missiles	For hybrid applications where maintenance and replacement are extremely difficult and reliability is imperative

CD4000-Series CMOS ICs
Transient Radiation Resistance

Samples of CD4000-series devices representing all levels of circuit complexity have been characterized for transient radiation effects. The data indicate the ranges of occurence of upset, latchup and survivability as a function of radiation dose rate.



EFFECTS OF TRANSIENT RADIATION (10^6 RADS (Si) ON CD4000-SERIES INTEGRATED CIRCUITS (ALUMINUM GATE CMOS ON BULK SILICON)

Latchup

Latchup occurs because of the presence of inherent bipolar SCR structures in bulk CMOS devices. In normal operation, the parasitic bipolar SCR remains inactive. The device is said to be in the latchup state when the parasitic SCR structures become activated, thereby creating a low impedance path from V_{DD} to V_{SS}. In the "ON" condition, the SCR can conduct heavily at low voltages. Latchup may be induced by the resultant photocurrents of high intensity transient ionizing radiation or by applying excessive voltage. Once turned on, the SCR can be rendered dormant again only by removing the power supply. Burn-out of the device may result if the current is not limited in some way.

The region of occurance of the latch condition in CMOS ICs under high intensity transient radiation is quite wide. Only two known device types latch below the 1 x 10^9 RAD (Si)/s level. A significant number of device types do not latch above dose rates of 1 x 10^{11} RADs (Si)/s.

Latchup Protection

Latchup protection in bulk CMOS devices can be achieved by taking advantage of the effects of neutron irradiation. Neutron irradiation will reduce minority-carrier lifetime, which, in turn attenuates the current gains, or betas, of bipolar transistors. To turn on the SCR structure of CMOS devices, it is necessary for the beta product of its bipolar transistors are majority- carrier devices, normal CMOS performance is generally unaffected by neutron irradiation. Therefore, neutron irradiation is a suitable method for precluding latchup in CMOS devices. In addition, neutron-irradiated CMOS devices are less susceptible to logic upset due to transient radiation.

Neutron-Irradiated CMOS

Harris offers custom CD4000-series devices which are made from wafers that are exposed to a neutron fluence of approximately 1 x 10^{14}n/cm^2. After neutron irradiation, wafers can be assembled and screened to all requirements of the Harris level product.

Survivability

Survivability level is the maximum transient-radiation level at which damage does not occur. Above this level photocurrents are created to the extent that excessive dissipation is caused, resulting in permanent damage to the device.

Standard DC Electrical Characteristics

Standard "B" Series Devices

The following table contains electrical characteristics for all CD4000B-series standard output CMOS devices. These parameters are 100% tested except where indicated.

Static Electrical Parameters	Conditions			Limits at indicated Temperatures						Units	Notes
				-55°C		+25°C		+125°C			
	V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	Min.	Max.		
Functional Test•	—	—	—	—	—	—	—	—	—		4
Quiescent device current I_{DD}	—	0,5	5	—	0.25•	—	0.25•	—	7.5•		
	—	0,10	10	—	0.5•	—	0.5•	—	15•		
SSI Types	—	0,15	15	—	1•	—	1•	—	30•	μA	1
See Classification Chart	—	0,20	20	—	5	—	5	—	150		
MSI-1	—	0,5	5	—	1•	—	1•	—	30•		
See Classification	—	0,10	10	—	2•	—	2•	—	60•		
Chart	—	0,15	15	—	4•	—	4•	—	120•	μA	1, 2
	—	0,20	20	—	20	—	20	—	600		
MSI-2	—	0,5	5	—	5•	—	5•	—	150•		
See Classification	—	0,10	10	—	10•	—	10•	—	300•		
Chart	—	0,15	15	—	20•	—	20•	—	600•	μA	1
	—	0,20	20	—	100	—	100	—	3000		
Output low drive	0.4	0,5	5	0.64•	—	0.51	—	0.36•	—		
current	0.5	0,10	10	1.6•	—	1.3	—	0.9•	—	mA	
I_{OL} min.	1.5	0,15	15	4.2•	—	3.4	—	2.4•	—		
Output high drive	4.6	0,5	5	-0.64	—	-0.51	—	-0.36•	—		
current	2.5	0,5	5	-2.0	—	-1.6	—	-1.15•	—		
I_{OH} min.	9.5	0,10	10	-1.6	—	-1.3	—	-0.9•	—	mA	
	13.5	0,15	15	-4.2	—	-3.4	—	-2.4•	—		
Output voltage	—	0,5	5	—	0.05•	—	0.05•	—	0.05•		
low-level	—	0,10	10	—	0.05•	—	0.05•	—	0.05•	V	
V_{OL} max.		0,15	15	—	0.05	—	0.05	—	0.05		
Output voltage	—	0,5	5	4.95•	—	4.95•	—	4.95	—		
high-level	—	0,10	10	9.95•	—	9.95•	—	9.95	—	V	
V_{OH} min.		0,15	15	14.95	—	14.95	—	14.95	—		
Input low voltage	4.5	—	5	—	1.5	—	1.5	—	1.5		
V_{IL} max.	9	—	10	—	3•	—	3	—	3	V	
Buffered (B)	13.5	—	15	—	4	—	4	—	4		
	4.5	—	5	—	1•	—	1	—	1		
Unbuffered (UB)	9	—	10	—	2	—	2	—	2	V	
	13.5	—	15	—	2.5	—	2.5	—	2.5		
Input high voltage	0.5, 4.5	—	5	3.5	—	3.5	—	3.5	—		
V_{IH} min.	1, 9	—	10	7	—	7	—	7	—	V	
Buffered (B)	1.5, 13.5	—	15	11	—	11	—	11	—		
	0.5,4.5	—	5	4	—	4	—	4	—		
Unbuffered (UB)	1,9	—	10	8	—	8	—	8	—	V	
	1.5, 13.5	—	15	12.5	—	12.5	—	12.5	—		
Input current I_{IN}	—	0,20	20	—	±0.1	—	±0.1	—	±1	μA	1
3-state output leakage current I_{OUT}	0,20	0,20	20	—	±0.4	—	±0.4	—	±12	μA	1, 3

• These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

NOTES:

1. At -55°C test is performed with V_{DD} of 18V.
2. CD4047B - Maximum DC supply voltage V_{DD} is 13V for radiation hardened version of this type when operating with RC network.
3. For applicable devices only.
4. At 25°C V_{IN} = 0 - 20V, V_{DD} = 20V; 125°C V_{IN} = 0 - 18V, V_{DD} = 18V; and at -55°C V_{IN} = 0 - 3V, V_{DD} = 3V.

Non-Standard DC Electrical Characteristics

Non-Standard "B" Series Devices

The table below indicates all devices which are considered to be non-standard. Non-standard devices are types such as bilateral switches (CD4066B), multiplexers (CD4051B), special sink or source currents (CD4049UB, CD4050B), and open drain buffer/drivers (CD40107B) which exhibit non-standard outputs or special parameters. This table shows the 100% electrical tests that are performed on these specialized devices. These tests take the place of corresponding parameters in the Standard Electrical Characteristics table. For the types listed with R_{ON} tests, drive current and output voltage tests should be deleted from the Standard Electrical Characteristics table.

Static Electrical Parameters	Conditions			Limits at Indicated Temperatures				Units
				-55°C	+25°C		+125°C	
	V_O	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD4009UB, CD4010B								
Output low drive current I_{OL} min.	0.4	0,5	4.5	3.2•	2.6•	—	1.8•	mA
	0.4	0,5	5	3.75•	3	—	2.1•	
	0.5	0,10	10	10.0•	8	—	5.6•	
	1.5	0,15	15	30.0•	24	—	16.0•	
Output high drive current I_{OH} min.	4.6	0,5	5	-0.25•	-0.2	—	-0.15•	mA
	2.5	0,5	5	-1.0•	-0.8	—	-0.58•	
	9.5	0,10	10	-0.55•	-0.45	—	-0.33•	
	13.5	0,15	15	-1.65•	-1.5	—	-1.1•	
CD4016B								
Control Input voltage low V_{IL} max.	$V_{IS}=V_{SS}$, $V_{OS}=V_{DD}$		5	0.9	—	0.7	0.4	V
	$V_{IS}=V_{DD}$, $V_{OS}=V_{SS}$		10	0.9•	—	0.7	0.4•	
	$\lvert I_{IS}\rvert < 10\mu A$		15	0.9	—	0.7	0.4	
Control Input voltage high V_{IH} min.	—		5	3.5	3.5	—	3.5	V
			10	7.0•	7.0•	—	7.0•	
			15	11.0	11.0	—	11.0	
On-state resistance R_{ON} max. R_L = 10k returned to V_{DD}-V_{SS}/2	$V_{IS}=V_{DD}$ or V_{SS}		10	600	—	660	960	ohms
	V_{IS} = 4.75 or 5.75		10	1870	—	2000	2600	
	$V_{IS}=V_{DD}$ or V_{SS}		15	360	—	400	600	
	V_{IS} = 7.25 or 7.75		15	775	—	850	1230	
CD4031B								
Output low drive current I_{OL} min. Q	0.4	0,5	5	2.56•	2.04	—	1.44•	mA
	0.5	0,10	10	6.4•	5.2	—	3.6•	
	1.5	0,15	15	16.8•	13.6	—	9.6•	
$\overline{Q}$, Q', CLd	0.4	0,5	5	0.64•	0.51	—	0.36•	mA
	0.5	0,10	10	1.6•	1.3	—	0.9•	
	1.5	0,15	15	4.2•	3.4	—	2.4•	
Output high drive current I_{OH} min. Q, $\overline{Q}$, Q', CLd	4.6	0,5	5	-0.64•	-0.51	—	-0.36•	mA
	2.5	0,5	5	-2.0•	-1.6	—	-1.15•	
	9.5	0,10	10	-1.6•	-1.3	—	-0.9•	
	13.5	0,15	15	-4.2•	-3.4	—	-2.4•	
CD4041UB								
Output low drive current I_{OL} min.	0.4	0,5	5	2.1•	1.6	—	1.2•	mA
	0.5	0,10	10	6.25•	5	—	3.5•	
	1.5	0,15	15	24•	19	—	13•	
Output high drive current I_{OH} min.	4.6	0,5	5	-2.1•	-1.6	—	-1.2•	mA
	2.5	0,5	5	-8.4•	-6.4	—	-4.6•	
	9.5	0,10	10	-6.25•	-5.0	—	-3.5•	
	13.5	0,15	15	-24•	-19	—	-13•	

Limits with black dots (•) are tested 100%.

• These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

Non-Standard DC Electrical Characteristics (Continued)

Static Electrical Parameters	Conditions			Limits at Indicated Temperatures				Units
				-55°C	+25°C		+125°C	
	V_O	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD4046B								
Zener diode voltage (V_Z)	I_Z = 50 μA			—	4.45•	6.5•	—	V
Quiescent leakage phase comparator pin 14 open pin 5 = V_{DD}	—	0,5	5	0.2	—	0.2	—	mA
	—	0,10	10	1.0	—	1.0	—	
	—	0,15	15	1.5	—	1.5	—	
	—	0,20	20	4.0	—	4.0•	—	
Quiescent leakage phase comparator pin 14 = V_{SS} or V_{DD} pin 5 = V_{DD}	—	0,5	5	20	—	20	—	μA
	—	0,10	10	40	—	40	—	
	—	0,15	15	80	—	80	—	
	—	0,20	20	160	—	160•	—	
CD4049UB, CD4050B								
Output low drive current I_{OL} min.	0.4	0,5	4.5	3.3	2.6•	—	1.8	mA
	0.4	0,5	5	4.0	3.2•	—	2.4	
	0.5	0,10	10	10	8.0•	—	5.6	
	1.5	0,15	15	26	24•	—	18	
Output high drive current I_{OH} min.	4.6	0,5	5	-0.81	-0.8•	—	-0.48	mA
	2.5	0,5	5	-2.6	-3.2•	—	-1.55	
	9.5	0,10	10	-2.0	-1.8•	—	-1.18	
	13.5	0,15	15	-5.2	-6.0•	—	-3.1	
CD4051B, CD4052B, CD4053B, CD4067B, CD4097B								
On-state resistance R_{ON} max.	R_L = 10k returned to V_{DD}-V_{SS}/2 V_{IS} = V_{SS} to V_{DD}		5	800	—	1050•	1300•	ohms
			10	310	—	400•	500•	
			15	200	—	240•	320•	
Input voltage low V_{IL} max.	V_{EE} = V_{SS} R_L = 1k to V_{SS} $\lvert I_{IS} \rvert < 2\ \mu A$		5	1.5•	—	1.5•	1.5•	Volts
			10	3.0	—	3.0	3.0	
			15	4.0•	—	4.0•	4.0•	
Input voltage high V_{IH} min.	V_{EE} = V_{SS} R_L = 1k to V_{SS} $\lvert I_{IS} \rvert < 2\ \mu A$		5	3.5•	3.5•	—	3.5•	Volts
			10	7.0	7.0	—	7.0	
			15	11.0•	11.0•	—	11.0•	
Off channel leakage current Any channel off max.	V_{SS}-V	V_{EE}-V						
All channels (common out/in) off max.	0	0	18	± 100•	—	± 100•	± 1000•	nA

• These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

Non-Standard DC Electrical Characteristics (Continued)

Static Electrical Parameters	Conditions			Limits at Indicated Temperatures				Units
				-55°C	+25°C		+125°C	
	V_O	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD4066B								
On-state resistance R_{ON} max.	R_L = 10k returned to V_{DD}-V_{SS}/2 V_{IS} = V_{SS} to V_{DD}		5	800•	—	1050•	1300•	ohms
			10	310•	—	400•	550•	
			15	200•	—	240•	320•	
Control Input Voltage Low V_{ILC} max.	V_{IS} = V_{SS}, V_{OS} = V_{DD} V_{IS} = V_{DD}, V_{OS} = V_{SS} $\lvert I_{IS} \rvert < 10\mu A$		5	1.0•	—	1.0•	1.0•	Volts
			10	2.0	—	2.0	2.0	
			15	2.0•	—	2.0•	2.0•	
Control Input Voltage High V_{IHC} min.	—		5	3.5•	3.5•	—	3.5•	Volts
			10	7.0	7.0	—	7.0	
			15	11.0•	11.0•	—	11.0•	
Input output leakage current (switch off) Effective off resistance V_C = V_{SS}	0	0	18	± 100	—	± 100	± 1000	nA
CD4093B								
Positive Trigger Threshold Voltage V_P min.	—	a	5	2.2•	2.2•	—	2.2•	V
	—	a	10	4.6	4.6	—	4.6	
	—	a	15	6.8•	6.8•	—	6.8•	
	—	b	5	2.6•	2.6•	—	2.6•	
	—	b	10	5.6	5.6	—	5.6	
	—	b	15	6.3	6.3	—	6.3	
V_P max.	—	a	5	3.6•	—	3.6•	3.6•	V
	—	a	10	7.1	—	7.1	7.1	
	—	a	15	10.8•	—	10.8•	10.8•	
	—	b	5	4•	—	4•	4•	
	—	b	10	8.2	—	8.2	8.2	
	—	b	15	12.7	—	12.7	12.7	
Negative Trigger Threshold Voltage V_N min.	—	a	5	0.9•	0.9•	—	0.9•	V
	—	a	10	2.5	2.5	—	2.5	
	—	a	15	4•	4•	—	4•	
	—	b	5	1.4•	1.4•	—	1.4•	
	—	b	10	3.4	3.4	—	3.4	
	—	b	15	4.8	4.8	—	4.8	
V_N max.	—	a	5	2.8•	—	2.8•	2.8•	V
	—	a	10	5.2	—	5.2	5.2	
	—	a	15	7.4•	—	7.4•	7.4•	
	—	b	5	3.2•	—	3.2•	3.2•	
	—	b	10	6.6	—	6.6	6.6	
	—	b	15	9.6	—	9.6	9.6	
Hysteresis Voltage V_H min.	—	a	5	0.3•	0.3•	—	0.3•	V
	—	a	10	1.2	1.2	—	1.2	
	—	a	15	1.6•	1.6•	—	1.6•	
	—	b	5	0.3•	0.3•	—	0.3•	
	—	b	10	1.2	1.2	—	1.2	
	—	b	15	1.6	1.6	—	1.6	
V_H max.	—	a	5	1.6	—	1.6•	1.6•	V
	—	a	10	3.4	—	3.4	3.4	
	—	a	15	5•	—	5•	5•	
	—	b	5	1.6	—	1.6•	1.6•	
	—	b	10	3.4	—	3.4	3.4	
	—	b	15	5	—	5	5	

[a] Input on terminals 1, 5, 8, 12, or 2, 6, 9, 13; other inputs to V_{DD}.
[b] Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD}.

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Non-Standard DC Electrical Characteristics (Continued)

Static Electrical Parameters		Conditions			Limits at Indicated Temperatures				Units
					−55°C	+25°C		+125°C	
		V_O	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD4502B									
Output low drive current I_{OL} min.		0.4 0.5 1.5	0,5 0,10 0,15	5 10 15	3.84 9.6 25.2	3.06• 7.8• 20.4•	— — —	2.16 5.4 14.4	mA
CD4503B									
Output low drive current I_{OL} min.		0.4 0.5 1.5	0 0 0	5 10 15	2.6 6.5 19.2	2.1• 5.5• 16.1•	— — —	1.3 3.8 11.2	mA
Output high drive current I_{OH} min.		4.6 2.5 9.5 13.5	5 5 10 15	5 5 10 15	-1.2 -5.8 -3.1 -8.2	-1.02• -4.8• -2.6• -6.8•	— — — —	-0.7 -3.0 -1.8 -4.8	mA
CD4504B									
	V_{CC}								
Input low voltage V_{IL} max. TTL-CMOS	5	1	—	10	0.8	—	0.8	0.8	V
TTL-CMOS	5	1	—	15	0.8•	—	0.8•	0.8•	
CMOS-CMOS	5	1	—	10	1.5•	—	1.5•	1.5•	
CMOS-CMOS	5	1.5	—	15	1.5	—	1.5	1.5	
CMOS-CMOS	10	1.5	—	15	3•	—	3•	3•	
Input high voltage V_{IH} min. TTL-CMOS	5	9	—	10	2	2	—	2	
TTL-CMOS	5	13.5	—	15	2•	2•	—	2•	
CMOS-CMOS	5	9	—	10	3.5•	3.5•	—	3.5•	
CMOS-CMOS	5	13.5	—	15	3.5	3.5	—	3.5	
CMOS-CMOS	10	13.5	—	15	7•	7•	—	7•	
CD4511B									
Output voltage high-level V_{OH} min.		— — —	0, 5 0, 10 0, 15	5 10 15	4 9 14•	4.1 9.1 14.1•	— — —	4.2 9.2 14.2•	V
	I_{OH} (mA)								
Output drive voltage high level V_{OH} min.	0	—	—	5	4.0	4.10	—	4.20	V
	5	—	—	5	—	—	—	—	
	10	—	—	5	3.80	3.90	—	3.90	
	15	—	—	5	—	—	—	3.50	
	20	—	—	5	3.55	3.40•	—	—	
	25	—	—	5	3.40	3.10	—	—	
	0	—	—	10	9.0	9.10	—	9.20	V
	5	—	—	10	—	—	—	—	
	10	—	—	10	8.85	9.0	—	9.0	
	15	—	—	10	—	—	—	—	
	20	—	—	10	8.70	8.60•	—	8.40	
	25	—	—	10	8.60	8.30	—	—	
	0	—	—	15	14.0	14.10	—	14.20	V
	5	—	—	15	—	—	—	—	
	10	—	—	15	13.90	14.0	—	14.0	
	15	—	—	15	—	—	—	—	
	20	—	—	15	13.75	13.70•	—	13.50	
	25	—	—	15	13.65	13.50	—	—	

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Non-Standard DC Electrical Characteristics (Continued)

Static Electrical Parameters	Conditions			Limits at Indicated Temperatures				Units
				−55°C	+25°C		+125°C	
	V_O	V_{IN}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD40106B								
Positive trigger threshold voltage V_P min.	—	—	5	2.2•	2.2•	—	2.2•	V
	—	—	10	4.6•	4.6•	—	4.6•	
	—	—	15	6.8•	6.8•	—	6.8•	
V_P max.	—	—	5	3.6•	—	3.6•	3.6•	V
	—	—	10	7.1•	—	7.1•	7.1•	
	—	—	15	10.8•	—	10.8•	10.8•	
Negative trigger threshold voltage V_N min.	—	—	5	0.9•	0.9•	—	0.9•	V
	—	—	10	2.5•	2.5•	—	2.5•	
	—	—	15	4•	4•	—	4•	
V_N max.	—	—	5	2.8•	—	2.8•	2.8•	V
	—	—	10	5.2•	—	5.2•	5.2•	
	—	—	15	7.4•	—	7.4•	7.4•	
Hysteresis voltage V_H min.	—	—	5	0.3•	0.3•	—	0.3•	V
	—	—	10	1.2•	1.2•	—	1.2•	
	—	—	15	1.6•	1.6•	—	1.6•	
V_H max.	—	—	5	1.6•	—	1.6•	1.6•	V
	—	—	10	3.4•	—	3.4•	3.4•	
	—	—	15	5•	—	5•	5•	
CD40107B								
Output low current I_{OL} min.	0.4	0,5	5	21	16•	—	12	mA
	1	0,5	5	44	34•	—	25	
	0.5	0,10	10	49	37•	—	28	
	1	0,10	10	89	68•	—	51	
	0.5	0,15	15	66	50•	—	38	
Output high current I_{OH} min.	NO INTERNAL PULL-UP DEVICE							
Input low voltage V_{IL} max. *	4.5	—	5	1.5•	—	1.5•	1.5•	V
	9	—	10	3	—	3	3	
	13.5	—	15	4•	—	4•	4•	
Input high voltage V_{IH} min. *	0.5, 4.5	—	5	3.5•	3.5•	—	3.5•	V
	1,9	—	10	7	7	—	7	
	1.5, 13.5	—	15	11•	11•	—	11•	

* Measured with external pull-up resistor, R_L = 10kΩ to V_{DD}

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† At −55°C test is performed with V_{DD} of 18V

Non-Standard DC Electrical Characteristics (Continued)

Static Electrical Parameters	Conditions			Limits at Indicated Temperatures				Units
				−55°C	+25°C		+125°C	
	V_O	V_{CC}	V_{DD}	Min./Max.	Min.	Max.	Min./Max.	
CD40109B								
Input low voltage V_{IL} max.	1,9 1.5, 13.5	5 10	10 15	1.5• 3•	— —	1.5• 3•	1.5• 3•	V
Input high voltage V_{IH} max.	1,9 1.5, 13.5	5 10	10 15	3.5• 7•	3.5• 7•	— —	3.5• 7•	V
CD40110B								
	I_{OH}	V_{OH}	V_{IN}	V_{DD}				
Output Voltage Low-Level V_{OL} max.	— — —	— — —	0,5 0,10 0,15	5 10 15	0.05 0.05 0.05•	— — —	0.05 0.05 0.05•	0.05 0.05 0.05•	V
High-Level V_{OH} min.	— — —	— — —	0,5 0,10 0,15	5 10 15	— — —	— — —	— — —	— — —	V
	■ -5 -10 -15 -20 -25	— — — — — —	— — — — — —	5 5 5 5 5 5	3.9 3.65 3.55 3.5 3.45 3.4	3.9 3.7 3.65 3.6 3.45• 3.4	— — — — — —	4 3.7 3.65 3.5 3.35 3.3	V
7-Segment Outputs Output Drive Voltage, High V_{OH} min.	■ -5 -10 -15 -20 -25	— — — — — —	— — — — — —	10 10 10 10 10 10	8.75 8.45 8.42 8.4 8.4 8.3	8.75 8.55 8.5 8.47 8.45• 8.3	— — — — — —	8.85 8.55 8.5 8.47 8.40 8.25	V
	■ -5 -10 -15 -20 -25	— — — — — —	— — — — — —	15 15 15 15 15 15	13.8 13.65 13.6 13.6 13.6 13.3	13.8 13.75 13.72 13.7 13.65• 13.3	— — — — — —	13.9 13.75 13.72 13.7 13.6 13.25	V
7-Segment Outputs Output Low (Sink) Current I_{OL} min.	— — —	0.4 0.5 1.5	0,5 0,10 0,15	5 10 15	1.28 3.2 8.4	1• 2.6• 6.8•	— — —	0.72 1.8 4.8	mA

• These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

■ 0 (10μA)

Switching Characteristics at 25°C

The chart below lists all Harris high reliability CD4000B-series devices and shows which switching parameters are 100% tested at final electrical and Group A. In general, Harris tests propagation delay, transition time, and maximum clock frequency at 5V where applicable. Harris warrants all other switching parameters shown in the appropriate commercial data sheet. Harris high reliability switching tests are performed on a one-input to one-output basis only.

TYPE	CONDITIONS* V_{DD} = 5V, C_L = 50pF	PROP DELAY (ns)	TRANS. TIME (ns)	MAX CLOCK INPUT FREQ. (MHz)
CD4000B	-	250	200	-
CD4001B	-	250	200	-
CD4002B	-	250	200	-
CD4006B	-	400	200	2.5
CD4007UB	-	110	200	-
CD4008B	Sum In to Sum Out	800	200	-
	Carry In to Sum Out	740	-	-
	Sum In to Carry Out	400	-	-
	Carry In to Carry Out	200	-	-
CD4009UB	-	140*	350*	-
	-	60▲	70▲	-
CD4010B	-	200*	350*	-
	-	130▲	70▲	-
CD4011B	-	250	200	-
CD4012B	-	250	200	-
CD4013B	Clock to Q or $\overline{Q}$	300	200	3.5
	Set to Q or Reset to $\overline{Q}$	300*	-	-
	Set to $\overline{Q}$ or Reset to Q	400▲	-	-
CD4014B	-	320	200	3
CD4015B	Clock to Q	320	200	3
	Reset to Q	400▲	-	-
CD4016B	Sig. Input to Sig. Output	100	-	-
	Turn On	70	-	-
CD4017B	Clock to Out	650	200	2.5
	Clock to Carry Out	600	-	-
	Reset to Out	530	-	-
CD4018B	Clock to Q	400	200	3
	Preset/Reset to Q	550	-	-
CD4019B	-	300	200	-
CD4020B	ϕ to Q1	360	200	3.5
	Qn to Qn + 1	330	-	-
	Reset to Q	280▲	-	-
CD4021B	-	320	200	3
CD4022B	Clock to Carry Out	600	200	2.5
	Clock to Decode Out	650	-	-
	Reset to Output	530	-	-
CD4023B	-	250	200	-

TYPE	CONDITIONS* V_{DD} = 5V, C_L = 50pF	PROP DELAY (ns)	TRANS. TIME (ns)	MAX CLOCK INPUT FREQ. (MHz)
CD4024B	ϕ to Q1	360	200	3.5
	Qn to Qn + 1	330	-	-
	Reset to Q	280▲	-	-
CD4025B	-	250	200	-
CD4026B	Clock to Carry Out	500	200	2.5
	Clock to Decode Out	700	-	-
	Reset to Carry Out	550*	-	-
	Reset to Decode Out	600	-	-
CD4027B	Clock to Q or $\overline{Q}$	300	200	3.5
	Set to Q or Reset to $\overline{Q}$	300*	-	-
	Set to $\overline{Q}$ or Reset to Q	400▲	-	-
CD4028B	-	350	200	-
CD4029B	Q Output	500	200	2
	Carry Output	560	-	-
	Preset Enable to Q	470	-	-
	Preset Enable to Carry Out	640	-	-
	Carry Input to Carry Out	340	-	-
CD4030B	-	280	200	-
CD4031B	Clock to $\overline{Q}$	500	200	2
	Clock to Q	500*	-	-
	Clock to Q	380▲	-	-
	Clock to Q'	380	-	-
	$\overline{\text{Clock}}$ to CL_D	200	-	-
CD4033B	Clock to Carry Out	500	200	2.5
	Clock to Decode Out	700	-	-
	Reset to Carry Out	550*	-	-
	Reset to Decode Out	600	-	-
CD4034B	Parallel In to Parallel Out	700	200	2
	AE to "A" Out t_{PLZ}, t_{PZL}, t_{PHZ}, t_{PZH}	400	-	-
CD4035B	Clock to Q	500	200	2
	Reset to Q	460	-	-
CD4040B	ϕ to Q1	360	200	3.5
	Qn to Qn + 1	330	-	-
	Reset to Q	280▲	-	-
CD4041UB	-	120	80	-

* t_{TLH} or t_{PLH} ▲ t_{THL} or t_{PHL}

Switching Characteristics at 25°C

TYPE	CONDITIONS* V_{DD} = 5V, C_L = 50pF	PROP. DELAY (ns)	TRANS. TIME (ns)	MAX. CLOCK INPUT FREQ. (MHz)
CD4042B	Data In to Q	220	200	–
	Data In to $\overline{Q}$	300	–	–
	Clock to Q	450	–	–
	Clock to $\overline{Q}$	500	–	–
CD4043B, 44B	Set or Reset to Q	300	200	–
	Enable to Q – t_{PHZ}, t_{PZH}	230	–	–
	Enable to Q – t_{PLZ}, t_{PZL}	180	–	–
CD4046B	AC Coupled Signal Input Voltage Sensitivity (Peak to Peak) f_{IN} = 100kHz Sine Wave	360mV Max		
CD4047B	t_R to Q, $\overline{Q}$	1000	200	–
	Astable to Q, $\overline{Q}$	700	–	–
	Retrigger to Q, $\overline{Q}$	600	–	–
	Astable to Oscillator	400	–	–
	Reset to Q, $\overline{Q}$	500	–	–
CD4048B	Ka to Output	600	200	–
CD4049UB	–	120*	160*	–
	–	65▲	60▲	–
CD4050B	–	140*	160*	–
	–	110▲	60▲	–
CD4051B, 52B, 53B	Add to Signal Out	720	–	–
	Inhibit to Signal Out – Channel On	720	–	–
	Inhibit to Signal Out – Channel Off	450	–	–
CD4060B	Input Pulse Operation ϕ1 to Q4	740	200	3.5
	Qn to Qn = 1	200	–	–
	Reset Operation	360▲	–	–
CD4063B	Comparator Input to Output	1250	200	–
	Cascade Input to Output	1000	–	–
CD4066B	Signal Input to Signal Output R_L = 200k, $V_C = V_{DD}$, V_{SS} = GND, V_{IS} = Square Wave ≃ 5V and t_r, t_f = 20ns	40	–	–
	t_{pdc} t_{rc}, t_{fc} = 20ns, R_L = 1k & V_{IS} < 5V	70	–	–
CD4067B	Add or inhibit to Signal Out Channel On	650	–	–
	Signal In to Out	60	–	–
CD4068B	–	300	200	–
CD4070B	–	280	200	–

TYPE	CONDITIONS* V_{DD} = 5V, C_L = 50pF	PROP. DELAY (ns)	TRANS. TIME (ns)	MAX. CLOCK INPUT FREQ. (MHz)
CD4071B, 72B, 73B, 75B	–	250	200	–
CD4076B	Clock to Q	600	200	–
CD4077B	–	280	200	–
CD4078B	–	300	200	3
CD4081B, 82B	–	250	200	–
CD4085B, 86B	Data	450▲	200	–
		620*	–	–
	Inhibit	300▲	–	–
		500*	–	–
CD4089B	Clock to Out	300	200	1.2
	Clear to Out	760	–	–
	Cascade to Out	180	–	–
CD4093B	–	380	200	–
CD4094B	Clock to Serial Out Qs	600	200	1.25
	Clock to Serial Out Q's	460	–	–
	Clock to Parallel Out	840	–	–
	Strobe to Parallel Out	580	–	–
	Out Enable to Parallel Out, t_{PHZ}, t_{PZH}	280	–	–
	Out Enable to Parallel Out, t_{PLZ}, t_{PZL}	200	–	–
CD4095B, 96B	Clock to Output	500	200	3.5
	Set or Reset	300	–	–
CD4097B	Address or Inhibit to Sig. Out – Channel On	650	–	–
	Signal In to Out	60	–	–
CD4098B	Trigger to Q, $\overline{Q}$	500	200	–
CD4099B	Data to Output	400	200	–
CD4502B	Data or Inhibit Delay Time	380*	200*	
		270▲	120▲	–
	Disable Delay Time – t_{PHZ}	120	–	–
	Disable Delay Time – t_{PZH}	220	–	–
	Disable Delay Time – t_{PLZ}, t_{PZL}	250	–	–
CD4503B	–	150*	90*	–
	–	110▲	70▲	–
	t_{PHZ}, t_{PZH}	140	–	–
	t_{PLZ}, t_{PZL}	180	–	–

* t_{TLH} or t_{PLH} ▲ t_{THL} or t_{PHL}

Switching Characteristics at 25°C

TYPE	CONDITIONS* V_{DD} = 5V, C_L = 50pF			PROP. DELAY (ns)	TRANS. TIME (ns)	MAX. CLOCK INPUT FREQ. (MHz)
CD4504B	SHIFT MODE	V_{CC}	V_{DD}			
	TTL to CMOS $V_{DD} > V_{CC}$	5	10	280▲	–	–
	CMOS to CMOS $V_{DD} > V_{CC}$	5	10	240▲	–	–
	CMOS to CMOS $V_{CC} > V_{DD}$	10	5	550▲	–	–
	TTL to CMOS $V_{DD} > V_{CC}$	5	10	280*	–	–
	CMOS to CMOS $V_{DD} > V_{CC}$	5	10	240*	–	–
	CMOS to CMOS $V_{CC} > V_{DD}$	10	5	400*	–	–
	All Modes	–	5	200	–	–
	t_{THL}, t_{TLH}	–	10	100	–	–
CD4508B	Strobe In to Data Out			260	200	–
CD4510B	Clock to Q Output			400	200	2
	Preset or Reset to Q			420	–	–
	Clock to Carry Out			480	–	–
	Carry In to Carry Out			250	–	–
	Preset or Reset to Carry Out			640	–	–
CD4511B	Data to Output			1040▲	310▲	–
	–			1320*	80*	–
CD4512B	Inhibit to Output			280	200	–
	"A" Select to Output			400	–	–
	Data to Output			360	–	–
	t_{PHZ}, t_{PZH}			120	–	–
CD4514B, 15B	Strobe or Data			970	200	–
	Inhibit			500	–	–
CD4516B	Clock to Q Output			400	200	2
	Preset or Reset to Q			420	–	–
	Clock to Carry Out			480	–	–
	Carry In to Carry Out			250	–	–
	Preset or Reset to Carry Out			640	–	–
CD4517B	Clock to Q16			400	200	3
CD4518B, 20B	Clock to Output			560	200	1.5
	Reset to Output			650▲	–	–
CD4527B	Clock to Out			300	200	1.2
	Clear to Out			760	–	–
	Cascade to Out			180	–	–
CD4532B	E_I to E_O, E_I to Gs			220	200	–
	Dn to Qm			440	–	–
	Dn to Gs, E_1 to Qm			340	–	–

TYPE	CONDITIONS* V_{DD} = 5V, C_L = 50pF	PROP. DELAY (ns)	TRANS. TIME (ns)	MAX. CLOCK INPUT FREQ. (MHz)
CD4536B	Clock to Q1 8 Bypass High	2000	200	0.5
	Clock to Q1 8 Bypass Low	5000	–	–
	Clock to Q16	8000	–	–
	Reset to Qn	6000▲	–	–
CD4555B, 56B	Select to Any Output	440	200	–
	$\overline{\text{Enable}}$ to Any Output	400	–	–
CD4585B	Comparator Inputs to Outputs	600	200	–
	Cascade Inputs to Outputs	400	–	–
CD4724B	Data to Outputs	400	200	–
	Write Disable to Output	400	–	–
	Reset to Output	350▲	–	–
	Address to Output	450	–	–
CD1438B	Trigger to Q, $\overline{Q}$	600	200	–
	Reset to Q or $\overline{Q}$	500	–	–
CD40100B	–	720	200	1
CD40101B	Data In to Output	700	200	–
	Inhibit In to Output	280	–	–
CD40102B, 103B	Clock to Output	600	200	0.7
	Carry In/Counter Enable to Output	400	–	–
	Asynchronous Preset Enable to Output	1300*	–	–
	$\overline{\text{Clear}}$ to Output	750▲	–	–
CD40104B	Clock to Q	440	200	3
	t_{PZH}, t_{PLZ}, t_{PZL}	160	–	–
	t_{PHZ}	90	–	–
CD40105B	Shift Out or Reset to Data Out Ready	370▲	200	1.5
	Shift In to Data In Ready	320▲	–	–
	3-State Control to Data Out t_{PZH}	280	–	–
	Ripple Thru Delay Input to Out t_{PLH}	4000*	–	–
CD40106B	–	280	200	–
CD40107B	R_L = 120Ω	200	100	–
CD40108B	Clock or Write Enable to Q	720	200	1.5
	Read or Write Address to Q	600	–	–
	Disable Delay Time t_{PZH}, t_{PHZ}	200	–	–
	Disable Delay Time t_{PZL}, t_{PLZ}	260	–	–

* t_{TLH} or t_{PLH} ▲ t_{THL} or t_{PHL}

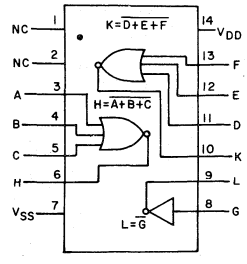
Switching Characteristics at 25°C

TYPE	CONDITIONS* V_{DD} = 5V, C_L = 50pF				PROP. DELAY (ns)	TRANS. TIME (ns)	MAX. CLOCK INPUT FREQ. (MHz)
CD40109B	Data Input to Output						
	SHIFT MODE		V_{CC}	V_{DD}			
	L-H		5V	10V	600▲	100	–
	L-H		5V	10V	260*	–	–
	H-L		10V	5V	500▲	200	–
	H-L		10V	5V	460*	–	–
	3-State Disable Delay R_L = 1kΩ						
		SHIFT MODE	V_{CC}	V_{DD}			
	t_{PHZ}	L-H	5V	10V	120	–	–
	t_{PHZ}	H-L	10V	5V	400	–	–
	t_{PLZ}	L-H	5V	10V	740	–	–
	t_{PLZ}	H-L	10V	5V	500	–	–
	t_{PZH}	L-H	5V	10V	–	–	–
	t_{PZH}	H-L	10V	5V	600	–	–
	t_{PZL}	L-H	5V	10V	200	–	–
	t_{PZL}	H-L	10V	5V	400	–	–
CD40110B	Clock to Carry or Borrow				600	–	1.0
CD40147B	In-Phase Output				900	200	–
CD40160B, 161B, 162B, 163B	Clock to Q				400	200	2
	Clock to C_{OUT}				450	–	–
	T_E to C_{OUT}				250	–	–
	Clear to Q (CD40160B & CD 40161B only)				500▲	–	–
CD40174B	Clock to Output				300	200	3.5
	$\overline{\text{Clear}}$ to Output				200▲	–	–
CD40175B	Clock to Q Output				400	200	2.0
	Clear to Q Output				500▲	–	–

* t_{TLH} or t_{PLH} ▲ t_{THL} or t_{PHL}

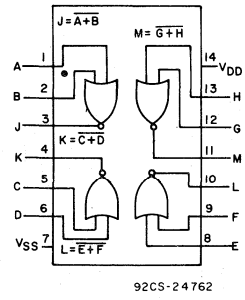
TYPE	CONDITIONS* V_{DD} = 5V, C_L = 50pF	PROP. DELAY (ns)	TRANS. TIME (ns)	MAX. CLOCK INPUT FREQ. (MHz)
CD40181B	A or B to F (Logic Mode) A or B to G or P	800	200	–
	A or B to F, Cn + 4, or A = B	1000	–	–
	Cn to F	640	–	–
	Cn to Cn + 4	400	–	–
CD40182B	P, G_{IN} to P, G_{OUT} and Carry Outs	400	200	–
	Cn to Carry Outs	480	–	–
CD40192B, 193B	Clock Up or Clock Down to Q, Reset Q	500	200	2
	$\overline{\text{PE}}$ to Q	400	–	–
	Clock Up to Carry, Clock Down to $\overline{\text{Borrow}}$	320	–	–
	Reset or PE to $\overline{\text{Borrow}}$ or $\overline{\text{Carry}}$	600	–	–
CD40194B	Clock to Q	440	200	3
	Reset to Q	460▲	–	–
CD40208B	Clock or Write Enable to Q	720	200	1.5
	Read or Write Address to Q	600	–	–
	3-State Disable Delay Time t_{PZH}, t_{PHZ}	200	–	–
	t_{PZL}, t_{PLZ}	260	–	–
CD40257B	Data Input to Output	300	200	–
	Select to Output	380	–	–
	Output Disable to Output	–	–	–
	t_{PZH}, t_{PHZ}	190	–	–
	t_{PZL}, t_{PLZ}	190	–	–

Functional Diagrams



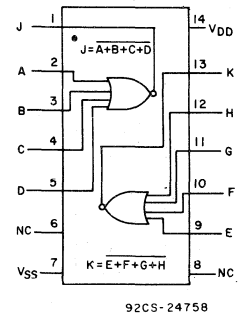
Dual 3-Input NOR Gate Plus Inverter

CD4000B (File No. 985)



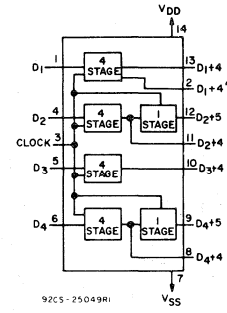
Quad 2-Input NOR Gate

CD4001B (File No. 985) (File No. 945)



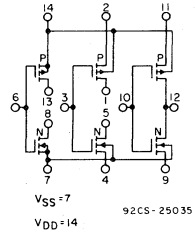
Dual 4-Input NOR Gate

CD4002B (File No. 985)



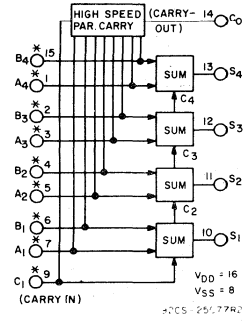
18-Stage Static Shift Register

CD4006B (File No. 1033)



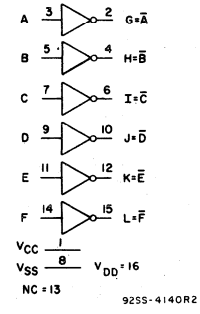
Dual Complementary Pair Plus Inverter

CD4007UB (File No. 977)



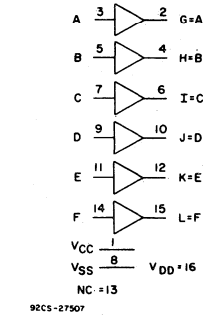
4-Bit Full Adder with Parallel Carry Out

CD4008B (File No. 951)



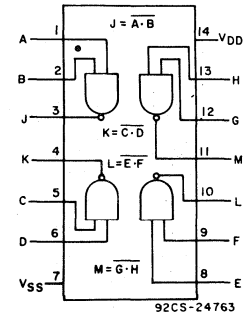
Hex Buffer/Converter Inverting Type

CD4009UB (File No. 940)



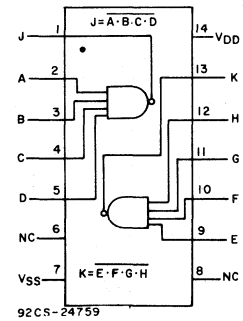
Hex Buffer/Converter Non-Inverting Type

CD4010B (File No. 940)



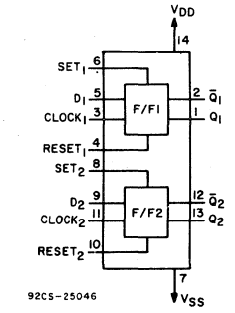
Quad 2-Input NAND Gate

CD4011B (File No. 986)



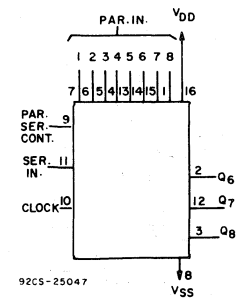
Dual 4-Input NAND Gate

CD4012B (File No. 986)



Dual "D" Flip-Flop with Set/Reset Capability

CD4013B (File No. 936)

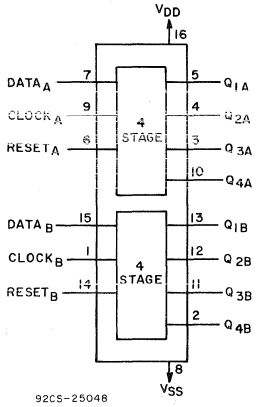


8-State Synchronous Shift Register with Parallel or Serial Input/Serial Output

CD4014B (File No. 1043)

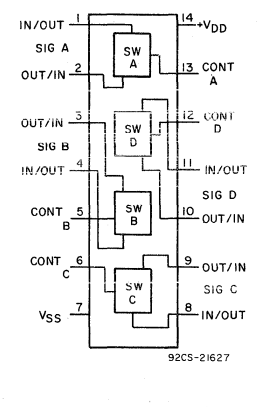
File No. = commercial data sheet

Functional Diagrams



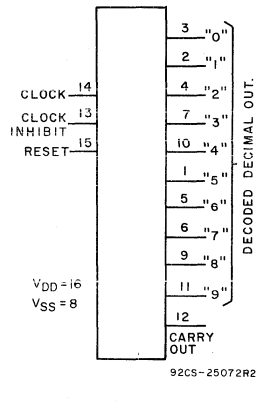
Dual 4-Stage Static Shift Register with Serial Input/Parallel Output

CD4015B (File No. 1024)



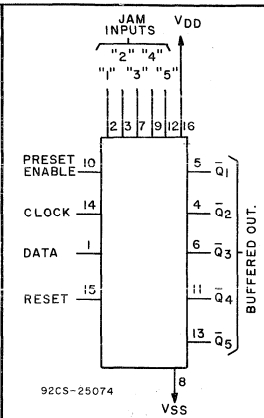
Quad Bilateral Switch

CD4016B (File No. 953)



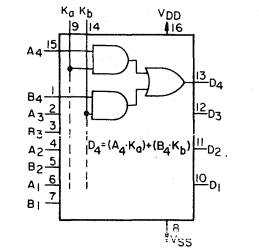
Decade Counter/Divider with 10 Decoded Decimal Outputs

CD4017B (File No. 1113)



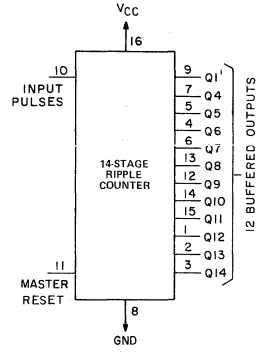
Presettable Divide-by-"N" Counter Fixed or Programmable

CD4018B (File No. 1034)



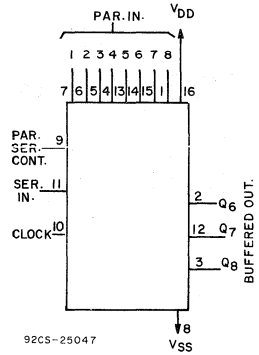
Quad AND/OR Select Gate

CD4019B (File No. 1045)



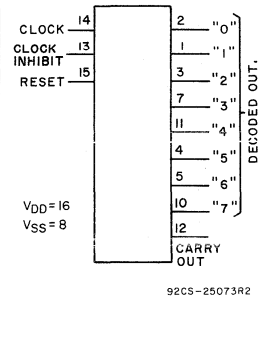
14-Stage Binary Ripple Counter

CD4020B (File No. 1063)



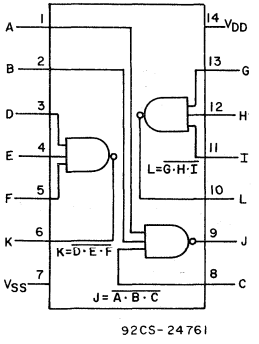
8-Stage Static Shift Register Asynchronous Parallel or Synchronous Serial Input/ Serial Output

CD4021B (File No. 1043)



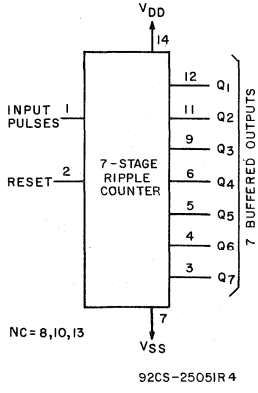
Divide-by-8 Counter/Divider with 8 Decoded Decimal Outputs

CD4022B (File No. 1113)



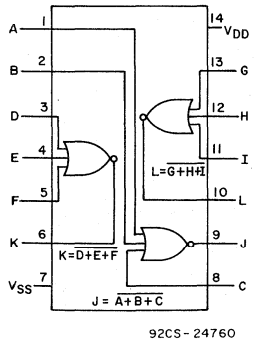
Triple 3-Input NAND Gate

CD4023B (File No. 986)



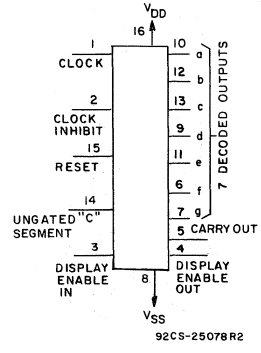
7-Stage Ripple-Carry Binary Counter/Divider

CD4024B (File No. 1063)



Triple 3-Input NOR Gate

CD4025B (File No. 985)

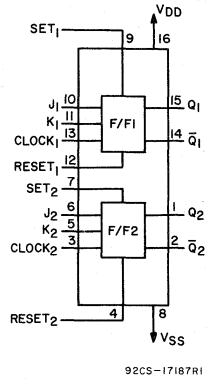


Decade Counter/Divider with 7-Segment Display Output and Display Enable

CD4026B (File No. 1118)

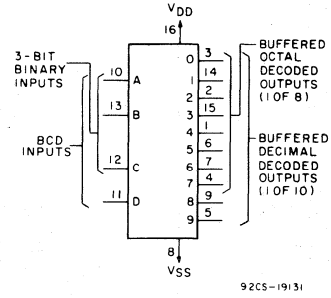
File No. = commercial data sheet

Functional Diagrams



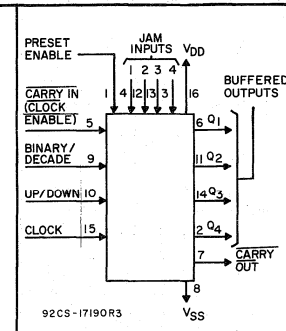
Dual J-K Master-Slave Flip-Flop with Set-Reset Capability

CD4027B (File No. 942)



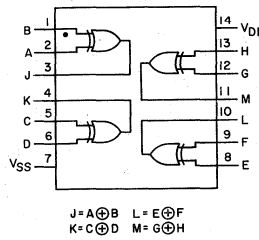
BCD-to-Decimal Decoder

CD4028B (File No. 1016)



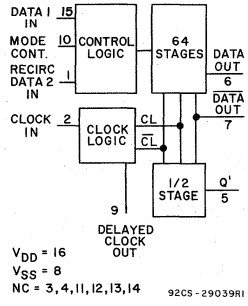
Presettable Up/Down Counter, Binary or BCD-Decade

CD4029B (File No. 1028)



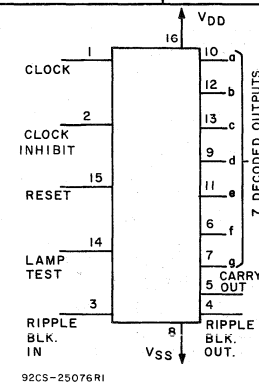
Quad Exclusive-OR Gate

CD4030B (File No. 1055)



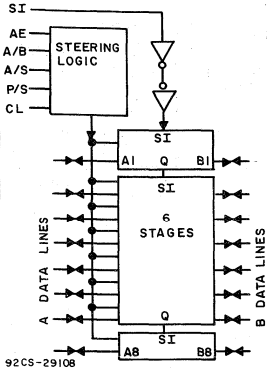
64-Stage Static Shift Register

CD4031B (File No. 1073)



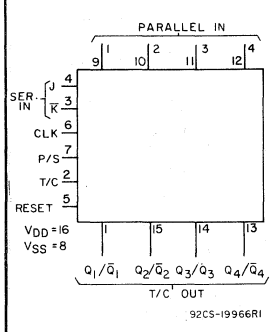
Decade Counter/Divider with 7-Segment Display Outputs and Ripple Blanking

CD4033B (File No. 1118)



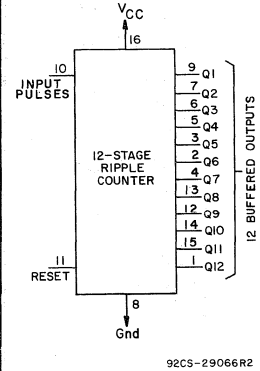
8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

CD4034B (File No. 1062)



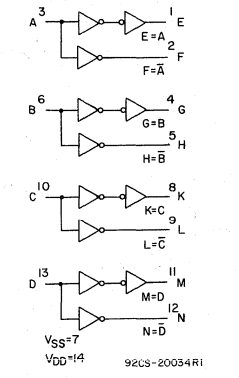
4-Stage Parallel In/Parallel Out Shift Register with J-K Serial Inputs and True/ Complement Outputs

CD4035B (File No. 1101)



12-Stage Ripple-Carry Binary Counter/Divider

CD4040B (File No. 1063)

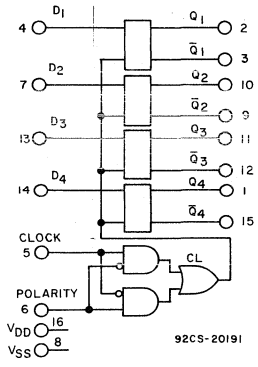


Quad True/Complement Buffer

CD4041UB (File No. 934)

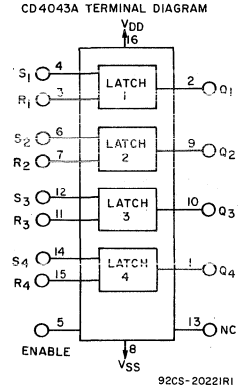
File No. = commercial data sheet

Functional Diagrams



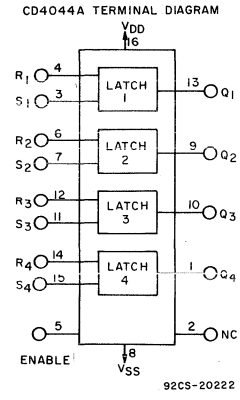
Quad Clocked "D" Latch

CD4042B (File No. 954)



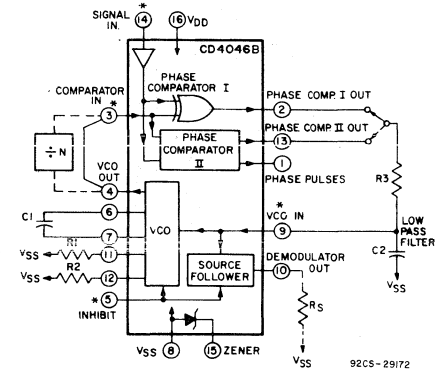
Quad 3-State NOR R/S Latch

CD4043B (File No. 956)



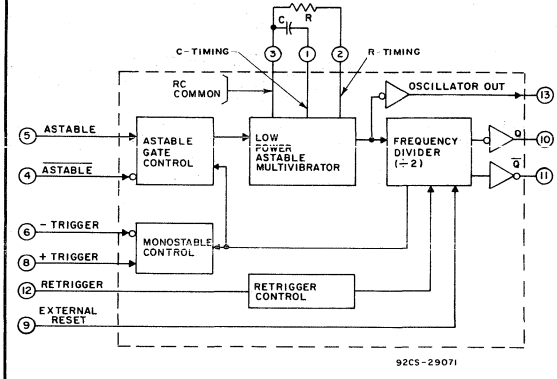
Quad 3-State NAND R/S Latch

CD4044B (File No. 956)



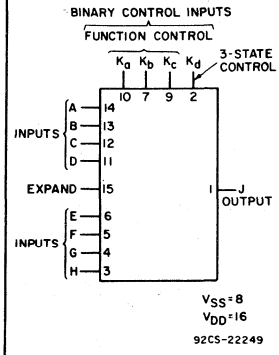
Micropower Phase-Locked Loop

CD4046B (File No. 1099)



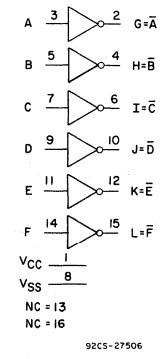
Low-Power Monostable/Astable Multivibrator

CD4047B (File No. 1123)



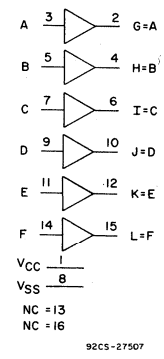
Multi-Function Expandable 8-Input Gate

CD4048B (File No. 1124)



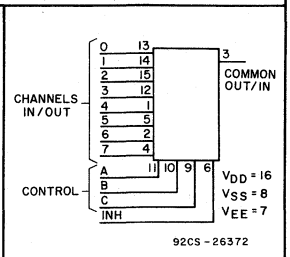
Hex Buffer/Converter Inverting Type

CD4049UB (File No. 926)



Hex Buffer/Converter Non-Inverting Type

CD4050B (File No. 926)

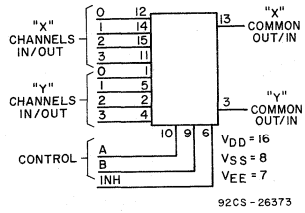


Single 8-Channel Analog Multiplexer/Demultiplexer

CD4051B (File No. 902)

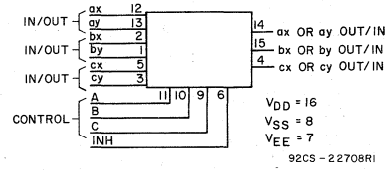
File No. = commercial data sheet

Functional Diagrams



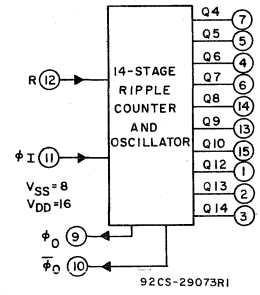
Differential 4-Channel Analog Multiplexer/Demultiplexer

CD4052B (File No. 902)



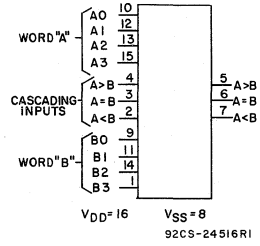
Triple 2-Channel Multiplexer/Demultiplexer

CD4053B (File No. 902)



14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

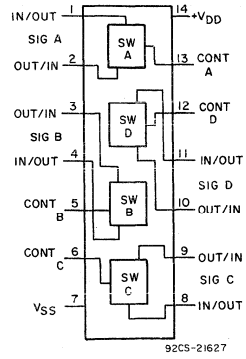
CD4060B (File No. 1120)



4-Bit Magnitude Comparator

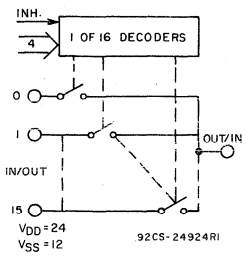
CD4063B (File No. 805)

Functional Diagrams



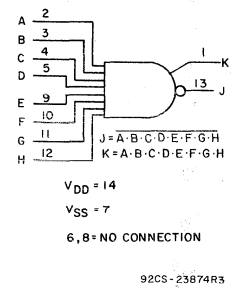
Quad Bilateral Switch

CD4066B (File No. 1114)



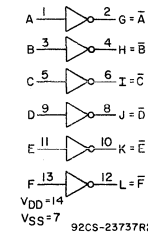
16-Channel Multiplexer/Demultiplexer

CD4067B (File No. 909)



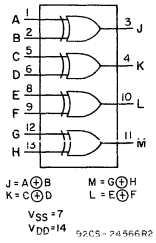
8-Input NAND/AND Gate

CD4068B (File No. 809)



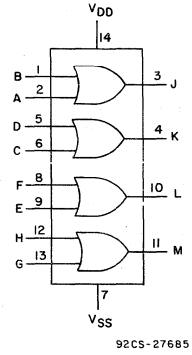
Hex Inverter

CD4069UB (File No. 804)



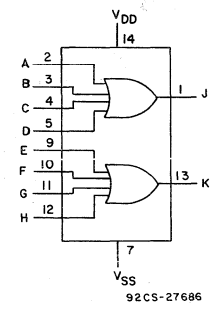
Quad Exclusive-OR Gate

CD4070B (File No. 910)



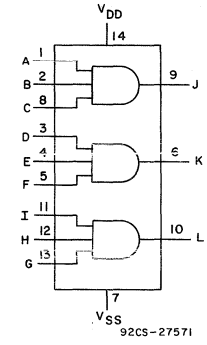
Quad 2-Input OR Gate

CD4071B (File No. 807)



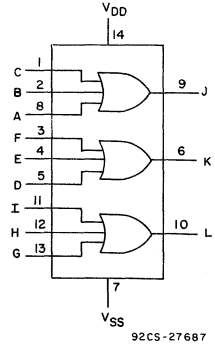
Dual 4-Input OR Gate

CD4072B (File No. 807)



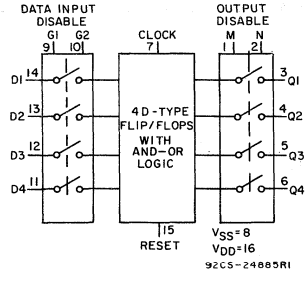
Triple 3-Input AND Gate

CD4073B (File No. 806)



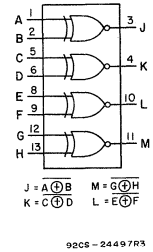
Triple 3-Input OR Gate

CD4075B (File No. 807)



4-Bit D-Type Register

CD4076B (File No. 903)

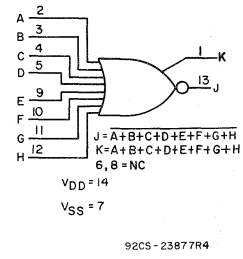


Quad Exclusive-NOR Gate

CD4077B (File No. 910)

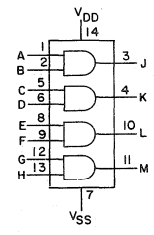
File No. = commercial data sheet

Functional Diagrams



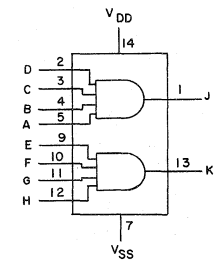
8-Input NOR/OR Gate

CD4078B (File No. 810)



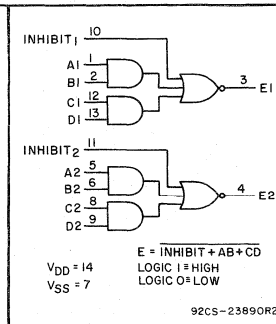
Quad 2-Input AND Gate

CD4081B (File No. 806)



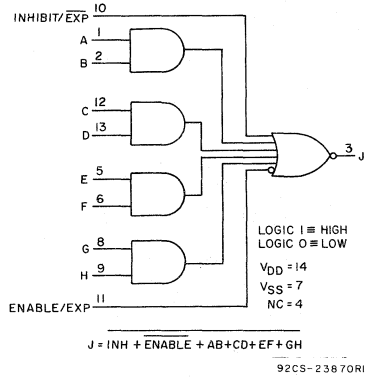
Dual 4-Input AND Gate

CD4082B (File No. 806)



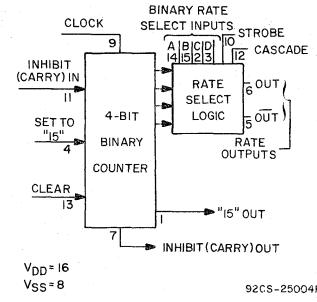
Dual 2-Wide, 2-Input AND-OR-INVERT (AOI) Gate

CD4085B (File No. 811)



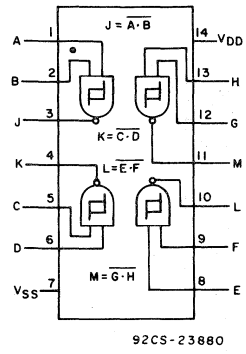
Expandable 4-Wide, 2-Input AND-OR-INVERT (AOI) Gate

CD4086B (File No. 812)



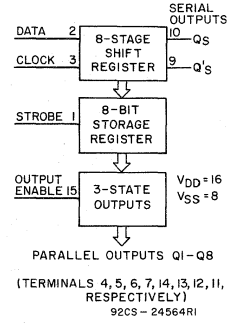
Binary Rate Multiplier

CD4089B (File No. 1003)



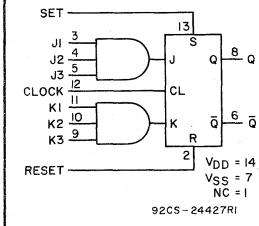
Quad 2-Input NAND Schmitt Trigger

CD4093B (File No. 836)



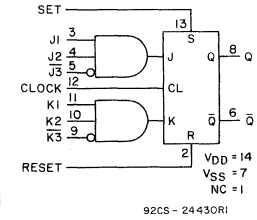
8-Stage Shift-and-Store Bus Register

CD4094B (File No. 869)



Gated J-K Master-Slave Flip-Flop, Non-Inverting Inputs

CD4095B (File No. 879)

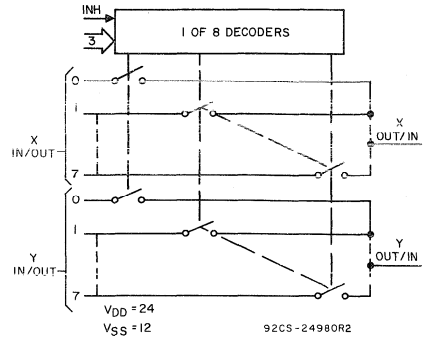


Gated J-K Master-Slave Flip-Flop, Inverting and Non-Inverting Inputs

CD4096B (File No. 879)

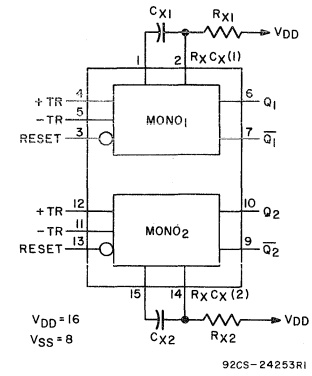
File No. = commercial data sheet

Functional Diagrams



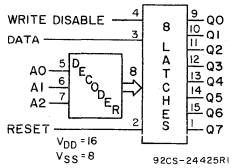
Differential 8-Channel Multiplexer/Demultiplexer

CD4097B (File No. 909)



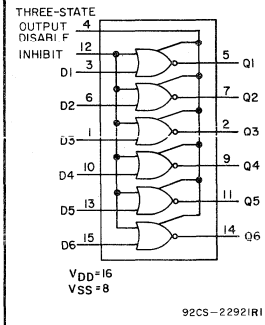
Dual Monostable Multivibrator

CD4098B (File No. 979)



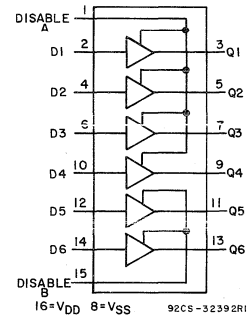
8-Bit Addressable Latch

CD4099B (File No. 948)



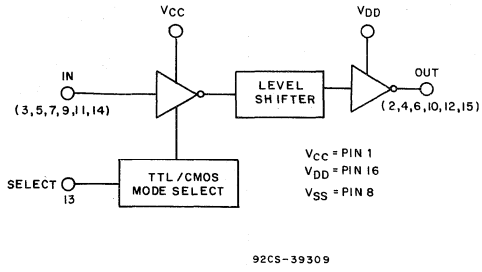
Strobed Hex Inverter/Buffer

CD4502B (File No. 1002)



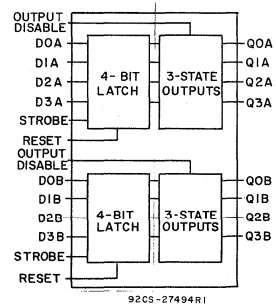
Hex Buffer Non-Inverting Type

CD4503B (File No. 1224)



Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

CD4504B (File No. 1846)

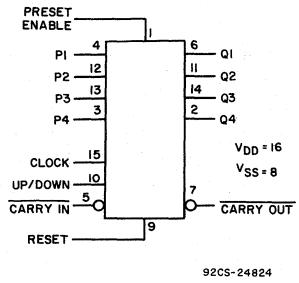


Dual 4-Bit Latch

CD4508B (File No. 1009)

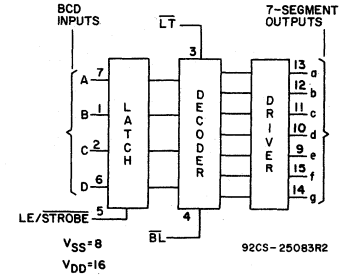
File No. = commercial data sheet

Functional Diagrams



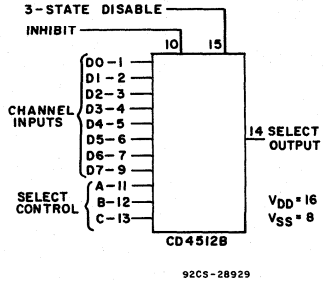
BCD Presettable Up/Down Counter

CD4510B (File No. 899)



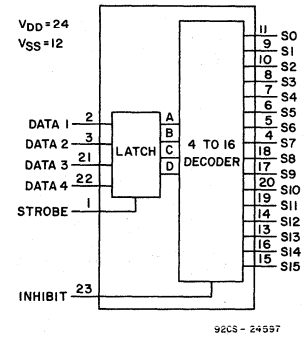
BCD-to-7-Segment Latch Decoder Driver

CD4511B (File No. 901)



8-Channel Data Selector

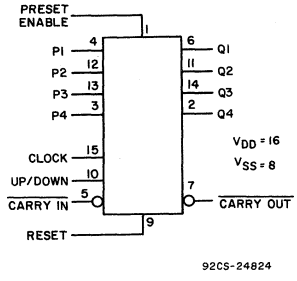
CD4512B (File No. 1032)



4-Bit Latch/4-to-16 Line Decoder

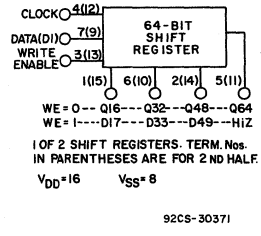
CD4514B (File No. 814) Output "High" on Select

CD4515B (File No. 814) Output "Low" on Select



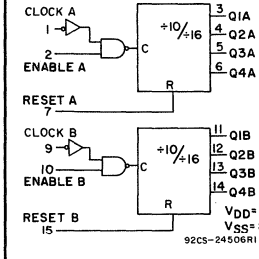
Binary Presettable Up/Down Counter

CD4516B (File No. 899)



Dual 64-Bit Shift Register

CD4517B (File No. 1148)



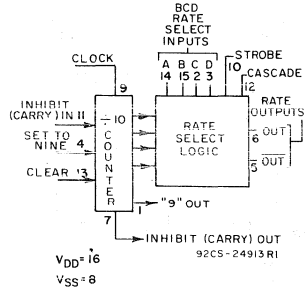
Dual Up Counter

CD4518B (File No. 808) BCD

CD4520B (File No. 808) Binary

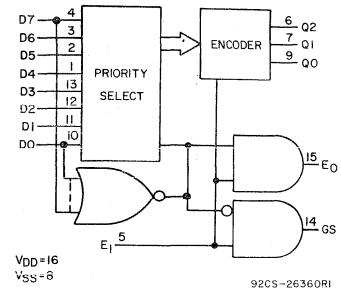
File No. = commercial data sheet

Functional Diagrams



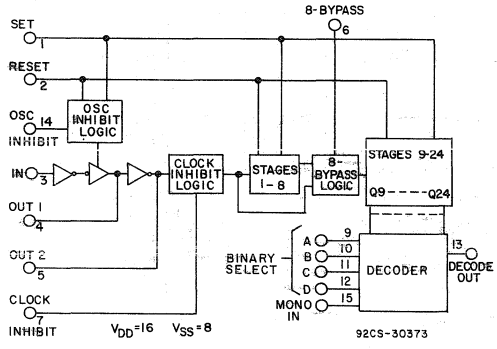
BCD Rate Multiplier

CD4527B (File No. 1006)



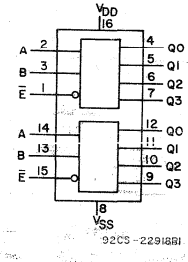
8-Bit Priority Encoder

CD4532B (File No. 876)



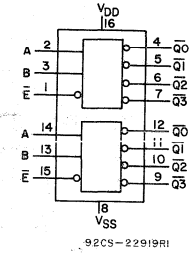
Programmable Timer

CD4536B (File No. 1186)



Dual Binary-to-1-of-4 Decoder/Demultiplexer Output "High" on Select

CD4555B (File No. 858)

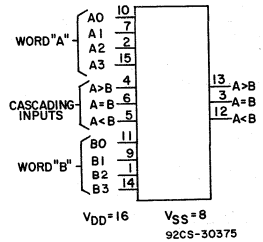


Dual Binary-to-1-of-4 Decoder/Demultiplexer Output "Low" on Select

CD4556B (File No. 858)

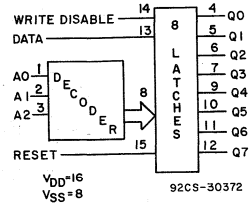
File No. = commercial data sheet

Functional Diagrams



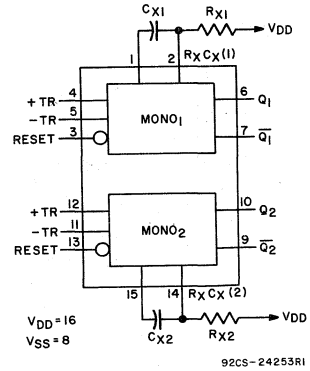
4-Bit Magnitude Comparator

CD4585B (File No. 1146)



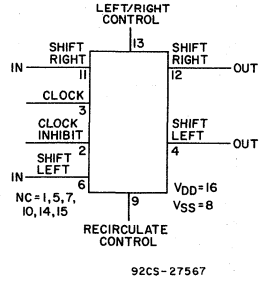
8-Bit Addressable Latch

CD4724B (File No. 1111)



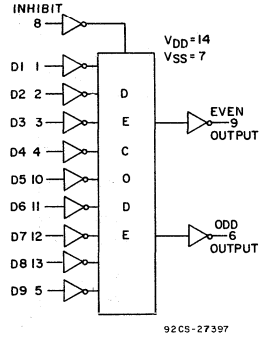
Dual Precision Monostable Multivibrator

CD14538 (File No. 2098)



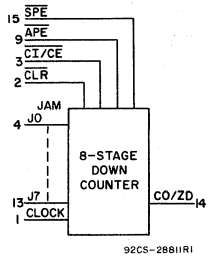
32-Stage Static Left/Right Shift Register

CD40100B (File No. 980)



9-Bit Parity Generator/Checker

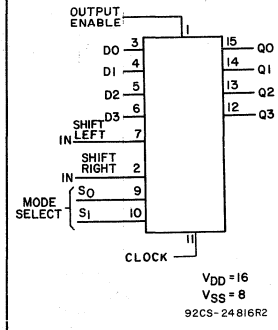
CD40101B (File No. 1000)



8-Stage Presettable Synchronous Down Counter

CD40102B (File No. 984)
2-Decade BCD

CD40103B (File No. 984)
8-Bit Binary

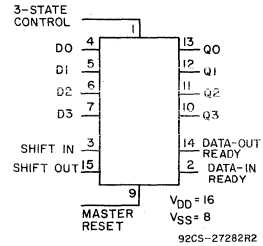


4-Bit Bidirectional Universal Shift Register

CD40104B, CD40194B
(File No. 1220)

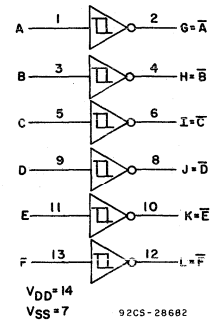
File No. = commercial data sheet

Functional Diagrams



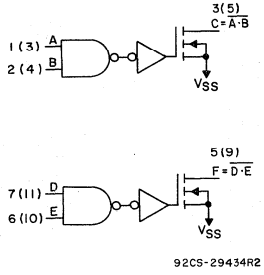
FIFO Register
4-Bits Wide by 16-Bits Long

CD40105B (File No. 1044)



Hex Schmitt Trigger

CD40106B (File No. 1017)

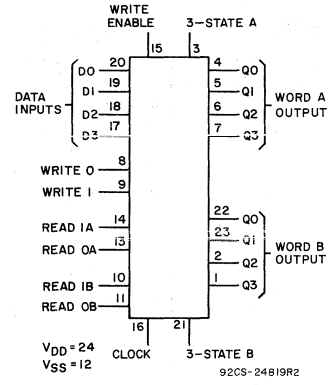


V_{SS} = 4(7)

NOTE:
NUMBERS IN PARENTHESES FOR CD40107BF, OTHERS FOR CD40107BE.

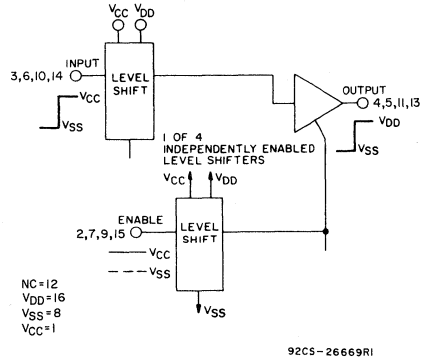
Dual 2-Input NAND Buffer/Driver

CD40107B (File No. 1015)



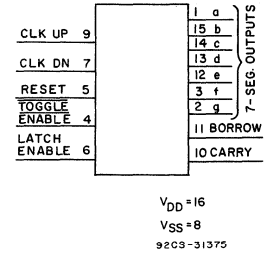
4-by-4 Multiport Register

CD40108B (File No. 1011)



Quad Low-to-High Voltage Level Shifter

CD40109B (File No. 1018)

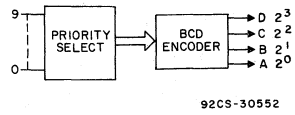


Decade Up-Down Counter/ Decoder/Latch/Driver

CD40110B (File No. 1125)

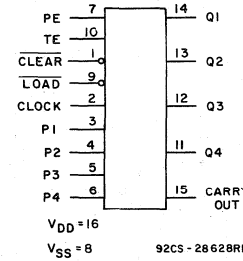
File No. = commercial data sheet

Functional Diagrams



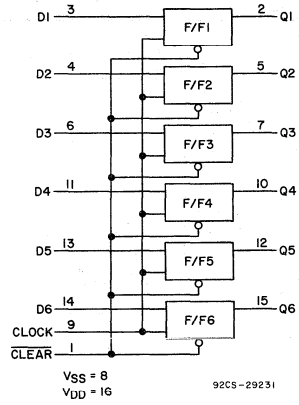
10-Line-to-4-Line BCD Priority Encoder

CD40147B (File No. 1117)



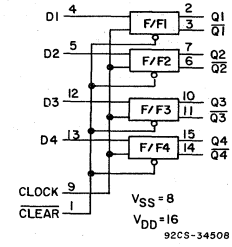
Synchronous 4-Bit Counter

CD40160B (File No. 1047)
Decade with Asynchronous Clear
CD40161B (File No. 1047)
Binary with Asynchronous Clear
CD40162B (File No. 1047)
Decade with Synchronous Clear
CD40163B (File No. 1047)
Binary with Synchronous Clear



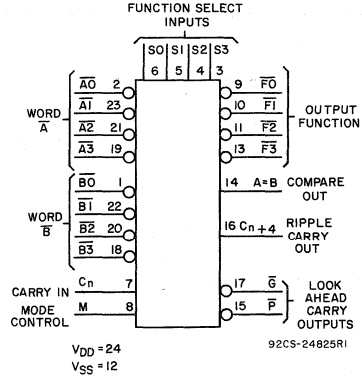
Hex "D" Type Flip-Flop

CD40174B (File No. 1031)



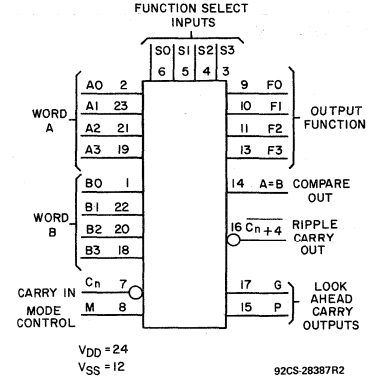
Quad 'D'-Type Flip-Flop

CD40175B (File No. 1326)



Active-Low Data

CD40181B



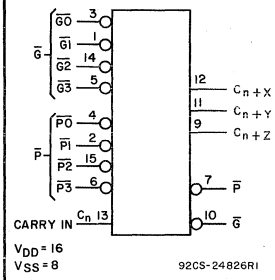
4-Bit Arithmetic Logic Unit

Active-High Data

(File No. 989)

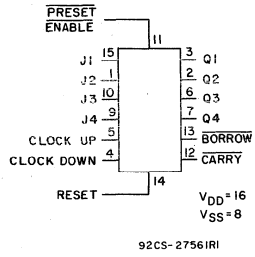
File No. = commercial data sheet

Functional Diagrams



Look-Ahead Carry Generator

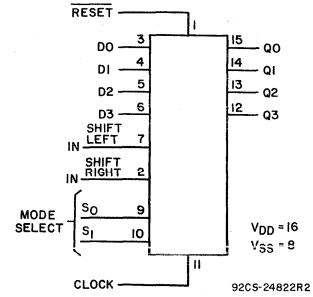
CD40182B (File No. 1008)



Presettable Up/Down Counter (Dual Clock with Reset)

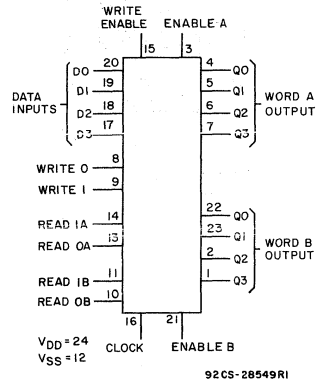
CD40192B (File No. 993) BCD

CD40193B (File No. 993) Binary



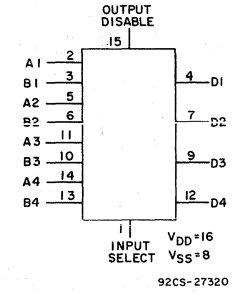
4-Bit Universal Bidirectional Shift Register with Asynchronous Master Reset

CD40194B (File No. 1220)



4-by-4 Multiport Register

CD40208B (File No. 1007)



Quad 2-Line-to-1-Line Data Selector/Multiplexer

CD40257B (File No. 982)

File No. = commercial data sheet

Static Burn-In Test Circuit Connections

For Type A devices, use V_{DD} = 12.5V. For Type B and UB devices, use V_{DD} = 18V.
NOTE: Each pin except V_{DD} and V_{SS} must have resistors of 2-47 kilohms. In most cases, V_{SS} is at pin 7 (of 14-pin IC), pin 8 (of 16-pin) or pin 12 (of 24-pin), while V_{DD} is at the highest-numbered pin; exceptions are noted by an asterisk (*).

	STATIC BURN-IN I			STATIC BURN-IN II		
TYPE	OPEN	GROUND	V_{DD}	OPEN	GROUND	V_{DD}
CD4000	1,2,6,9,10	3-5,7,8,11-13	14	1,2,6,9,10	7	3-5,8,11-14
CD4001	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9, 12-14
CD4002	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4006	2,8-13	1,3-7	14	2,8-13	7	1,3-6,14
CD4007	1,5,8,12,13	3,4,6,7,9,10	2,11,14	1,5,8,12,13	4,7,9	2,3,6,10,11,14
CD4008	10-14	1-9,15	16	10-14	8	1-7,9,15,16
CD4009*	2,4,6,10,12, 13,15	3,5,7-9,11,14	1•,16•	2,4,6,10,12,13,15	8	1•,3,5,7,9,11, 14,16•
CD4010*	2,4,6,10,12, 13,15	3,5,7-9,11,14	1•,16•	2,4,6,10,12,13,15	8	1•,3,5,7,9,11, 14,16•
CD4011	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4012	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4013	1,2,12,13	3-11	14	1,2,12,13	7	3-6,8-11,14
CD4014	2,3,12	1,4-11,13-15	16	2,3,12	8	1,4-7,9-11,13-16
CD4015	2-5,10-13	1,6-9,14,15	16	2-5,10-13	8	1,6,7,9,14-16
CD4016	2,3,9,10	1,4-8,11-13	14	2,3,9,10	7	1,4-6,8,11-14
CD4017	1-7,9-12	8,13,15	14,16	1-7,9-12	8,14	13,15,16
CD4018	4-6,11,13	1-3,7-9,10,12, 14,15	16	4-6,11,13	8	1-3,7,9,10,12 14-16
CD4019	10-13	1-9,14,15	16	10-13	8	1-7,9,14-16
CD4020	1-7,9,12-15	8,10,11	16	1-7,9,12-15	8	10,11,16
CD4021	2,3,12	1,4-11,13-15	16	2,3,12	8	1,4-7,9-11,13-16
CD4022	1-7,9-12	8,13,15	14,16	1-7,9-12	8,14	13,15, 16
CD4023	6,9,10	1-5,7,8,11-13	14	6,9,10	7	1-5,8,11-14
CD4024	3-6,8-13	1,2,7	14	3-6,8-13	7	1,2,14
CD4025	6,9,10	1-5,7,8,11-13	14	6,9,10	7	1-5,8,11-14
CD4026	4-7,9-14	1-3,8,15	16	4-7,9-14	8	1-3,15,16
CD4027	1,2,14,15	3-13	16	1,2,14,15	8	3-7,9-13,16
CD4028	1-7,9,14,15	8,10-13	16	1-7,9,14,15	8	10-13,16
CD4029	2,6,7,11,14	1,3-5,8-10,12, 13,15	16	2,6,7,11,14	8	1,3-5,9,10,12,13 15,16
CD4030	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4031	3-7,9,11-14	1,2,8,10,15	16	3-7,9,11-14	8	1,2,10,15,16
CD4033	4-7,9-13	1-3,8,14,15	16	4-7,9-13	8	1-3,14-16
CD4034	1-8	12,15-23	9-11,13,14,24	1-8	12	9-11,13-24
CD4035	1,13-15	2-12	16	1,13-15	8	2-7,9-12,16
CD4040	1-7,9,12-15	8,10,11	16	1-7,9,12-15	8	10,11,16
CD4041	1,2,4,5,8,9,11,12	3,6,7,10,13	14	1,2,4,5,8,9,11,12	7	3,6,10,13,14
CD4042	1-3,9-12,15	4-8,13,14	16	1-3,9-12,15	8	4-7,13,14,16
CD4043	1,2,9,10,13	3-8,11,12,14,15	16	1,2,9,10,13	8	3-7,11,12,14-16
CD4044	1,2,9,10,13	3-8,11,12,14,15	16	1,2,9,10,13	8	3-7,11,12,14-16
CD4046	1,2,4,6,7,10,11, 13,15	3,5,8,9,14	12,16	1,2,4,6,7,10,11, 13,15	8	3,5,9,12,14,16
CD4047	1,2,10,11,13	3-9,12	14	1,2,10,11,13	7	3-6,8,9,12,14

*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using resistor.

Static Burn-In Test Circuit Connections

TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{DD}	OPEN	GROUND	V_{DD}
CD4048	1	2-15	16	1	8	2-7,9-16
CD4049*	2,4,6,10,12, 13,15	3,5,7-9,11,14	1•,16•	2,4,6,10,12, 13,15	8	1•,3,5,7,9,11, 14,16•
CD4050*	2,4,6,10,12, 13,15	3,5,7-9,11,14	1•,16•	2,4,6,10,12, 13,15	8	1•,3,5,7,9,11, 14,16•
CD4051*	3	1,2,4-6,7•,8•, 9-15	16	3	7•,8•	1,2,4-6,9-16
CD4052*	3,13	1,2,4-6,7•,8•, 9-12,14,15	16	3,13	7•,8•	1,2,4-6,9-12, 14-16
CD4053*	4,14,15	1-3,5,6,7•,8•, 9-13	16	4,14,15	7•,8•	1-3,5,6,9-13,16
CD4060	1-7,9,10,13-15	8,11,12	16	1-7,9,10,13-15	8	11,12,16
CD4063	5-7	1,2,4,8-15	3,16	5-7	3,8	1,2,4,9-16
CD4066	2,3,9,10	1,4-8,11-13	14	2,3,9,10	7	1,4-6,8,11-14
CD4067	1	2-23	24	1	12	2-11,13-23
CD4068	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4069	2,4,6,8,10,12	1,3,5,7,9,11,13	14	2,4,6,8,10,12	7	1,3,5,9,11,13,14
CD4070	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4071	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4072	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4073	6,9,10	1-5,7,8,11-13	14	6,9,10	7	1-5,8,11-14
CD4075	6,9,10	1-5,7,8,11-13	14	6,9,10	7	1-5,8,11-14
CD4076	3-6	1,2,7-15	16	3-6	8	1,2,7,9-16
CD4077	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4078	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4081	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4082	1,6,8,13	2-5,7,9-12	14	1,6,8,13	7	2-5,9-12,14
CD4085	3,4	1,2,5-13	14	3,4	7	1,2,5,6,8-14
CD4086	3,4	1,2,5-13	14	3,4	7	1,2,5,6,8-14
CD4089	1,5-7	2-4,8-15	16	1,5-7	8	2-4,9-16
CD4093	3,4,10,11	1,2,5-9,12,13	14	3,4,10,11	7	1,2,5,6,8,9,12-14
CD4094	4-7,9-14	1-3,8,15	16	4-7,9-14	8	1-3,15,16
CD4095	1,6,8	2-5,7,9-13	14	1,6,8	7	2-5,9-14
CD4096	1,6,8	2-5,7,9-13	14	1,6,8	7	2-5,9-14
CD4097	1,17	2-16,18-23	24	1,17	12	2-11,13-24
CD4098	2,6,7,9,10,14	1,3-5,8,11-13,15	16	2,6,7,9,10,14	1,8,15	3-5,11-13,16
CD4099	1,9-15	2-8	16	1,9-15	8	2-7,16
CD4502	2,5,7,9,11,14	1,3,4,6,8,10,12, 13,15	16	2,5,7,9,11,14	8	1,3,4,6,10,12,13 15,16
CD4503	3,5,7,9,11,13	1,2,4,6,8,10,12, 14,15	16	3,5,7,9,11,13	8	1,2,4,6,10,12, 14-16
CD4504	2,4,6,10,12,15	3,5,7-9,11,14	16 (1•,13)[1]	2,4,6,10,12,15	8	16 (1•,3,5,7,9, 11,13,14)[1]
CD4508	5,7,9,11,17,19, 21,23	1-4,6,8,10, 12-16,18,20,22	24	5,7,9,11,17,19, 21,23	12	1-4,6,8,10,13-16, 18,20,22,24
CD4510	2,6,7,11,14	1,3-5,8-10,12, 13,15	16	2,6,7,11,14	8	1,3-5,9,10,12, 13,15,16
CD4511	9-15	1-8	16	9-15	8	1-7,16
CD4512	14	1-13,15	16	14	8	1-7,9-13,15,16

*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using resistor.
[1]Pin voltage is $V_{DD}/2$ for pins inside parentheses.

Static Burn-In Test Circuit Connections

TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{DD}	OPEN	GROUND	V_{DD}
CD4514	4-11,13-20	1-3,12,21-23	24	4-11,13-20	12	1-3,21-24
CD4515	4-11,13-20	1-3,12,21-23	24	4-11,13-20	12	1-3,21-24
CD4516	2,6,7,11,14	1,3-5,8-10,12, 13,15	16	2,6,7,11,14	8	1,3-5,9,10,12, 13,15,16
CD4517	1,2,5,6,10,11, 14,15	3,4,7-9,12,13	16	1,2,5,6,10,11, 14,15	8	3,4,7,9,12, 13,16
CD4518	3-6,11-14	1,2,7-10,15	16	3-6,11-14	8	1,2,7,9,10, 15,16
CD4520	3-6,11-14	1,2,7-10,15	16	3-6,11-14	8	1,2,7,9,10, 15,16
CD4527	1,5-7	2-4,8-15	16	1,5-7	8	2-4,9-16
CD4532	6,7,9,14,15	1-5,8,10-13	16	6,7,9,14,15	8	1-5,10-13,16
CD4536	4,5,13	1-3,6-12,14,15	16	4,5,13	8	1-3,6,7,9-12, 14-16
CD4555	4-7,9-12	1-3,8,13-15	16	4-7,9-12	8	1-3,13-16
CD4556	4-7,9-12	1-3,8,13-15	16	4-7,9-12	8	1-3,13-16
CD4585	3,12,13	1,2,4-11,14,15	16	3,12,13	8	1,2,4-7,9-11, 14-16
CD4724	4-7,9-12	1-3,8,13-15	16	4-7,9-12	8	1,3,13-16
CD14538	2,6,7,9,10,14	1,3-5,8,11-13,15	16	2,6,7,9,10,14	1,8,15	3-5,11-13,16
CD40100	1,4,5,7,10,12,14 15	2,3,6,8,9,11,13	16	1,4,5,7,10,12, 14,15	8	2,3,6,9,11, 13,16
CD40101	6,9	1-5,7,8,10-13	14	6,9	7	1-5,8,10-14
CD40102	14	1-13,15	16	14	8	1-7,9-13,15,16
CD40103	14	1-13,15	16	14	8	1-7,9-13,15,16
CD40104	12-15	1-11	16	12-15	8	1-7,9-11,16
CD40105	2,10-14	1,3-9,15	16	2,10-14	8	1,3-7,9,15,16
CD40106	2,4,6,8,10,12	1,3,5,7,9,11,13	14	2,4,6,8,10,12	7	1,3,5,9,11, 13,14
CD40107	1,2,5,6,8,9, 12,13	3,4,7,10,11	14	1,2,5,6,8,9,12,13	7	3,4,10,11,14
CD40108	1,2,4-7,22,23	3,8-21	24	1,2,4-7,22,23	12	3,8-11,13-21, 24
CD40109*	4,5,11-13	2,3,6-10,14,15	1•,16	4,5,11-13	8	(1•,2,3,6,7,9,10, 14,15)[1]16
CD40110	1-3,10-15	4-9	16	1-3,10-15	8	4-7,9,16
CD40147	6,7,9,14	1-5,8,10-13,15	16	6,7,9,14	8	1-5,10-13,15,16
CD40160	11-15	1-10	16	11-15	8	1-7,9,10,16
CD40161	11-15	1-10	16	11-15	8	1-7,9,10,16
CD40162	11-15	1-10	16	11-15	8	1-7,9,10,16
CD40163	11-15	1-10	16	11-15	8	1-7,9,10,16
CD40174	2,5,7,10,12,15	1,3,4,6,8,9,11, 13,14	16	2,5,7,10,12,15	8	1,3,4,6,9,11,13, 14,16

*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using resistor.
[1]Pin voltage is $V_{DD}/2$ for pins inside parentheses.
[2]V_{DD} = 11.5 volts; V_{CC} = 6.5 volts; use 300 Ω resistors at pins 10,13-21.

Static Burn-In Test Circuit Connections

TYPE	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{DD}	OPEN	GROUND	V_{DD}
CD40175	2,3,6,7,10,11, 14,15	1,4,5,8,9,12,13	16	2,3,6,7,10,11, 14,15	8	1,4,5,9,12,13,16
CD40181	9-11,13-17	1-8,12,18-23	24	9-11,13-17	12	1-8,18-24
CD40182	7,9-12	1-6,8,13-15	16	7,9-12	8	1-6,13-16
CD40192	2,3,6,7,12,13	1,4,5,8-11,14,15	16	2,3,6,7,12,13	8	1,4,5,9-11, 14-16
CD40193	2,3,6,7,12,13	1,4,5,8-11,14,15	16	2,3,6,7,12,13	8	1,4,5,9-11, 14-16
CD40194	12-15	1-11	16	12-15	8	1-7,9-11,16
CD40208	1,2,4-7,22,23	3,8-21	24	1,2,4-7,22,23	12	3,8-11,13-21, 24
CD40257	4,7,9,12	1-3,5,6,8,10,11, 13-15	16	4,7,9,12	8,15	1-3,5,6,10,11, 13,14,16

Dynamic Burn-In Test Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{DD}	V_{DD}	OSCILLATOR	
					50 kHz	25 kHz
CD4000	1,2	7	6,9,10	14	3-5,8,11-13	—
CD4001	—	7	3,4,10,11	14	1,2,5,6,8,9,12,13	—
CD4002	6,8	7	1,13	14	2-5,9-12	—
CD4006	2	7	8-13	14	3	1,4-6
CD4007	—	4,7,9	1,5,8,12,13	2,11,14	3,6,10	—
CD4008	—	8	10-14	16	2,4,6,15	1,3,5,7,9
CD4009*	13	8	2,4,6,10,12,15	1•,16•	3,5,7,9,11,14	—
CD4010*	13	8	2,4,6,10,12,15	1•,16•	3,5,7,9,11,14	—
CD4011	—	7	3,4,10,11	14	1,2,5,6,8,9,12,13	—
CD4012	6,8	7	1,13	14	2-5,9-12	—
CD4013	—	4,6-8,10	1,2,12,13	14	3,11	5,9
CD4014	—	1,4-9,13-15	2,3,12	16	10	11
CD4015	—	6,8,14	2-5,10-13	16	1,9	7,15
CD4016	—	7	2,3,9,10	14	5,6,12,13	1,4,8,11
CD4017	—	8,13,15	1-7,9-12	16	14	—
CD4018	—	2,8,9,15	4-6,11,13	1,3,12,16	7,14	10
CD4019	—	8	10-13	16	—	1-7,9,14,15
CD4020	—	8,11	1-7,9,12-15	16	10	—
CD4021	—	1,4-9,13-15	2,3,12	16	10	11
CD4022	—	8,13,15	1-7,9-12	16	14	—
CD4023	—	7	6,9,10	14	1-5,8,11-13	—
CD4024	8,10,13	2,7	3-6,9,11,12	14	1	—
CD4025	—	7	6,9,10	14	1-5,8,11-13	—
CD4026	—	2,8,15	4-7,9-14	3,16	1	—
CD4027	—	4,7-9,12	1,2,14,15	5,6,10,11,16	3,13	—
CD4028	—	8	1-7,9,14,15	16	10,12,13	11
CD4029	—	1,3-5,8,12,13	2,6,7,11,14	9,10,16	15	—
CD4030	—	7	3,4,10,11	14	2,6,9,13	1,5,8,12
CD4031	3-5,11-14	8,15	6,7,9	1,16	2	10

*Non-standard pin arrangment, or multiple supply pins; connect pins marked (•) without using a resistor.

Dynamic Burn-In Test Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{DD}	V_{DD}	OSCILLATOR	
					50 kHz	25 kHz
CD4033	—	2,3,8,14,15	4-7,9-13	16	1	—
CD4034	—	1-8,11-14	16-23	9,24	15	10
CD4035	1,3,4	2,5,7-12	13-15	16	6	—
CD4040	—	8,11	1-7,9,12-15	16	10	—
CD4041	—	7	1,2,4,5,8,9,11,12	14	3,6,10,13	—
CD4042	—	8	1-3,9-12,15	6,16	5	4,7,13,14
CD4043	13	8	1,2,9,12	5,16	4,6,12,14	3,7,11,15
CD4044	2	8	1,9,10,13	5,16	4,6,12,14	3,7,11,15
CD4046	1,4,6,7,10,11, 13,15	8,9	2	3,5,12,16	14	—
CD4047	—	7,9,12	1,2,10,11,13	4,5,14	6,8	3
CD4048	—	8,15	1	2,16	9-14	3-7
CD4049*	13	8	2,4,6,10,12,15	1•,16	3,5,7,9,11,14	—
CD4050*	13	8	2,4,6,10,12,15	1•,16	3,5,7,9,11,14	—
CD4051*	—	4-6,7•,8•,9, 12,14	3	1,2,13,15,16	11	10
CD4052*	—	4-6,7•,8•,12,15	3,13	1,2,11,14,16	10	9
CD4053*	—	1,5,6,7•,8•,12	4,14,15	2,3,13,16	9-11	—
CD4054	—	7•,8	3-6	1,10,12,14	2	9,11,13,15
CD4055	—	7•,8	1,9-15	16	6	2-5
CD4056	—	7•,8	9-15	1,16	6	2-5
CD4060	—	8,12	1-7,9,10,13-15	16	11	—
CD4063	—	1,2,4,8,10,11,13	5-7	3,16	12,15	9,14
CD4066	—	7	2,3,9,10	14	5,6,12,13	1,4,8,11
CD4067	—	12,15	1	24	2-9,16-23	(10,11,13,14)[1]
CD4068	6,8	7	1,13	14	2-5,9-12	—
CD4069	—	7	2,4,6,8,10,12	14	1,3,5,9,11,13	—
CD4070	—	7	3,4,10,11	14	1,5,8,12	2,6,9,13
CD4071	—	7	3,4,10,11	14	1,2,5,6,8,9,12,13	—
CD4072	6,8	7	1,13	14	2-5,9-12	—
CD4073	—	7	6,9,10	14	—	1-5,8,11-13
CD4075	—	7	6,9,10	14	—	1-5,8,11-13
CD4076	—	1,2,8-10,15	3-6	16	7	11-14
CD4077	—	7	3,4,10,11	14	1,5,8,12	2,6,9,13
CD4078	6,8	7	1,13	14	2-5,9-12	—
CD4081	—	7	3,4,10,11	14	1,2,5,6,8,9,12,13	—
CD4082	6,8	7	1,13	14	2-5,9-12	—
CD4085	—	7	3,4	14	1,2,5,6,8,9,12,13	10,11
CD4086	4	7	3	14	1,2,5,6,8,9,11-13	10
CD4089	—	2,4,8,10,12-15	1,5-7	3,16	9	11
CD4093	—	7	3,4,10,11	14	1,2,5,6,8,9,12,13	—
CD4094	—	8	4-7,9-14	1,15,16	3	2
CD4095	1	2,7,13	6,8	3-5,9-11,14	—	12
CD4096	1	2,5,7,9,13	6,8	3,4,10,11,14	12	—
CD4097	—	12,13	1,17	24	2-9,15,16,18-23	(10,11,14)[2]
CD4098	—	1,4,8,12,15	6,7,9,10	2,14,16	5,11	3,13

*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using a resistor.

[1]Pin 10 is @ 14 kHz; pin 11 is @ 7 kHz; pin 13 is @ 1.7 kHz; pin 14 is @ 3.5 kHz.

[2]Pin 10 is @ 14 kHz; pin 11 is @ 7 kHz; pin 14 is @ 3.5 kHz.

Dynamic Burn-In Test Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{DD}	V_{DD}	OSCILLATOR	
					50 kHz	25 kHz
CD4099	—	5-8	1,9-15	16	2,4	3
CD4502	—	8	2,5,7,9,11,14	16	4	1,3,6,10,12,13,15
CD4503	—	1,8,15	3,5,7,9,11,13	16	2,4,6,10,12,14	—
CD4504	—	8	1•,2,4,6,10,12,15	16	(3,5,7,9,11,14)[3]	13[3]
CD4508	—	1,3,12,13,15	5,7,9,11,17,19, 21,23	2,14,24	4,6,8,10,16,18, 20,22	—
CD4510	—	1,3,4,8,9,12,13	2,6,7,11,14	10,16	15	5
CD4511	9-15	5,8	—	3,4,16	1,2,7	6
CD4512	—	8,10,15	14	16	1-7,9,11,12	13
CD4514	—	2,3,12	4-11,13-20	21,22,24	1	23
CD4515	—	2,3,12	4-11,13-20	21,22,24	1	23
CD4516	—	1,3,4,8,9,12,13	2,6,7,11,14	10,16	15	5
CD4517	—	3,8,13	1,2,5,6,10,11 14,15	16	4,12	7,9
CD4518	—	7,8,15	3-6,11-14	2,10,16	1,9	—
CD4520	—	7,8,15	3-6,11-14	2,10,16	1,9	—
CD4527	—	2,4,8,10,12-15	1,5-7	3,16	9	11
CD4532	—	8	6,7,9,14,15	5,16	1-4,10-13	—
CD4536	—	1,2,6-8,14,15	4,5,13	9-12,16	3	—
CD4541	4,11	5-7	1,2,8	9,10,12-14	3	—
CD4543	—	6-8	9-15	1,4,16	2,3,5	—
CD4555	—	1,8,15	4-7,9-12	16	2,14	3,13
CD4556	—	1,8,15	4-7,9-12	16	2,14	3,13
CD4585	—	5-9,11,14,15	3,12,13	1,4,16	2	10
CD4724	—	1-3,8	4-7,9-12	16	14,15	13
CD14538	—	1,4,8,12,15	6,7,9,10	2,14,16	5,11	3,13
CD22100	—	8	10,11,14,15	7,16	1,3,9,12,13	(2,4-6)[4]
CD22101	—	12	4,5,8,9,16, 17,20,21	24	3,6,7,10,15 18,19,22	(1,2,11,14,23)[5]
CD40100	1,5,7,10,14,15	2,8,13	4,12	9,16	3	6,11
CD40101	—	4,7	6,9	12,14	2,3,5,8,10	1,11,13
CD40102	—	3,8,15	14	2,16	1,4,6,11,13	5,7,9,10,12
CD40103	—	3,8,15	14	2,16	1,4,6,11,13	5,7,9,10,12
CD40104	—	7,8,10	12-15	1,3-6,9,16	11	2
CD40105	—	1,8,9	2,10-14	16	3,15	4-7
CD40106	—	7	2,4,6,8,10,12	14	1,3,5,9,11,13	—
CD40107	1,2,6,8,12,13	7	5,9	14	—	3,4,10,11
CD40108	—	12	1,2,4-7,22,23	3,15,16,21,24	8,11,14,19,20	9,10,13,17,18
CD40109*	12	8	1•,4,5,11,13	16	(3,6,10,14)[5]	(2,7,9,15)[3]
CD40110	—	4-8	1-3,10-15	16	9	—
CD40116*	—	—	—	—	—	—
CD40117	—	7	3-6,8-11	14	12,13	1,2
CD40147	—	8	6,7,9,14	16	1,3,11,13	2,4,5,10,12,15
CD40160	—	8	11-15	1,7,9,10,16	2-6	—
CD40161	—	8	11-15	1,7,9,10,16	2-6	—
CD40162	—	8	11-15	1,7,9,10,16	2-6	—
CD40163	—	8	11-15	1,7,9,10,16	2-6	—
CD40174	—	8	2,5,7,10,12,15	1,16	9	3,4,6,11,13,14

[3]Pin Voltage is $V_{DD}/2$.
[4]Pin 5 is @ 14 kHz; Pin 6 is @ 7 kHz; Pin 2 is @ 3.5 kHz.
[5]Pin 2 is @ 14 kHz; Pin 1 is @ 7 kHz; Pins 14, 23 are @ 3.5 kHz.
*Non-standard pin arrangement, or multiple supply pins; connect pins marked (•) without using a resistor.

Dynamic Burn-In Test Circuit Connections

TYPE	OPEN	GROUND	1/2 V_{DD}	V_{DD}	OSCILLATOR	
					50 kHz	25 kHz
CD40175	—	8	2,3,6,7,10,11 14,15	1,16	9	4,5,12,13
CD40181	—	4-6,8,12	9-11,13-17	3,24	1,2,18-23	7
CD40182	—	8	7,9-12	16	1-6,14,15	13
CD40192	—	8,14	2,3,6,7,12,13	1,5,9-11,15,16	4	—
CD40193	—	8,14	2,3,6,7,12,13	1,5,9-11,15,16	4	—
CD40194	—	7,8,10	12-15	1,3-6,9,16	11	2
CD40208	—	12	1,2,4-7,22,23	3,15,16,21,24	8,10,14,19,20	9,11,13,17,18
CD40257	—	8,15	4,7,9,12	16	2,3,5,6,10,11, 13,14	1

Guide to Burn-In Delta Limits for Level /MS CD4000B-Series CMOS ICs

Delta Parameters

For the /MS level devices, certain parameters are data-logged and deltas are calculated from pre to post burn-in. These parameters are shown below.

Critical Parameters	Symbols	Test Conditions V_O (V)	Test Conditions V_{IN} (V)	Test Conditions V_{DD} (V)	Delta (Δ) Limits
Quiescent Device Current					
Gates	I_{DD}	—	0,20	20	± 0.1 μA
MSI-1 Types	I_{DD}	—	0,20	20	± 0.2 μA
MSI-2 Types	I_{DD}	—	0,20	20	± 1.0 μA
Output Low (Sink) Current	I_{OL}	0.4	0,5	5	± 20% of initial value
Output High (Source) Current	I_{OH}	4.6	0,5	5	± 20% of initial value
Types with R_{ON} limits instead of I_{OL} and I_{OH}	R_{ON}	—	—	10V	± 20% of initial value

Leadless Chip Carrier Pinouts

The following table and diagrams show JEDEC standard pinout conversions from 14, 16, 22 and 24 pin leaded FP/DIL packages to 20 and 28 terminal leadless chip carriers. Harris CD4000B-series products offered in leadless chip carriers are shown below.

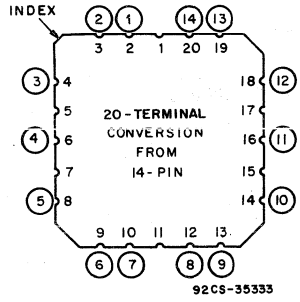
Pinout Conversion From Leaded Package to Leadless-Chip Carrier

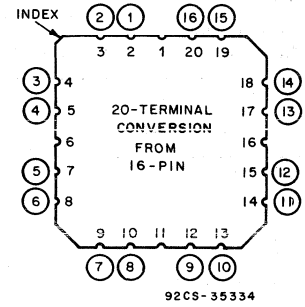
FP/DIL Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Leadless	2	3	4	6	8	9	10	12	13	14	16	18	19	20										
Chip	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20								
Carrier	2	3	4	5	6	8	10	11	12	13	14	16	17	18	19	20	22	24	25	26	27	28		
Terminal	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28

CD4000B-Series Conversion Diagrams

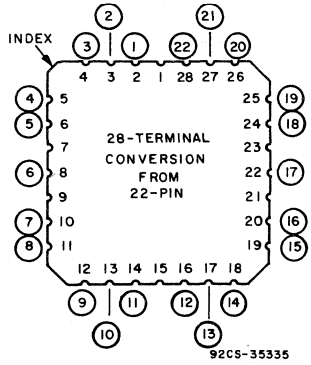
Top Views Shown

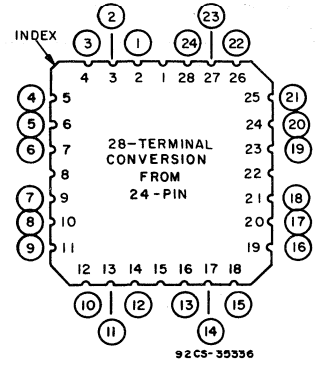
20-Terminal Leadless-Chip Carriers





28-Terminal Leadless-Chip Carriers





RAD-HARD 13

ARTICLE REPRINTS

Radiation Effects and Hardening Techniques for CMOS

Daniel B. Clifton, Brent R. Doyle

Defense systems are now being built to withstand both tactical and strategic nuclear environments. In the commercial sector, radiation hardness specifications are being set to reduce the inherent risk involved in sending a large investment into a harsh and remote environment. The advent of nuclear power has also created a need for radiation-qualified monitor and control systems. There are several system level radiation hardening techniques: current limiting resistors, overvoltage protection diodes, shielding, circumvention, etc. However, the weakest link in a system will usually turn out to be one of its many electronic components. As the scale of integration approaches several hundred thousand gates to a chip, the hardness of integrated circuits is becoming even more critical. Except for the costly practice of shielding, the only way to guarantee IC survivability in a radiation environment is to use radiation hardened ICs. Thus, the task of meeting a system's radiation requirement often begins with the semiconductor manufacturer.

The development of a radiation hardened integrated circuit is a difficult task. A thorough understanding of the technology is required, in addition to an understanding of radiation effects of the technology. Only with this combined knowledge can effective hardening techniques be developed.

Radiation Types

Radiation can be divided into four categories according to its effects on integrated circuits. Total dose ionizing radiation relates to the charging or ionization of the dielectric oxides of integrated circuits. This ionization affects silicon surface carrier concentrations and thus causes Metal Oxide Semiconductor (MOS) device thresholds to shift. Total dose accumulation occcurs at all dose rates, although at higher transient dose rates, other effects began to occur as well.

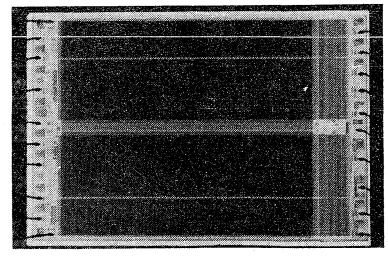
These effects constitute the second category, ionizing dose rate radiation. This type of radiation induces photocurrents across P-N junctions which cause data upset and latch-up. At the highest dose rates (prompt ionizing), these photocurrents can be so large that they effectively short out the supplies and present the danger of immediate circuit burn-out. Ionizing radiation includes gamma rays, charged particles (i.e., electrons and protons), and X-rays.

The third type of radiation, neutron fluence, lacks an electrical charge and thus does not cause ionization or photocurrents. Its primary effect is to cause disruptions in the silicon lattice through collisions with silicon atoms. This degrades the mobility of minority charge carriers and thus reduces the gain of bipolar transistors. However, neutrons have very little effect on Complementary Metal Oxide Semiconductor (CMOS) devices since CMOS is a majority carrier technology.

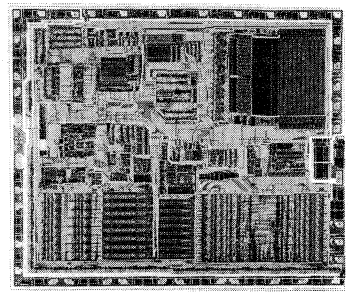
The last type, cosmic rays, is responsible for a phenomenon known as Single Event Upset (SEU). SEU is a type of soft data upset which is caused by the deposition of charge within a critical node by a single, high energy ion.

Ionizing Radiation Dose Rate

The most serious effect of prompt dose rate ionizing radiation on CMOS devices is the phenomenon of latch-up. Latch-up occurs when the radiation-induced photocurrents crossing the junction between the substrate and the P well (Ipp1) alter the voltage potential between the local substrate and the P+ source, as well as between the local P well and the N+ source. This is schematically shown in figure 1. These photocurrents, flowing laterally through Rs and Rw, forward bias the source-body junction of both the P channel and the N channel transistors (which are the base-emitter junctions of the parasitic PNP and the NPN devices). As the dose rate increases, the photocurrents increase until the potential across Rs or Rw is great enough to turn on either the PNP or the NPN, thus triggering the parasitic SCR structure illustrated. Once triggered on, this structure will continue to draw excessive current, even after the high dose rate gamma pulse is over, until either the IC burns out or power is shut off.



Radiation hardened 16k x 1 static RAM.



Radiation hardened 16-bit microprocessor.

At transient gamma dose rate levels (lower than prompt or peak gamma), latch-up may not occur, but data upset is possible. Referring to figure 1, the two photocurrents (Ipp2 and Ipp3) flowing into the P+ drain and out of the N+ drain can cause the output voltage of a CMOS inverter to briefly increase or decrease to an undefined logic level. (The net effect of Ipp2 and Ipp3 is determined by their difference in magnitude and depends on the logic state of the inverter, the drain areas involved and the doping levels used). If this output voltage reaches the switch point voltage of a clock input or feedback network of a bi-stable circuit, the circuit will change state.

Another cause of data upset is rail span collapse. Rail span collapse is characterized by a voltage drop on the power bus as a result of the combined photocurrents of the entire chip. Thus, rail span collapse is more serious in heavily integrated devices. Data upset from rail span collapse is the dominant form of upset at short pulse widths.

There are several methods to harden a CMOS IC against prompt radiation induced latch-up. One method is the use of an epitaxial substrate (and/or a heavily doped buried layer beneath the P or N well). This reduces the resistance of the substrate (and/or the P well), reducing the resistance of two shunt resistors, Rs and Rw (Figure 1). With reduced shunt resistance, the collector current of the PNP must be high to develop a Vbe across Rw, and the collector current of the NPN must be high to develop a Vbe across Rs. With low enough values of Rw and Rs, the transistor's operating currents are forced into the high level injection region where beta is greatly reduced. Thus, when the prompt event is over and the photocurrents vanish, the latch-up condition cannot be sustained due to the loop gain being less than one.

Other methods to prevent latch-up include reducing the beta product of the two parasitic bipolar transistors by gold doping, neutron irradiation or greater device separation. By disrupting the silicon lattice and thereby providing additional recombination centers, neutron fluence reduces the minority carrier lifetime. This results in lower betas for both of the parasitic bipolar transistors. Gold atoms also serve as recombination centers. Device separation increases the base width of the parasitic PNP transistor (or the NPN transistor if N well technology is used). This also results in a lower beta.

To prevent data upset from transient dose rates, the magnitude of the photocurrents must be reduced. This is most effectively achieved by reducing the generation volume around P-N junctions. One process that does this is the thin Silicon-On-Insulator (SOI) process (Figure 2). This process isolates each transistor in a tub formed by the buried insulator and the lateral insulators. The net reduction in generation volume is significant, resulting in an order of magnitude increase in transient upset hardness. The isolation of each transistor also eliminates all four-layer SCR structures, thereby preventing latch-up.

Hardening techniques to prevent rail span collapse are not as complex as other dose rate hardening techniques. Primarily, power and ground busses must be widened to handle the large photocurrents generated during a transient event. Increasing metal thickness also serves the same purpose. Additionally, the use of poly interconnects on the power busses must be eliminated.

Total Ionizing Radiation Dose

In addition to the dose rate effects of ionizing radiation, there are cumulative total dose effects as well. The predominant one is a positive ionization of the gate and field oxides. This is due to the fact that electrons have a much higher mobility than holes and are swept out of the oxides as the IC is irradiated, leaving the less mobile holes behind. Another effect of cumulative total dose radiation is the formation of interface states, i.e., ions trapped at the silicon-oxide interface.

Ionization of the MOS gate oxide causes shifts in threshold voltage. For both P and N channel transistors, this shift is initially in a negative direction. This effect tends to be more serious for the N channel transistor than the P channel transistor due to the fact that the threshold of the N channel transistor may drop below the minimum gate bias voltage. If this occurs, the transistor is left in an ON state (depletion

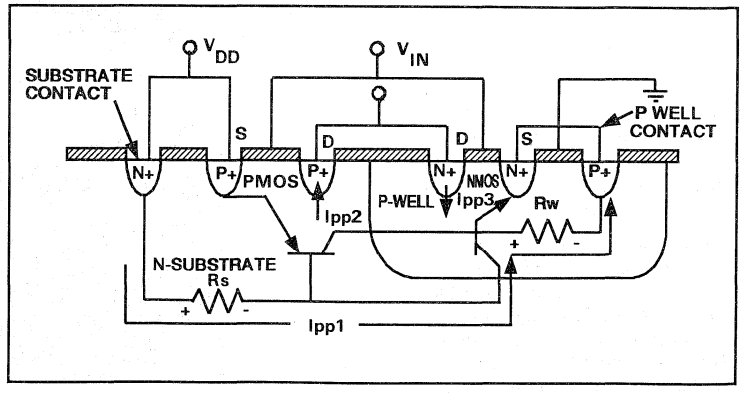


Fig. 1 Photocurrents generated by prompt gamma radiation in a CMOS inverter.

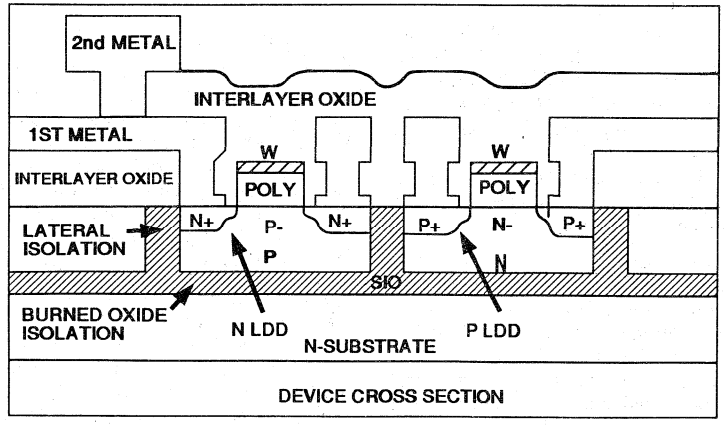


Fig. 2 Thin silicon-on-insulator process.

node) for all signal levels available on chip. This condition causes excessive leakage and usually leads to catastrophic device failure.

On the other hand, the ionization of field oxides produces an inversion layer across the surface of all P well (or the substrate in the case of N well technology). This radiation-induced inversion layer shorts the P channel body tie (Vdd supply contact) to the N channel source (ground). The net result is high static leakages.

Due to their negative polarity, interface states tend to offset the effect of positive gate oxide ionization in N channel transistors. Additionally, interface states anneal much more slowly than oxide ionization, resulting in an eventual rebound of N channel threshold voltage. For very slow dose rates, oxide ionization anneals as quickly as it is induced; thus, interface state formation dominates and N channel threshold voltage increases.

Interface states also cause a degradation in conduction factor (K') in both N channel and P channel transistors. By providing additional carrier scattering, interface states reduce carrier mobility and thus reduce the effective conduction factor of a MOS device. Since interface states anneal very slowly, degradation of conduction factor is a semi-permanent effect.

We believe the most effective way to harden a CMOS device against P silicon surface inversion is the Harris hardened field oxide formation process. This process produces an oxide that resists ionization and/or allows the swift dissipation of trapped charges. As a result, no inversion of the P well is seen. An older hardening method which also prevents surface inversion is the use of heavily doped guard rings around the perimeter of the P well. The high doping level requires a higher level of oxide ionization to invert.

Gate oxide hardening is also accomplished using a hardened process. In addition, a thinner MOS gate oxide reduces the total trapped charge volume under the gate. Unfortunately, there is as yet no effective hardening technique to reduce the formation of interface states.

Cosmic Rays: Ions, Alpha Particles

Heavy ions and alpha particles can cause SEU in a bulk CMOS IC whenever they pass through a critical node of a RAM cell or latch, or a critical pipeline to one of these devices. As the particle sweeps through the node, it creates a densely ionized track as it deposits its energy. The resistance of the track is much lower than the surrounding silicon, so the charge built up along the track is quickly (1 ns) funneled back to the node where it can induce a change of state (Figure 3). If this charge funnels into a P (or N) well of a CMOS device, it can also cause latch-up in much the same way as prompt gamma radiation.

A measure of an ion's Linear Charge Deposition (LCD) rate is its Linear Energy Transfer (LET). Most ions encountered in space have an LET of 40 Mev/gm/cm^2 or less. The minimum LET required to cause an upset in an IC, the LET threshold, is a measure of an IC's hardness to SEU. The total charge that is transferred to a node is determined by the linear charge deposition rate times the charge collection length (believed to be longer than the diffusion length due to funneling). As would be expected, the greater the particle's LET (or the higher its LCD rate) and the more oblique its angle of intersection (with the consequent increase in the length of intersection with the die), the higher is its total deposited charge.

Another measure of an IC's hardness to SEU is its device upset cross sectional area. This value is determined by dividing the total number of upsets witnessed during a test by the total particle fluence directed at the device during the test. Several different cross sectional areas are determined for a range of LET values to provide a complete characterization of the device. The expected upset frequency can then be determined by integrating the expected flux times the device upset cross sectional area over all ranges of LET.

The SEU hardness of a bulk CMOS device can be increased by introducing poly resistors in the feedback paths of bi-stable circuit elements (Figure 4). Although this increases write access time by about 20% at low temperatures, it also significantly increases an IC's LET threshold. The device

upset cross sectional area is increased as well. In some cases, this threshold can be raised so high that the device becomes effectively SEU-immune. The only other effective means to improve SEU hardness in bulk CMOS ICs is to increase feature size. This increases node capacitance and requires a consequently higher energy ion to cause an upset. However, the trend is for increased integration in IC technologies (smaller features); thus SEU hardness has become an important consideration in space applications.

To provide SEU hardness as device sizes decrease, the device upset cross sectional area must be reduced. This can best be achieved with a thin SOI process (Figure 2). The lateral trench isolation eliminates the diffusion junction on three sides of the source and drain implants. By bottoming the source and drain out to the buried insulator, the total diffusion junction area of the device is reduced further. An additional benefit is provided by the buried insulator, which limits charge funneling.

Techniques that prevent latch-up in a prompt gamma environment — neutron irradiation, EPI substrates, buried layers, gold doping and device separation — will also prevent latch-up due to heavy ions.

Conclusion

Advances in hardening technology result in increases in speed, density, and hardness (Table 1). For example, Harris Semiconductor's hardened CMOS static RAM technology has advanced from 1k RAMs with a cycle time of 450 ns and a hardness of 2×10^4 RAD(Si) total dose to today's 16k RAM which has a cycle time of 90 ns and a hardness of 2×10^5 RAD(Si). In the near future, SOI technology will provide a 64k RAM with a cycle time of only 50 ns and a total dose hardness of 1×10^6 RAD(Si).

In spite of rapid advances in hardening technologies, meeting a system's hardness requirements remains a difficult task. Radiation hardened devices are still scarce and expensive due to difficult processing, low run rates, complex testing, and periodic radiation testing. In many cases, radiation hardened devices have to be custom made (or ASIC semicustom) for a particular application. This situation is changing as manufacturers develop a wider selection of radiation hardened common usage devices such as memories, microprocessors, and peripheral chips. However, radiation hardened ICs will probably remain primarily custom and ASIC semicustom devices for many years to come.

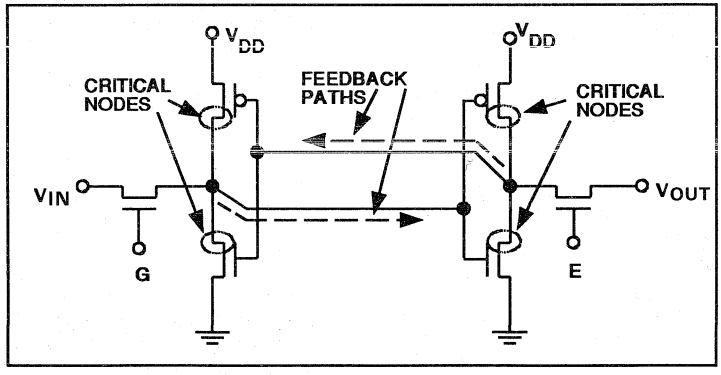


Fig. 3 Bi-stable circuit showing SEU-critical nodes.

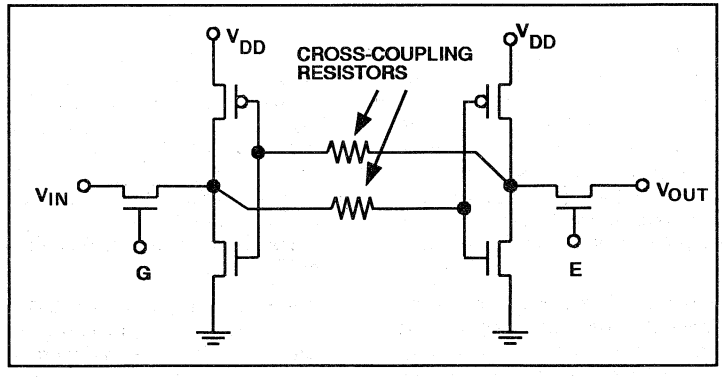


Fig. 4 Bi-stable circuit with cross-coupled resistors to prevent SEU.

TABLE 1
Hardness Levels and Speed By Technology

Technology	Total Dose Rad(Si)	Dose Rate Rad(Si)/s	RAM Cycle Time	RAM Size	LET Threshold MeV/mg/cm^2
Hardened Gate	2E4	1E8	450 ns	1k	37
Gamma Guard Ring with Hardened Gate	1E5	1E8	250 ns	4k	36
Gamma Guard Ring with Hardened Gate and Cross-Coupled Resistors	1E5	1E8	250 ns	4k	>80
Hardened Field with Hardened Gate	2E5	1E9	90 ns	16k	20
Hardened Field with Hardened Gate and Cross-Coupled Resistors	2E5	1E9	90 ns	16k	41
Hardened Field with Hardened Gate (Double Metal)	5E5	5E9	—	—	—
Silicon-On-Insulator	1E6	1E10	50 ns	64k	40

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Daniel B. Clifton *and* **Brent R. Doyle** *are senior applications engineer and director of digital product development, respectively, of Harris Semiconductor. Military and Aerospace Division*

Processing and Circuit Design Enhance A Data Converter's Radiation Tolerance

Robert Heuner, Victor Zazzu, Louis Pennisi
GE Solid State, Somerville, N.J. 08876

Abstract

Rad-hard CMOS/SOS processing has been applied to a novel comparator-inverter circuit design to develop 6 and 8-bit parallel (flash) ADC (analog-to-digital converter) circuits featuring high-speed operation, low power consumption, and total-dose radiation tolerances up to 1 Mrad(Si).

Radiation Tolerant CMOS/SOS Flash ADC Circuit

An MOS integrated circuit operating in a high-level radiation environment requires a circuit design that is virtually independent of threshold voltage shift, increased leakage, and FET mobility fall-off. As a consequence of radiation, the threshold of the n-channel transistor shifts towards depletion, while the threshold of the p-channel transistor shifts toward enhancement. Radiation also increases the device leakage and lowers the mobility of the CMOS/SOS transistors by damaging the lattice structure of the epitaxial silicon. An analog signal processing element that is highly tolerant of radiation-induced threshold and mobility variations is needed. Such a circuit is described in this paper.

Fig. 1 shows the architecture of a typical CMOS/SOS flash ADC (analog/digital converter), as first described by Dingwall.[1] The 6-bit CMOS/SOS flash ADC consists of 64 comparators connected in parallel. Each of the 64 comparators simultaneously compares the unknown input signal against a plurality of equally spaced voltage-reference potentials. The voltage-reference potentials are developed from a resistor ladder formed from a linear string of polysilicon, with equidistantly spaced contacts providing an input to the CMOS/SOS comparators. The low resistance of the polysilicon ladder network makes it relatively immune to total-dose and dose-rate radiation exposure. In addition, the equidistant voltage taps on the ladder make the network dependent only on resistor ratios rather than individual value.

The comparator outputs generate a "thermometer" code. All of the comparator outputs located below the comparator connected to the reference voltage tap closest to the input voltage produce a logic 1 output; all of the comparators above the comparator connected to the reference tap closest to the input produce a logic 0 output. This thermometer code is subsequently decoded into the appropriate binary code. The binary data is then latched into the output buffers.

The most critical component of CMOS/SOS flash ADC design is the analog comparator, especially when the ADC is operated in a radiation environment. The design specification requiring that the ADC have an input dynamic range equivalent to the power supply range ($V_{DD} - V_{SS}$) rules out the use of a conventional CMOS-type operational amplifier. Under radiation effects, as described above, the operating point and dynamic range of a conventional CMOS operational amplifier (comparator) would shift such that the device would not operate according to the dynamic range specification, even with autozero techniques.

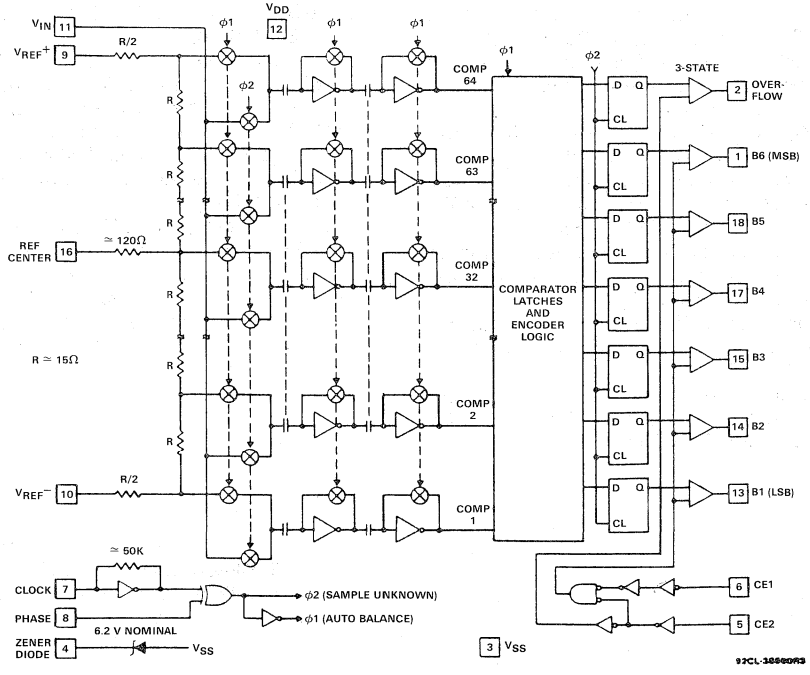

Fig. 1 Block diagram of the typical CMOS/SOS flash ADC.

To circumvent this problem, a CMOS comparator first described by McGrogan[2] is employed. This comparator is shown in Fig. 2. The McGrogan comparator consists of two sampling transmission gates ac coupled to a self-biasing "autozeroed" CMOS/SOS inverter amplifier. It is this autozero property of the CMOS inverter that makes this analog comparator ideal for operation in an environment where the MOS threshold voltages can shift dynamically.

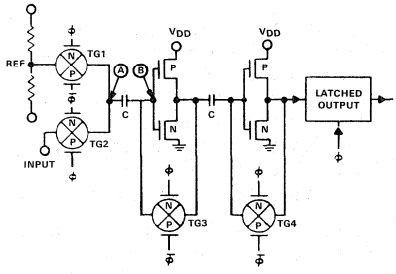

Fig. 2 The McGrogan comparator.

Fig. 3(a) shows the typical transfer curve of a CMOS/SOS inverter and its operating point. Note that the amplifier is biased at the high-gain region (i.e., the region of maximum slope). Any small voltage change in signal input will produce a large change in the output voltage. Fig. 3(b) shows the transfer curve after the device has been exposed to radiation. Note that the transfer curve has simply shifted, corroborating the previously described threshold variations. The inverter is still operating along its region of maximum small-signal gain. The autozeroing of the CMOS/SOS inverter automatically compensates for dynamic threshold variations.

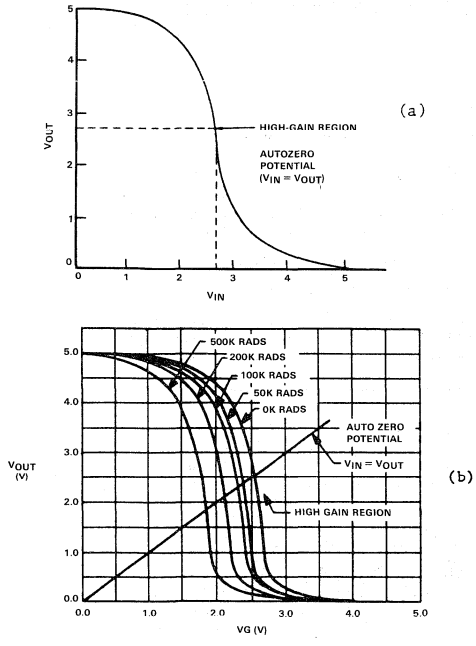

Fig. 3 (a) Typical transfer curve of a CMOS/SOS inverter, and its operating point, (b) CMOS/SOS inverter transfer curve after exposure to a variety of radiation levels.

As applied to CMOS/SOS flash ADC applications, the McGrogan comparator shown in Fig. 2 operates as follows. On the first half of the clock cycle, the reference voltage is applied to node A of the coupling capacitor via TG1, and the two autozero transmission gates, TG3 and TG4, are switched on, forcing the inverters to their autozero potential.

On the second half of the clock cycle, the autozero (TG3 and TG4) and reference (TG1) transmission gates are shut off and the input transmission gate (TG2) is switched on. The voltage at node B, V_B, shifts from its autozero potential, V_{AZ}, by the difference between the input and reference voltages as described in Eq. 1:

$$V_B = V_{AZ} - (V_{REF} - V_{IN}) \quad (1)$$

The potential at the output of inverter 1 is:

$$V_{OUT1} = A_{V1} V_B \quad (2)$$

where A_{V1} is the small-signal gain of the inverter amplifier biased at the high-gain region and given by:

$$A_{V1} = (g_{mp} + g_{mn})\ (r_{op} // r_{on}) \quad (3)$$

where g_{mp} and g_{mn} are the p and n-channel transconductances, and r_{op} and r_{on} are the p and n-channel dynamic output impedances, respectively. The CMOS/SOS inverter employed in the design of the ADC under discussion is typically operated at at frequency where the small-signal gain is 10.

Under total-dose radiation conditions, the quiescent current at a bias level of 2.5 volts ($V_{IN} = V_{OUT}$) remains constant, as shown in Fig. 7. The radiation effect on the n-channel MOSFET is such that V_{TN} shifts towards depletion and g_{mn} tends to increase. The transconductance is given by:

$$g_{mn} = \frac{2K'I_{DS}}{(V_g - V_T)} \quad (4)$$

The g_{mp} of the p-channel transistor tends to decrease. Over a limited radiation dose (i.e. up to 1 Mrad), the increasing g_{mn} and the decreasing g_{mp} tend to sum to a constant value.

Fig. 3(b) shows that the small-signal gain of a CMOS/SOS inverter is nearly constant under total-dose conditions. The maximum slope of the transfer curve represents the small-signal gain. The slope of each of the individual curves is nearly constant.

The second ac-coupled autozeroed-inverter gain stage is employed to further amplify the comparator output without having additional offset due to device mismatch of the second amplifier being reflected back into the first stage. The output data from the second stage is subsequently latched in a fully static D-type latch.

Another characteristic of the McGrogan comparator that proves very desirable for operation in radiation environments is the comparator's relative insensitivity to increased leakage. The inverter amplifiers are typically biased in a Class A configuration with approximately 50 uA of bias current. The leakage current associated with a single CMOS inverter amplifier employed in this design is well under 50 nA. Therefore any radiation-induced increase in leakage current is a small portion of overall quiescent bias current. As a consequence of the Class A bias of the inverter amplifier, the McGrogan comparator can tolerate large increases in radiation-induced leakage.

Fig. 4 shows a chip photomicrograph of the typical ADC. Note that the comparator bank has been designed in a straight-line configuration. This is an important factor. The monolithic design requires that each of the comparators track each other, and straight-line configurations do not produce extraneous boundary conditions that could lead to comparator mismatch and differential nonlinearity.

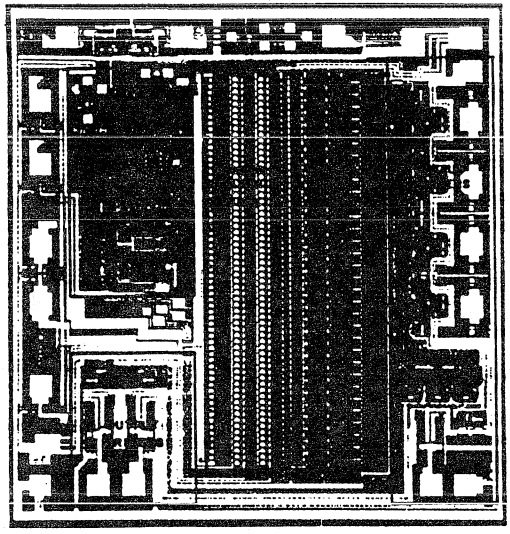

Fig. 4 Photomicrograph of the ADC circuit.

Radiation-Hard CMOS/SOS Process

Threshold shifts and leakage current increases are minimized by fabricating the flash ADC in a radiation-hardening CMOS/SOS process. Fig. 5 shows an outline of the basic process.[3] CMOS/SOS devices are made with epitaxial silicon islands on a sapphire substrate. This technique greatly reduces device capacitance and completely eliminates latch-up. A special channel-oxide process is used to achieve megarad p and n-transistor hardness levels.

The polysilicon gates of the transistors are deposited over the hardened, thin, gate oxide before the source and drain diffusions are defined. Ion implantation is then used to form the source and drain areas, with the polysilicon gates acting as a mask for the implantation. The source and drain are automatically aligned to the gate, hence the expression "self-aligned-gate" process. In this way, gate-to-source and gate-to-drain capacitances are minimized.

The CMOS/SOS sapphire substrate also isolates the n and p transistors from each other. Hence, this structure is highly resistant to transient radiation, total-dose radiation, and single event upsets. Overall, the CMOS/SOS technology offers superior radiation tolerance, high speed, low power, good noise immunity, and neutron resistance over the full military temperature range (−55°C to +125°C). Fig. 6 shows a cutaway view of the completed CMOS/SOS structure.

The flash ADC process has an added n+ capacitor implant step after channel oxidation, and requires one added mask level. This step implements the n+ plate of the capacitors used in the flash ADC circuit.

Fig. 7 shows the CMOS/SOS inverter characteristics for pre-rad, 100 krad, and 200 krad total-dose radiation. Note that very little off-transistor leakage increase occurs post radiation. Note also that post-radiation shifts are well under 0.25 volts per 100 krads for both the p and n transistors.

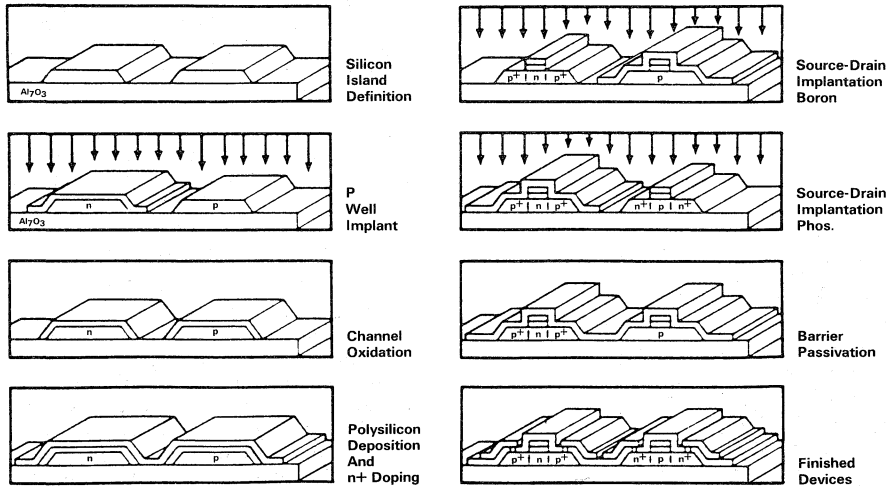

Fig. 5 Outline of the basic CMOS/SOS process.

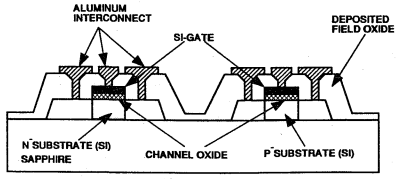

Fig. 6 Cutaway view of the completed CMOS/SOS structure.

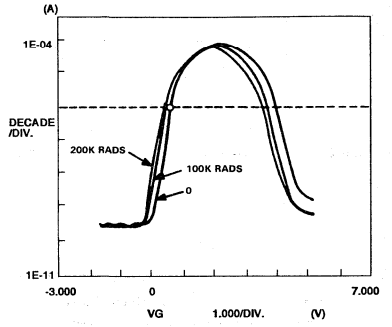

Fig. 7 CMOS/SOS inverter radiation characteristics.

Flash ADC Radiation-Test Results

When ADC circuits were fabricated, some with the standard nonrad-hard CMOS/SOS process, and some with the rad-hard CMOS/SOS process. Total-dose irradiation was performed on all devices using a Cobalt-60 gammacell. Results are graphically illustrated in Figs. 8 through 12. The data represents the average behavior of 10 samples from one 12-wafer lot of each process type, with results obtained on an automated test system. Rad testing of both standard and rad-hard process devices demonstrated the rad-hard-process devices functional to 1 Mrad compared to standard-process devices, which showed dc and functional failures at doses as low as 5 krad.

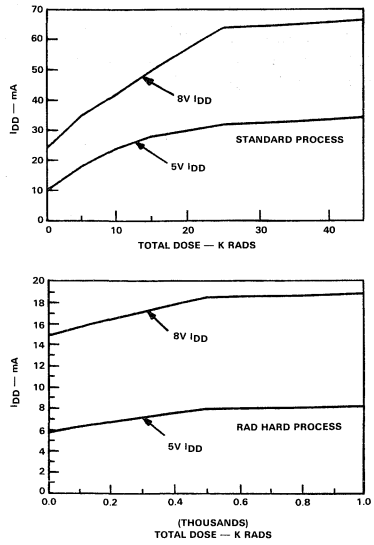

Fig. 8 I_{DD} readings at various rad levels.

Figs. 8(a) and 8(b) represent I_{DD} readings at various rad levels for both rad and non-rad types. A 45-krad, 5V I_{DD} increased from 10 mA to 32 mA while an 8V I_{DD} went from 23 mA to 68 mA in standard nonrad-hard-process devices. Rad-hard-process devices at 5V I_{DD} increased only 2.5 mA at the 1 Mrad level; there was a 4-mA increase for 8V I_{DD}. Figs. 9(a) and 9(b) show the tristate, I_{OZ}, measurements, with nonrad-hard-device values increasing to 1 mA at 45 krads, while rad-hard devices read only 1 uA at 1 Mrad.

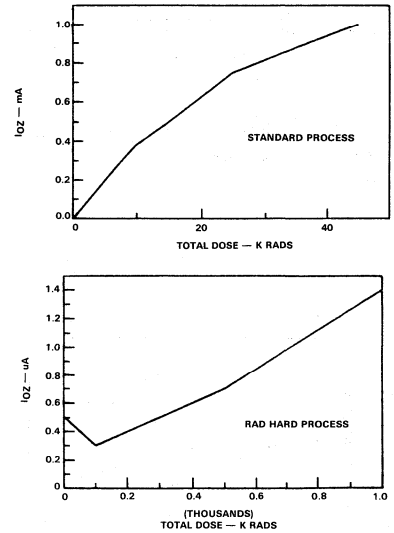

Fig. 9 I_{OZ} measurements.

Functionality was also checked on all devices tested. The nonrad-hard process units showed failures at levels as low as 5 krads; others remained functional to 45 krads. The main cause of failure is a combination of increased NMOS transistor back channel leakage and reduced NMOS transistor unit thresholds which eventually prevents proper operation of the comparator stage. The rad-hard-process units were all functional to 1 Mrad, and passed all parametric limits at +25°C.[4]

Figs. 10 through 12 illustrate other parameter shifts noted in the rad-hard process devices up to a 1-Mrad exposure. Fig. 10 demonstrates I_{sink} decreasing 1.5 mA and I_{source} decreasing 1 mA at the 1-Mrad level, with final readings well within prescribed limits. Fig. 11 plots offset and gain error expressed in LSBs throughout the Mrad range. These numbers also were within established limits of ±1 LSB. Differential and integral linearity limits of ±0.5 LSB were met by all rad-hard process devices up to 1 Mrad, as shown in Fig. 12. Significantly, as Figs. 11 and 12 show, the linearity, offset, and gain error characteristics remain within ±0.5 LSB over the 1-Mrad range. The exact LSB deviations relate to the matching of the p-to-n ratio of the comparator devices. During radiation exposure, the p-to-n ratio shifts (due to V_{TH} shifts) and the comparator gain characteristics may vary through an optimal operating point. Some increase in data delay was evident in some devices as readings approached maximum limits. Data delay measurements are used to determine maximum operating frequency of the device.

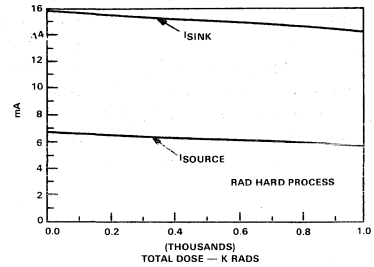

Fig. 10 I_{sink} decreasing 1.5 mA and I_{source} decreasing 1 mA at 1 Mrad level.

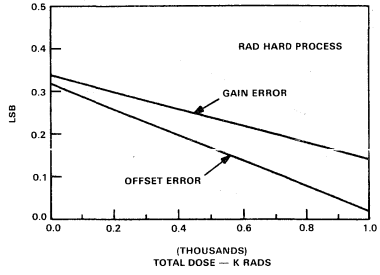

Fig. 11 Offset and gain error expressed in LSBs throughout the Mrad range.

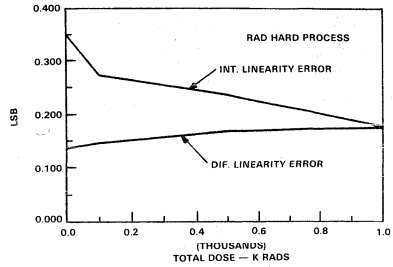

Fig. 12 Differential and integral linearity limits of ±0.5 LSB.

Conclusions

A 6-bit CMOS/SOS flash analog-to-digital converter has been developed with a tolerance to total-dose radiation up to 1 megarad. The heart of the radiation-tolerant A/D design is a novel CMOS autozero comparator. The autozero function serves to eliminate any comparator offset. The comparator design is also tolerant of voltage threshold variations associated with total-dose radiation.

References

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3. Schmitt, E.J., Chandrasekhar, H.S., Rauback, J., "Exceptional Radiation Levels from Silicon-on-Sapphire Processed High-Speed CMOS Logic," GE Solid State Application Note ICAN-8818.

4. For further details and parametric limits, see "High-Rel Series CMOS Video Speed 6-Bit Flash A/D Converter," GE Solid State Data Sheet No. 2115.

Electrical and Radiation Characterization of Three SOI Material Technologies

Wade A. Krull, James F. Buller, George V. Rouse, and Richard D. Cherne

Abstract

Many silicon-on-insulator (SOI) material technologies are currently under development. Each of these technologies possesses certain electrical or physical characteristics that affect the potential applications of the technology. This paper will describe a characterization study of three SOI material approaches in development at Harris Semiconductor: SIMOX, scaled dielectric isolation, and wafer bonding. The current status of material quality will be reviewed, typical CMOS electrical- and radiation-response characteristics will be presented, and the viability of the three technologies will be assessed.

Introduction

The applications for silicon-on-insulator (SOI) technologies are quite varied in both the commercial and military markets. With regard to the latter, the hostile environments anticipated for next-generation military systems will require significant improvements in both the speed and radiation tolerance of the associated integrated circuits. Current radiation-hardened systems employ circuits fabricated with one of three technologies: bulk silicon, dielectric isolation (DI), and silicon-on-sapphire (SOS). All of these technologies are, however, facing challenges in providing adequate immunity to radiation while increasing functional throughput. The need for higher density-hardened memory circuits for the Strategic Defense Initiative and other advanced applications has, therefore, been one of the driving forces behind the search for alternate technologies that will be able to meet the envisioned military requirements.

The limitations of the current technologies indicate the necessary characteristics of next-generation technologies. For bulk silicon circuits, the current technology is radiation-hardened CMOS on epi substrates. A limitation facing this technology is the requirement for improving immunity to transient radiation. The large substrate collection volume inherent in bulk technology constitutes an obstacle to improving this feature. The silicon-on-insulator structure provides a solution by minimizing the substrate volume and is the source of the claim that SOI is inherently rad-hard. All other parameters being equal, the transient dose immunity of a CMOS process can be improved by utilizing an SOI substrate. However, all other parameters are not equal, as will be described in this paper.

Several technologies currently exist for achieving an SOI structure. The process known as dielectric-isolation [1], [2] technology has been a production process for radiation-hardened integrated circuits for at least 10 years. Circuits are now available with both CMOS and bipolar technologies on DI. This technology provides the substrate isolation that is lacking on the bulk silicon substrate by including a thick oxide layer. However, the formation of the sidewall or lateral (or moat) isolation at the front end of the process places limitations on the achievable density possible with this technology. This aspect is improved with the scaled dielectric-isolation process flow to be described in this paper.

Finally, SOS provides the dielectric-isolation characteristic and is a currently available silicon-on-insulator technology. The problems encountered by SOS are poor material quality and the sapphire substrate material is somewhat incompatible with standard silicon processing. Several enhanced SOS processes, such as SPEAR (solid-phase epitaxy and regrowth) [3], are currently under development, which may allow SOS to evolve toward high-density circuit applications.

An ideal SOI material technology should address the areas in which current technologies are facing limitations: it should provide a thin silicon layer isolated from the substrate (improvement over bulk), possess electronic and material properties equivalent to bulk silicon (improvement over SOS), and be capable of supporting high-density integrated circuits (improvement over dielectric isolation). With such a substrate, known radiation-hardening techniques can be applied to achieve a technology with performance superior to currently available processes.

Material Fabrication Technologies

Three SOI technologies under development at Harris are: oxygen implantation (SIMOX) [4], scaled dielectric isolation, and wafer bonding. In an experiment aimed at comparing the quality of the active silicon layers associated with the three approaches, a 2-μm silicon film-thickness target was used in an effort to minimize influences associated with the back oxide. Lateral dielectric isolation was excluded for similar reasons. The goals for the experiment were to evaluate the silicon film, to determine whether scaled dielectric-isolation and wafer-bonding technologies are capable of providing a thin film, to investigate the effect of using SOI material on frontside oxide radiation hardness, and to identify discriminators that will provide selection criteria between the technologies for various applications.

SIMOX

The SIMOX process is becoming well known due to the increasing level of development efforts that have been made possible by the construction of the NV-200 oxygen implanter by Eaton Corporation. This is the first implanter that is capable of supplying large quantities of high-qualilty SIMOX wafers. The SIMOX material used in this study was implanted by the NV-200 prototype implanter at the Eaton facility in Beverly, Massachusetts. The process involves the implantation of very high doses of oxygen ions (O^+) into a silicon wafer to form a buried oxide layer. A dose of

1.8E18 cm^{-2} at an energy of 150 keV and an implantation temperature of 500°C was used. The oxygen implant is followed by an anneal to form the buried oxide layer and to reconstruct the superficial silicon layer. The anneal used in this study was 16 hours at 1250°C.

This process results in the formation of a buried silicon dioxide layer approximately 0.37 μm thick, with a silicon overlayer of 0.15 μm. The desired 2-μm silicon film is grown by vapor-phase epitaxy, using the superficial silicon layer as a seed. It should be noted that such high-dose implantation severely damages the silicon layer, making the quality of the epitaxial material strongly affected by the processes used to implant and anneal the material prior to epitaxy. Even the best SIMOX material will contain large numbers of threading dislocations [5], [6], which may have an adverse effect on the electrical quality of the epitaxial material.

Scaled Dielectric Isolation

The technology used in the current production version of dielectric isolation has been modified to yield very thin silicon layers. Normal DI material has a minimum thickness in the range of 10 μm, while a layer thickness on the order of 1μ is required for digital CMOS applications. In addition, the moat etch process of dielectric isolation has been removed, so that the material fabrication process will result in an SOI structure equivalent to other processes. Based upon Harris' extensive experience with DI material, it is believed that the moat isolation normally acts as a stress relief structure. Hence, scaled dielectric isolation, without moat isolation, is more highly stressed and may show degraded electrical characteristics as a result.

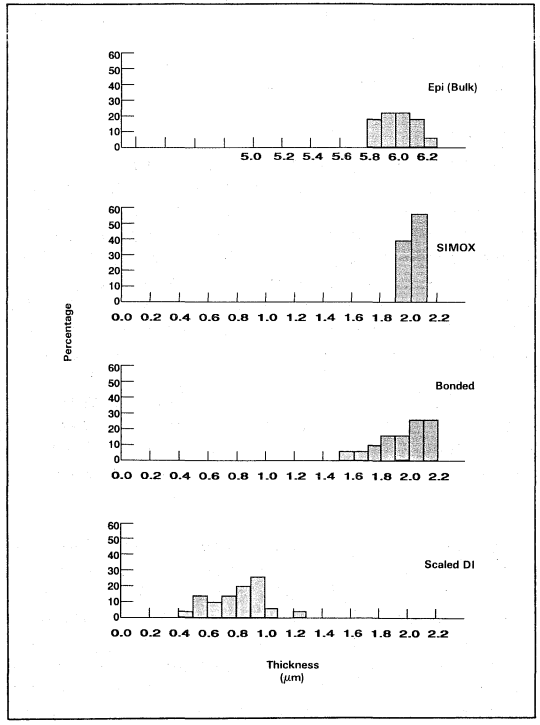

Fig. 1 Histogram of material film thickness.

The process flow begins with a heavily N+ doped silicon wafer upon which an epitaxial film of the desired final resistivity is grown. The epilayer will contain the final device regions. This layer is thermally oxidized to the desired isolation oxide thickness. Standard DI uses an oxide thickness of 2-4 μm; however, this was reduced to 1.2 μm in this study. Next, polysilicon is deposited at high temperature to a thickness equal to the thickness of the original wafer, or about 750 μm. This polysilicon will form the substrate, which provides mechanical support only. The polysilicon can be doped if substrate biasing is required; in this study, the polysilicon was deposited undoped. The polysilicon is ground to provide a smooth back surface. The wafer is turned over and the N+ substrate material is ground to a thickness of approximately 25 μm. The remaining N+ material is then electrochemically removed, leaving only the epilayer, oxide, and the polysilicon substrate. Note that the accuracy in stopping on the epilayer is very important in fabricating uniformly thin films. The epilayer, which starts at approximately 7-10 μm in thickness, is now gently polished to the desired final silicon film thickness. This polishing procedure is very similar to the polish used as a final step by all silicon wafer vendors. Thus, an SOI structure can be fabricated utilizing DI fabrication techniques.

Bonded Wafers

The DI technology also forms the basis for the third SOI material technology — bonded wafers. The wafer-bonding process has been described in recent literature [7], [8]. The bonding process allows the long, high-temperature polysilicon deposition to be removed from the DI process. The bonding process involves the attachment of two silicon slices by a single high-temperature furnace cycle.

In this process, the starting material includes two silicon slices: one N+ substrate with the device layer grown as epitaxy (as in DI) and a second slice of arbitrary character, which is oxidized (to 1.2 μm in this study) and will become the mechanical support for the SOI structure. These two wafers are bonded together by placing them in contact with each other and then bonding at high temperature in an oxidizing ambient. The remainder of the process is the same as that for scaled dielectric isolation. The N+ layer is ground and electrochemically removed, and the epilayer is then polished to the desired thickness. Note that the polysilicon deposition, which places the wafer under stress, is not performed in wafer bonding.

Results of Material Fabrication

Using the procedures described previously, SOI wafers employing each of the three technologies were fabricated using 2 μm as the target thickness for the active silicon layers. These wafers were subsequently combined into a single lot, which was then processed using a production hardened-field CMOS flow. For control purposes, several standard 6-μm-thick N— epi on N+ bulk slices were also included in the run. The electrical characteristics derived from devices built in the SOI material using the production flow will be presented in a subsequent section; however, the actual material characteristics will first be discussed.

Figure 1 represents a histogram of the film thickness (as determined by an infrared reflectance measurement), which was obtained by using the three SOI wafer formation techniques. The epi on bulk results are shown for reference and, again, were targeted for a nominal thickness of 6 μm. The variation of a standard production epitaxy process is about ±4 percent across the lot, and this is typical of all epitaxy processes. The average SIMOX film thickness was very close to the targeted 2 μm. The observed variation of ±4 percent was similar to that of the epitaxy process. It should be noted that the variation due to the nonuniformity of the oxygen implant dose is insignificant. With a dose uniformity specificaion of ±5 percent, the variation of silicon film thickness is only 200 Å, i.e., less than the variation of the epitaxy process. The buried oxide thickness will reflect the dose variability more directly. The bonded wafers also had an average film thickness that corresponded well to the targeted 2 μm but showed a slightly larger spread in the distribution. This distribution is directly related to the control of the electrochemical etch and the final polish steps. These wafers and the scaled dielectric-isolation wafers were processed as an engineering experiment on DI production equipment. The variability represents an improvement over current production practice that is transferable to volume production. The scaled dielectric-isolation average film thickness was notably less than the targeted 2 μm, with a value of about 0.9 μm. This thickness is controlled by the final polish step, and it is believed that a proper bias can be installed to correct the average to more closely obtain the desired film thickness. Since this was an early experiment, part of the purpose was to establish the need for such a bias. It is interesting to note that the scaled dielectric-isolation technique provided a submicron SOI layer. However, the frontside processing was not tuned for this film thickness, and some of the device results to be presented below show the influence of a layer that was thinner than desired. The variability of the thickness of scaled DI was slightly larger than that of the bonded wafers and was about ±0.4 μm. Again, the nonuniformity in this case is determined by the control of the electrochemical etch and final polish, and it is encouraging that the DI processing can be controlled to this degree.

Goals for Material Production

The wafer characteristics described previously represent the results of early engineering efforts to produce SOI material. A few comments are therefore in order regarding the long-range production goals for the three technologies.

The SIMOX process provides an SOI structure with the best control over the silicon film thickness since it does not rely on any etching or polishing processes. The minimum film thickness (1000Å) would involve the original SIMOX superficial silicon layer and no epitaxy. The variation of this layer thickness would be about ±200 Å. For layers thicker than 2000 Å, epitaxy is required and will add typically ±4 percent (or 800 Å for a 2-μm film) to the variability. The oxide thicknesses possible are limited with the SIMOX process since the oxide is formed by implantation with the constraint that a silicon seed layer be preserved. This oxide thickness ranges between 0.3 and 0.5 μm with currently available implanters but could be increased if implanters with higher energy become available.

The bonded-wafer approach provides the SOI structure with grater flexibility with regard to the oxide layer thickness. The minimum silicon film thickness is proposed to be 1.0 μm, based on a conservative estimate of the control of the polishing technique. The variation of this thickness would be controlled to ±0.5 μm in a production environment. Tighter thickness variation is possible through binning, with only a yield impact. The oxide thickness does not impact any other aspect of the fabrication sequence and is available between 0.4 and 4.0 μm. This is the range of oxide thicknesses currently available with standard DI technology. Note that the thicker oxide layer available with bonded wafers, compared to SIMOX, implies a significant reduction of substrate parasitic effects. Also, it will be seen that the crystal quality available with bonded-wafer technology makes it very attractive for many applications.

The scaled dielectric-isolation specifications are very similar to the bonded-wafer specifications, due to the similiarity between the technologies. The recommended minimum silicon film thickness is 1.0 μm, which was the average result obtained in the present study. The proposed production-variation limit on this thickness is similar to that of bonded wafers at ±0.5 μm. The oxide thicknesses available are again the same as those of the current DI process, with a range of 0.4-4.0 μm. The only difference between the bonded-wafer process and the scaled dielectric-isolation process is in the formation of the mechanical support and the implications of this process on the quality of the device layer.

CMOS Device Results

As noted in the previous section, for the evaluation of devices built with the various SOI materials, a device fabrication lot was processed that was composed of wafers produced with each of the various technologies. The front-side process used was the standard Harris hardened-field CMOS process [9], which is a well-established, full-production process. The features of this process are as follows. The standard starting material is N− epi on N+ substrates, and this material was included as a control reference. The process uses a p-well technology with a p-well depth of 1.6 μm. The hardened gate oxide is nominally 325 Å and is grown in steam at 850°C. To maintain hardness, all subsequent processing steps are performed at temperatures of 850°C or less. The process uses direct moat isolation, with a 0.8-μm hardened-field oxide. Phosphorus-doped polysilicon is used as the gate electrode, and sputter-deposited 1-percent aluminum-silicon is used for the interconnect metal. The nominal, drawn gate lengths are 2.5 μm for the n-channel devices and 3.0 μm for the p-channel devices.

In Table 1, a summary of the transistor parameters, including threshold voltage, breakdown voltage, and effective channel mobility (or K') for the three SOI and epi (bulk) technologies, is shown. With regard to threshold voltage, the values are all within the process specifications. The threshold voltages of the scaled DI n-channel devices were slightly higher and exhibited more scatter than those of the other three material technologies. This resulted from the presence of a thinner (submicron) epilayer and a larger relative film-thickness variation, as described in the subsection "Results of Material

Fabrication." For the epi thickness realized on the scaled DI, the standard boron p-well diffusion region results in a higher surface concentration in this region. Simulations using SUPREM-III (as well as spreading resistance probe measurements) have verified this effect. The normal p-well junction depth is 1.6 μm. For a silicon layer of 1.15 μm, the surface concentration increased only 12 percent, but at a thickness of 0.6 μm, the surface concentration increased 105 percent.

Technology	V_{TO}V	BV_{DSS}, V	μ_{eff} (V_{GS} = 5V), cm^2/V-sec.	K' (V_{GS} = 5V), $\mu A/V^2$
		2.5-μm n-channel		
Epi (bulk)	0.91	14.9	468	24.9
SIMOX	0.85	14.3	466	24.7
Bonded	0.84	13.1	451	23.9
Scaled DI	1.09	12.4	416	22.1
		3.0-μm p-channel		
Epi (bulk)	-0.75	-14.9	151	8.0
SIMOX	-0.81	-14.3	151	8.0
Bonded	-0.85	-15.2	124	6.6
Scaled DI	-0.98	-15.3	122	6.5

Table 1 Typical transistor parameters for epi (bulk) and SOI n- and p-channel transistors.

The breakdown voltages of the transistors for the various technologies were found to be similar, averaging 14-15V. The average value of the n-channel BV_{DSS} for the bonded-wafer devices was reduced slightly, due to a few units that exhibited low breakdown voltages. The majority of the devices from the bonded wafers show a distribution that is very nearly the same as the devices from the epi (bulk) wafers. Also, BV_{DSS} for the scaled DI transistors had a fairly wide distribution. The breakdown voltage of the n-channel SIMOX and scaled DI transistors tended to be a soft breakdown. This is exemplified in Fig. 2, which shows representative reverse-biased characteristics of a N+/P— diode for the four technologies. The diode from bonded wafers exhibited characteristics most closely resembling epi (bulk) material. The rate of increase in leakage current with reverse bias prior to the avalanche breakdown region for epi (bulk) and bonded wafers was about 0.02 dec/V, while the SIMOX and scaled DI devices had a value of 0.2 dec/V. This data is shown in Table 2. Thus, the reverse-biased leakage current increases with voltage at a rate 10 times higher for SIMOX and scaled DI N+/P— diodes compared to epi (bulk) or bonded-wafer diodes. For the P+/N— diodes, this effect was not observed. The P+/N— diodes on all SOI materials did not exhibit a soft breakdown characteristic.

The third column of Table 1 indicates the effective mobility (at $|V_{GS}| = 5V$) for the technologies. It was observed that SIMOX n- and p-channel average mobilities were very nearly the same as their epi (bulk) counterpart. The mobilities

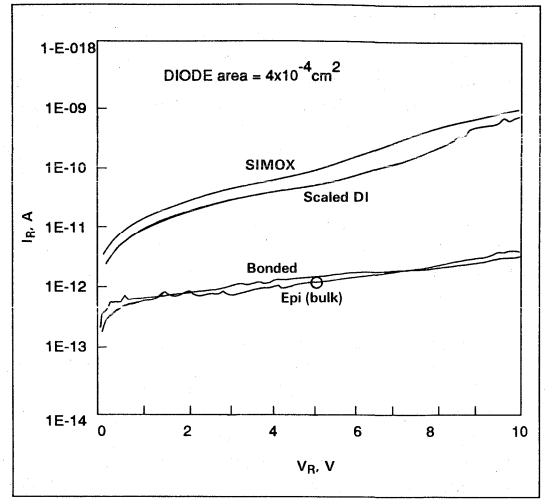

Fig. 2 Reverse-biased junction leakage characteristic of N+/P— diodes for epi (bulk) and the various SOI technologies.

Technology	I_R, nA/cm^2	$\Delta I_R/\Delta V_R$ dec/V	n
Epi (bulk)	10	0.02	1.07
SIMOX	400	0.2	1.45
Bonded Wafers	10	0.02	1.15
Scaled DI	2500	0.2	1.48

Table 2 N+/P— diode characteristics for epi (bulk) and the SOI technologies.

for the scaled DI and bonded-wafer devices were reduced on average by 11 and 3.6 percent, respectively.

Figure 3 shows histograms of the n-channel effective mobility. The average n-channel mobility for the bonded wafers was reduced by a few units that had anomalously low values, similar to the BV_{DSS} distribution. The majority of the bonded-wafer devices showed n-channel mobilities very similar to the epi (bulk) devices. However, the distribution for the p-channel transistor mobilities for bonded wafers was significantly different than that for epi (bulk). There was a substantial amount of wafer-to-wafer variation here, indicating that there may be film stress reproducibility concerns with the bonding process, which affects hole mobility. It should be noted that these wafers were from an early bonding experiment, and refinements are in progress that address this issue.

A very important parameter of any CMOS technology is leakage current. The comparison was made for the three SOI technologies versus epi (bulk). In Fig. 4, a histogram of reverse-biased leakage current (I_R @ V_R = 5V) for a large N+/P— diode is shown. The representative leakage for these diodes in units of nA/cm^2 is shown in Table 2. The epi (bulk) and bonded-wafer diode leakage characteristics were very similar. The SIMOX diode leakage current was about 40 times larger than the epi (bulk), while scaled DI leakage showed a broad distribution. However, many of

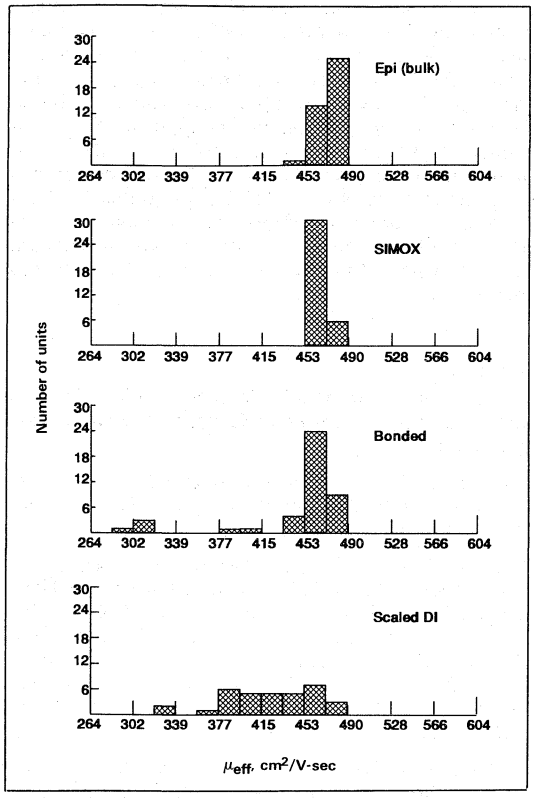

Fig. 3 Histogram of 2.5-μm n-channel effective mobility (V_{GS} = 5 V) for epi (bulk) and the SOI technologies.

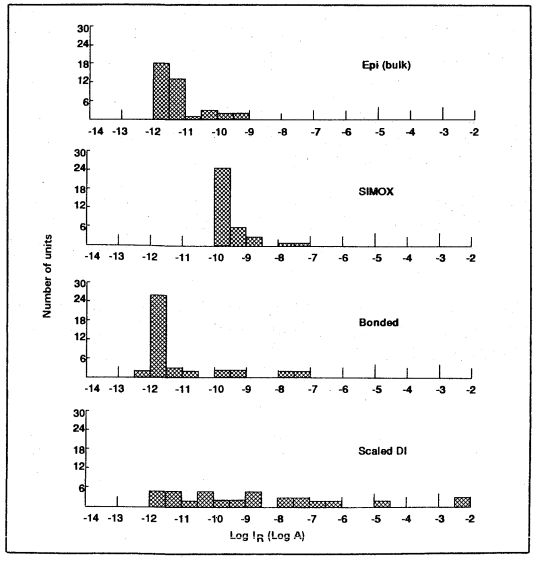

Fig. 4 Histogram of reverse-biased (V_R = 5 V) junction leakage current of N+/P− diode for epi (bulk) and SOI technologies.

the scaled DI diodes had leakage current as low as the epi (bulk) diodes. The scatter in the distribution increased the average values considerably. Similar results were obtained for the P+/N− diodes.

Also in Table 2, the average value of the diode ideality factor, n, for the four technologies is shown. The ideality factor is defined by the equation

$$I \text{ @ } I_0 \exp(qV/nkT)$$

where n = 1.0 for an ideal diode dominated by diffusion current. From the preceding, the bonded-wafer diodes resemble the epi (bulk) diodes most closely. The SIMOX diodes, as expected, are influenced by recombination currents. However, these values are still acceptable, indicating relatively good starting material. The diodes of the scaled DI wafers were observed to have ideality factors near those of the SIMOX diodes, again confirming stress effects in this material.

Total Ionizing Dose Radiation-Hardness Results

Transistors from the three types of SOI material were irradiated using a Co-60 Gamma Cell-200 with a dose rate of approximately 100 rad (Si)/sec. The n-channel devices were biased with the gate at +5.5V and the source, drain, and body at ground. The p-channel devices were biased with the gate, source, and body at +5.5V and the drain at ground. These bias conditions were chosen to maximize the radiation effects for worst-case digital circuit conditions.

Figures 5 and 6 shown n- and p-channel threshold voltage shifts versus total dose for the various technologies. As can be seen, all technologies displayed comparable gate oxide hardness. The scaled DI devices were, however, removed from testing after 250 k-rad (Si) due to excessive leakage current, which was assumed to be due to the backside n-channel device. As such, no threshold shift data is displayed in Figs. 4 and 5 beyond 250 k-rad (Si). Recall that the scaled DI wafers had very thin epitaxial silicon (<0.5 μm worst case), and no deep implants were added to the process to reduce back-channel leakage. The SIMOX and bonded-wafer transistors, which were fabricated in much thicker epitaxial layers, showed an increase in leakage current with total dose that was similar to that of epi (bulk) transistors.

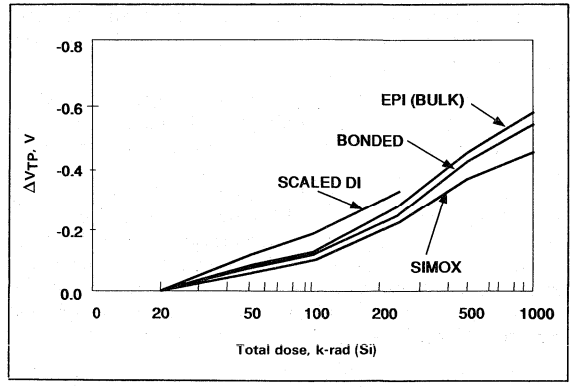

Fig. 5 Threshold voltage shift versus total ionizing dose for 2.5-μm n-channel transistors.

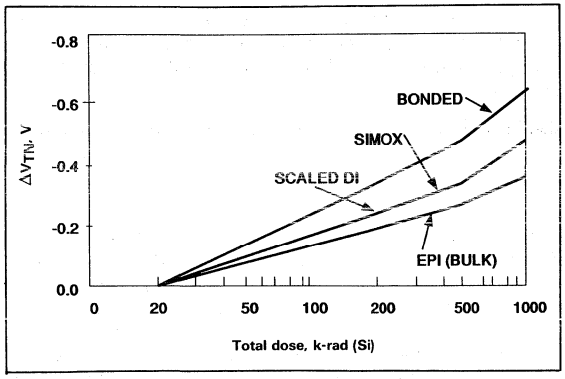

Fig. 6 Threshold voltage shift versus total ionizing dose for 3.0-μm p-channel transistors.

Summary and Conclusions

The results of this study show that the material technologies under evaluation each have unique characteristics that must be considered relative to the requirements of the application. The primary trade-off is found to be the quality of the silicon layer versus the control of the thickness of that layer. The silicon film quality has been evaluated with the result that the bonded-wafer approach provided generally better electrical characteristics. All material technologies resulted in CMOS devices with basic parameters within specification for the process used to fabricate the devices. It was found that SIMOX material contained defects that caused an increase in junction leakage current. Scaled dielectric-isolation material exhibits a high stress state in the film, which also produced an increase in the junction leakage current. Work is in progress to reduce the junction leakage on these technologies, which may eliminate this difference.

The ability of these technologies to provide the desired physical structure with adequate control was also evaluated. It was found that each technology achieved the SOI structure with some limitations. SIMOX technology is limited in the range of oxide thickness that can be realized. Bonded-wafer and scaled DI technologies are limited in the minimum thickness of silicon possible and the minimum variation of that thickness across the wafer. These parameters are important considerations for the selection of a technology for a given application.

The frontside oxide radiation hardness was also investigated on each of the three SOI technologies. All three technologies showed gate oxide hardness comparable to the epi (bulk) controls. No consistent trend was found to indicate any generic problem with oxide hardness on SOI material. This allows the general conclusion that all of these SOI approaches are feasible for radiation-hardened integrated circuits. Note that the back-channel leakage observed on the scaled DI devices strongly indicates the need to properly design the frontside process, such as the use of deep back-channel implants, to achieve a radiation-hardened structure.

Finally, some applications are suggested by the results presented in this paper. Since the SIMOX devices showed the tight parameter distributions and the best surface mobilities, this is the indicated technology for immediate, high-density, radiation-hardened CMOS integrated circuits, particularly if a very thin (submicron) film is required. The bonded-wafer results, especially the low leakage currents, are favorable for advanced bipolar applications. This is substantiated by the fact that bipolar applications require somewhat thicker films, reducing the importance of the minimum film thickness and variation. Bonded wafers may also be attractive for some CMOS applications, such as very low-power or high-voltage circuits, where the film thickness is not required to be minimized. Scaled dielectric isolation has potential applications very similar to the bonded wafers.

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Designing For Radiation Hardened Application Specific IC's

J.S. Tirado, D.C. Young, D.A. Carver
Harris Semiconductor, P.O. Box 883
Melbourne, FL 32902-0883

Introduction

Since 1942, when the Joint Army Navy (JAN) program was formed, the government has used a Qualified Products List (QPL) concept for providing parts to military systems. Today, with advances in technology, the push is now towards Application Specific Integrated Circuits (ASIC) and VHSIC/VLSI circuits. The government is heavily engaged in developing a new Qualified Manufacturer's List (QML) program for qualifying these new devices and the use of Statistical Process Control (SPC) techniques which modify the screening and qualification testing currently outlined in Mil-M-38510. The added requirement for radiation hardened circuits, however, has introduced a set of issues that, in some cases, is not fully addressed in QML and SPC procedures.

In this paper, we will address the QML and SPC concepts and how it affects ASIC's going into radiation hardened systems. We will demonstrate how Harris Semiconductor has developed a library of rad-hard standard cells and what special design techniques were made to insure consistent rad-hard ASIC circuits. Special techniques are needed with ASIC designs because radiation hardness is not only process, but design and layout dependent as well. We will also discuss the type of controls that are needed to insure ASIC designs will continue to be rad-hard in spite of the many configurations that can be developed using standard cells.

QML

The present QML concept calls for certifying a manufacturers line and process through SPC programs and periodic qualification testing. SPC is used to insure quality and reliability are obtained without excessive testing by controlling each element of the manufacturing line. So long as appropriate SPC controls are used, various devices can be built on the same process flow as long as the design and fabrication process is adequately monitored. This is fine for standard devices, but is not enough for devices with radiation requirements. Present radiation hardness criteria under the QPL process calls for controlling the passivation, diffusion, and sintering or annealing temperature/time for RHA circuits and performing Group E radiation testing on lot samples. This same criteria has been levied on the QML process with some minor modification. During wafer qualification special Technology Characterization Vehicles (TCV's), or test structures, and a number of Process Monitor (PM) structures, will be incorporated to charcterize the technology's capability for producing rad-hard circuits. How this will be done, however, is not explained. TCV's and PM's may be able to monitor process, but it may be more difficult to monitor how the design contributed or degrades the radiation hardness of ASIC circuits. Additionally, Standard Evaluation Circuits (SEC's) will monitor long term reliability of the wafer fabrication facility. These SEC's will contain, as a minimum, one half the number of transistors expected to be used in the largest microcircuit to be built on the QML'd line. SEC's, however, will be used only during initial qualification and at least once a year thereafter. Finally, qualification will only be required on a lmited number of demonstration vehicles for generic qualification. Qualification of each newly designed device will not be required so long as the circuits are manufactured using the same process flow. For the QML program this means that a device from a "rad-tolerant" process could end up softer than expected. In order to control hardness a number of things must be taken into consideration, particularly for ASIC circuits.

1. Process parameters must be effectively controlled.
2. Test structures must be able to monitor process changes in electrical characteristics pertinent to radiation hardness.
3. Circuit modeling must include device radiation degradation models.
4. Controls must insure that layout does not degrade the device hardness characteristics.

We will suggest that by implementing adequate controls the radiation hardness of devices built using the QML process can be assured.

Ionizing Radiation Effects

With the advancement of newer process technologies and resulting thinner gate oxides, many manufacturers are claiming radiation hardness of their products. Even though the thinner gate oxides do allow higher tolerance levels for digital CMOS circuits to total dose radiation effects, most of the libraries were not designed or tested specifically for radiation environments and exhibit high field leakages. These types of products are considered radiation tolerant, since their design has not been optimized nor modified for radiation hardened use. A radiation hardened process has been specifically designed and characterized with radiation environments in mind. To illustrate this point, we can compare a few radiation hardened and radiation tolerant device parameters. Figure 1 and 2 shows the N channel threshold shift and normalized subthreshold swing variability as a function of total dose exposure, respectively. Each figure contains a curve representing a radiation hardened and radiation tolerant process response variability to total dose irradiation for equivalent gate oxide thicknesses. In

the case shown, the radiation tolerant process variability seems to be roughly twice that of the radiation hardened process. As you can see, libraries which were not designed with radiation environments in mind may become non-functional due to the high device parametric variability. Thinner gate oxides do not guarantee radiation hardness over all process conditions.

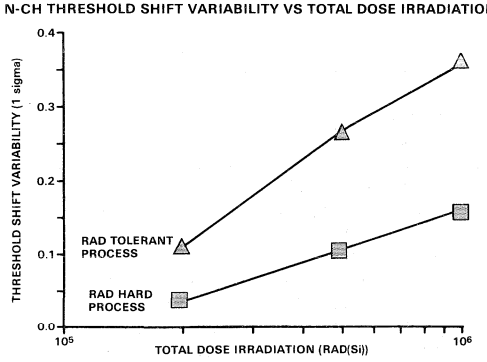

Figure 1. N-channel threshold shifts (ΔVTN) variability as a function of ionizing radiation. Depicted are curves representing a radiation hardened and radiation tolerant process response.

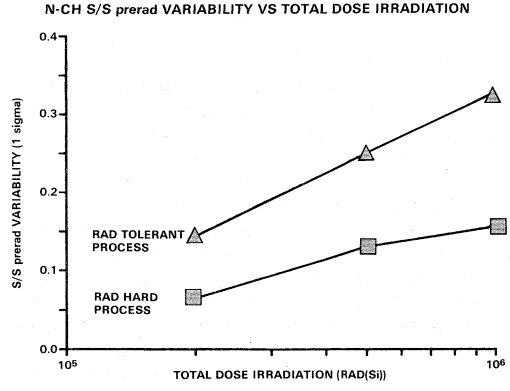

Figure 2. N-channel normalized subthreshold swing (S/S pre-rad) versus total dose radiation exposure. Curves representing a radiation hardened and radiation tolerant process response are shown.

Since there is no "standard" qualification procedure, it is important to examine the procedures used by the vendor for QML qualification. A cell library designed for a radiation hardened environment should have several characteristics, since there are several different types of radiation environments and applications to be considered in the design. Radiation stimuli are numerous and can come from natural or man made sources. The radiation exposure can either be long term, low level exposure as might be encountered in a spacecraft application in low earth orbit or a high dose, very brief exposure as might occur as the result of a nuclear blast. Each situation creates different types of effects and requires different design techniques and testing procedures.

For example, total dose accumulated by ionizing radiation such as gamma or x-ray has specific effects. The first dominant effect is a threshold shift that occurs due to the accumulation of trapped oxide charge (positive in nature) in the gate and field oxides during the ionizing radiation event [2,3]. The second effect is device drive degradation that occurs as a result of a reduction in channel mobility in irradiated MOS devices due to the presence of both trapped oxide charge near the $S_iO_2 - S_i$ interface and interface states [2,3].

As the transistor threshold is lowered in the N device, the Propagation Time High to Low (TPHL) of the logic gate decreases. The opposite occurs in the P type transistor. The threshold increases, making it more difficult to turn on. The Propagation Time Low to High (TPLH) of the logic gate increases. This effect causes a drastic skew in the TPLH and TPHL times for a gate. Such skews can create race conditions which could make the circuit non-functional. Transistor drive reduction increases the delay of the logic gate. If the transistor is in the output of the I/O buffer, not only will speed be affected but V_{OL} and V_{OH} may shift out of specification, creating electrical interface problems with other system circuitry. Correct modeling of these effects must be used when performing logic and timing simulations.

These effects must be simulated to generate accurate timing models when the cell library is designed. While used by many vendors, simple scaling of pre-radiation delays is not sufficient to accurately model the post-radiation effects. Transistor models for specific accumulated total dose levels must be used to simulate threshold shifts and device degradation so accurate timing information can be modeled. This will allow the circuit to remain functional and within specification after a particular dose.

HSC-RH Library

Harris developed a radiation hardened CMOS standard cell HSC-RH library. To assure radiation hardness, test chips were designed to observe individual cells of a hardened field technology. The first was a bulk single level metal CMOS with 2.5 micron N-channel (drawn) and 3.0 micron P-channel devices. The second was a double level metal design with 2.0 micron and 2.5 micron devices. These test chips were tested for total ionizing dose, transient dose, and Single Event Upset. Using these test chips, we were able to demonstrate a hardened cell design in excess of 1 mega rad (Si) total dose, no data upset at rates of 10^9 Rad (Si)/sec, a SEU LET threshold in excess of 34 MeV/mg/cm_2, and an immunity to latchup [1].

Design Controls

SPC is the key to the QML process being successful. Standard SPC programs insure the quality of gate and field oxides through monitoring of thicknesses, contaminates, and equipment cleanliness. Although this is adequate for commercial applications to insure good product, quantitative factors which influence process tolerance to radiation are not always monitored with traditional controls. In fact, physical process attributes which influence radiation performance are generally very difficult to monitor in a normal manufacturing environments due to time limitations and lack of sophisticated measurement equipment. The alternate solution is to monitor device parametric radiation response. With the availability of wafer level irradiation sources, such as the Aracor 10KeV X-Ray source, device parametric response to ionizing radiation can be SPC monitored without impacting the manufacturability of a process to a large degree. The obvious question is what device parameters need to be monitored.

Circuit simulators predict overall circuit performance using specific device component models. In general, logic circuits are most influenced by transistor threshold and drive parametric characteristics. The transistor threshold parameter may be monitored by direct calculation from actual transistors or by flat band voltage derived from MOS capacitors [3,5]. The device drive degradation [$K' = (u_n WC_o)/L$] may be determined by change in channel mobility, subthreshold swing [5], transconductance [5], or interface state density of a transistor [5,6]. On the other hand, capacitance at mid-gap (Cmg) and strong inversion (Cinv) may be used to derive the change in interface state density as shown by Winokur [6]. Additionally, parasitic devices (field, sidewall, etc.) generate leakages which need to be minimized and monitored in order to insure post irradiation circuit performance functionality. As an example, N channel field device off and subthreshold leakages increase with exposure to ionizing radiation as shown by Figure 3.

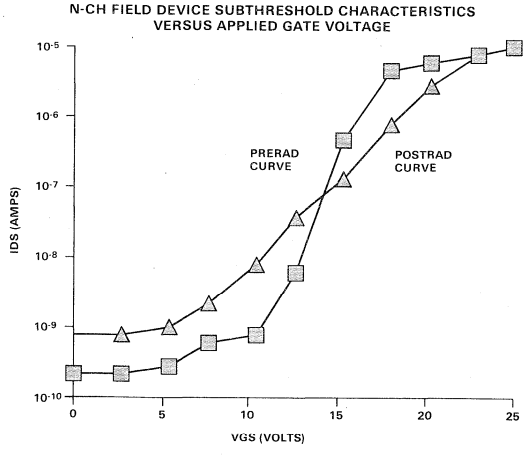

Figure 3. N-channel field device subthreshold characteristics versus applied gate voltage. Curves representing pre-rad and post-rad conditions are shown for comparison.

As stated above, two types of devices may be used to track radiation performance of a process, capacitors or transistors. Both devices have advantages and disadvantages. Typically MOS capacitors are easier and quicker to fabricate than actual transistors but require more complex measurement techniques and equipment than residues in a manufacturing facility. Also, capacitors do not always accurately indicate parasitic device (field, sidewall, etc.) leakages due to non-accountable layout and lateral electric field dependencies. Therefore, SPC should be implemented using transistor type devices as the monitoring device.

With the above discussion in mind, SPC control limits should be developed on critical device parameters for a specific total dose irradiation exposure. Each QML process qualification will have to identify the key device parameters which effect circuit performance. At Harris the following device parameters are required to be controlled to insure hardness; active transistor thresholds and drive degradation, parasitic field transistor off and subthreshold leakages. Parametric testing and ionizing radiation exposure can be conducted at the wafer level with the use of standard electrical measurement equipment and an Aracor 10KeV X-Ray source. Monitoring will be done at periodic time intervals on process TCV's to insure the design transistor radiation parametric SPC response has been met. As long as the response lies within the control limits, circuit radiation response should be equivalent to that displayed during process circuit qualification under the QML process.

Dose Rate Radiation Effects

Additionally, continued functionality after a total dose exposure is not the only requirement for radiation hardened circuits. The effects of other types of radiation must be characterized and fully understood and considered in the development. Cosmic rays which are of great concern in space environments can cause latch up, data upset, or random errors in circuits. Particular attention must be given to these high energy particles in the original cell design. Accurate models must be used to determine the critical charge for device upset. This is extremely important in bi-stable circuits such as latches, flip-flops, and memory cells. The charge collection volume must be minimized.

Effects of transient radiation must also be considered. Immediately after a nuclear event, there is an instantaneous burst of gamma radiation. This burst of radiation is very brief and on the order of 25 ns. The pulse is short but the fluence is very large. When a circuit is exposed to this type of ionizing radiation, a tremendous number of hole electron pairs are generated. These additional hole-electron pairs appear as a photocurrent. This large amount of current will flow in the circuit until most of the hole electron pairs recombine. This type of event will cause a disruption in the circuit but if properly designed the circuit can return to operation after the pulse. A major problem is power rail collapse or burn out due to inadequately sized power buses. If adequate power rails are not provided to handle these large currents, fusing can occur resulting in a non functional circuit after the radiation pulse. Harris has created circuit simulation models which assist in calculating the total current generated by such an event. This allows

properly sized distribution lines to be used insuring that burn out does not occur resulting in a functional circuit after the event.

Each of these affects are discussed at much greater length and in more depth in other sources. The intent is to stress the fact that most vendors concentrate only on ionizing radiation and there are more types of radiation environments to consider.

Harris Semiconductor has constructed circuit simulation models for each of the above effects and considers each when designing a new cell library for radiation hardened circuits. Each new cell library is used to construct a test chip for characterization and evaluation purposes. Specific test structures are included which allow characterization of each of the effects described above.

Standard test procedures are used to characterize each new cell library, design methodology, and process at Harris. As an example, a recent project with Silicon Compiler Systems to develop a radiation hardened silicon compiler for the Harris processes is presently nearing completion using this testing methodology. Since the same test were performed on other cell libraries for this particular process, a consistent means for evaluation exists. The entire design process at Harris has been developed with QML for radiation hardened circuits in mind. Harris emphasizes that the above procedures must be followed to ensure that each new circuit designed for radiation hardness will in fact work in the expected environment.

Conclusion

In order to insure radiation hardness for devices designed to be manufactured on QML processes, it will be necessary to develop SPC techniques and TCV's to insure rad-hard ASIC designs. Controls will need to monitor specific process design and layout parameters, for the varied radiation requirements such as total ionizing dose, transient dose, and SEU. TCV's will also have to be developed and tested using new equipment such as the Aracor 10 KeV X-Ray source to monitor process parametric changes and insure that they remain within specified boundaries. Also, modeling techniques for ASIC circuits, must take into account the effects of varied radiation effects systems in order to assure radiation hardness for military.

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Radiation Hardening of Vertical DMOS (VDMOS) Power MOSFETs

by C. Frank Wheatley

This Note discusses the rad-hard testing and performance of Harris off-the-shelf rad-hard power MOSFETs. Total dose (gamma), neutron exposure, dose rate (prompt gamma or gamma-dot), and single-particle-destruct or single-event-upset (SEU) are addressed. Comparisons are made between pre-rad devices and the Harris GR series: GRM6756, GRM6758, GRK6764, GRK6766. Both device and circuit considerations are addressed. Future rad-hard power MOSFETs are also discussed.

In developing the GR-series of vertical DMOS, VDMOS, power MOSFETs, the goal established was to serve military and industry needs in tactical and aerospace applications involving radiation environments. Some subtle changes in power MOSFET structure and processing were made to achieve this goal. A secondary objective was to offer parts with exactly the same specifications as industry-standard JEDEC-registered parts. Both goals were accomplished with the exception of a few specifications of minimal consequence. These exceptions were tradeoffs chosen so as to minimize compromises in radiation hardness. Harris GR-series offerings include the Hex 3 and Hex 5 die-size MOSFETs with BV_{DSS} of 100 and 200 volts. These parts are identified as the GRM6756, GRM6758, GRK6764, and GRK6766, and are pre-rad look-alikes of the JEDEC-registered 2N6756, 2N6758, 2N6764, and 2N6766.

Post-rad specifications are offered on all parts at the conservative fluence level of 2E12 neutron/cm^2. In addition, four levels of gamma hardness are post-rad specified by a suffix notation of M, D, R, or H, resulting in sixteen different parts. The suffix notations denote hardness at 3, 10, 100, and 1000 krad(Si), respectively.

Hardness to total dose is assured by measuring a sample from each wafer-production lot. Hardness to neutron irradiation is assured by the capability signified in the 2E12 specification, as described further below in the section on neutron radiation.

The radiation hardness achieved in the GR series was limited to the goal of matching JEDEC parts spec.-for-spec. However, superior total dose, dose rate, neutron, and single-event-upset (SEU) hardness is attainable, and will be offered, along with a greater variety of die sizes and voltages, in the future. Rad-hard p-channel MOSFETs will also be offered.

The Vertical DMOS (VDMOS) Power MOSFET

The industry-standard power MOSFET, the VDMOS, is shown in cross section in Fig. 1. A review of the structure of this device shows significant physical differences from the MOSFET used in logic circuitry. As a consequence of these differences, hardening of the power MOSFET is more subtle than geometric scaling of a small logic FET would indicate. There can be many parallels, however.

When the drain voltage is very low and the gate is positively biased, an accumulation layer exists at the gate oxide/n^- interface. This accumulation layer may be thought of as providing and n^+ drain for the lateral MOSFET, where the source is labelled and the channel exists at the p-body

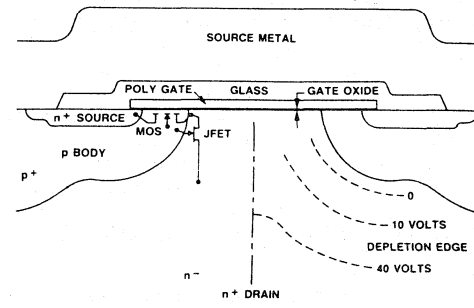


Fig. 1 Cross section of Power MOSFET.

interface. As the gate is biased more positively, the n^+ accumulation layer and the n^+ source are connected by an n^+ inversion layer formed at the gate oxide/p-body interface. The first difference we see between a logic FET and the power MOSFET relative to radiation hardness is that the surface concentration of the p-body, forming the channel, is nonuniform. In fact, it is formed by lateral diffusion and is gaussian in nature.

If the n^+ accumulation layer forms the lateral MOSFET drain, we must ask where the voltage is supported. This n^- epitaxial region directly beneath the accumulation layer is commonly called the "neck" of the power MOSFET, and is usually treated as though it were a parasitic resistor. It is, in fact, a vertical JFET, where the cathode is the n^+ accumulation layer, the anode is the n^- substrate generally thought of as the power MOSFET drain, and the sides of the p-body forming the neck function as the JFET gate. This structure is schematically shown in Fig. 1 at the left side of the neck.

Note that a grounded gate-cascode connection is made from the vertical JFET to the lateral MOSFET. The positive edge of the depletion layer is shown at the right side of the neck for applied voltages of 0, +10, and +40 volts. The negative edge exists in the p-body, and is omitted for clarity. It follows that most of the applied voltage is shielded from the gate oxide by the vertical JFET.

In addition, a p-n diode is always present. The p^+ diffusion contacted by the source metal is the anode, and the n^- epi layer followed by the n^+ substrate to the back metal (not shown) is the cathode.

An n-p-n transistor also exists that provides secondary photocurrent. The source metal to the n^+ source diffusion acts as the emitter, with the p-body serving as a base and the n^- followed by the n^+ substrate providing the collector function. the base of this transistor is short-circuited to the source metal by way of the low-resistivity p^+ diffusion.

Neutron Irradiation

When the silicon-crystal lattice in a power MOSFET is irradiated with neutrons, some silicon atoms are displaced, causing lattice damage that results in many vacancies and interstitials. With sufficient temperature and time, much of the damage will anneal as the atoms revert to their lattice sites. Of course, some other nearby atoms, such as oxygen, the heavy metals, etc. may occupy the site vacated by the displaced silicon atom and exclude the possibility of annealing. In any event, the damage-induced mid-gap states will annihilate some free carriers. Since the silicon resistivity varies inversely with the carrier concentration, a rise in resistivity will result with incresing neutron fluence (neutrons/cm^2). Buehler[1] developed an empirical relation as plotted in Fig. 2.

The mid-gap states also serve as recombination centers for both holes and electrons, reducing the carrier lifetime. The point defects may also act as scattering centers, reducing bulk and surface mobilities. A transmutation of silicon to phosphorus also occurs, but may be neglected for this discussion.

To support the required BV_{DSS} (blocking voltage) for a given VDMOS power MOSFET, it is necessary that the epitaxially deposited, lightly doped layer of silicon be of a minimum value of resistivity, as shown in Fig. 3. Current flowing vertically through this epitaxial layer encounters a resistance (R_{epi}) that contributes to the value of r_{DS}(on). R_{epi} is a function of epitaxial resistivity and thickness as well as a form factor. The relative pre-rad contribution of R_{epi} to r_{DS}(on) is shown in Fig. 4 as a function of BV_{DSS} for power VDMOS structures in current use.

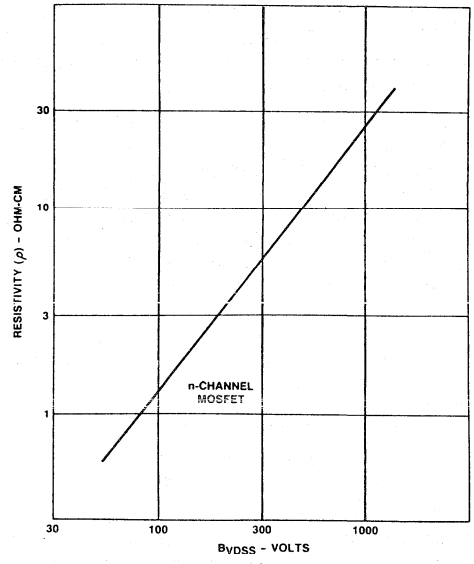


Fig. 3 Minimum resistivity capable of supporting a desired voltage.

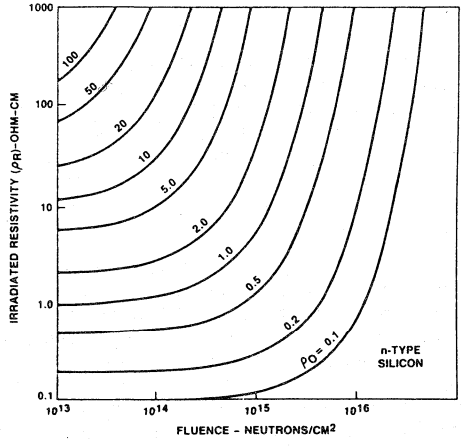


Fig. 2 Increase of n-type silicon resistivity vs neutron fluence, after Buehler[1].

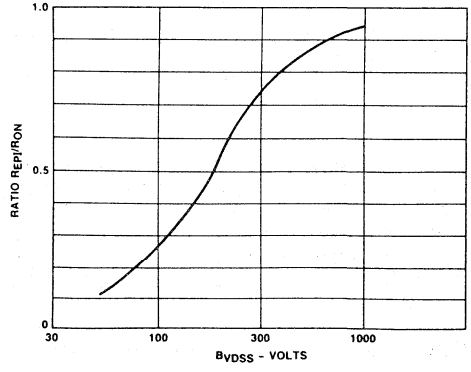


Fig. 4 The on resistance of a power MOSFET is dominated by the epitaxial resistance in high-voltage parts.

The sensitivity of $r_{DS}(on)$ to changes in R_{epi} is an order of magnitude lower in low-voltage VDMOS power MOSFETs than in high-voltage devices; Fig. 4. In addition, Buehler's data shows that the onset of neutron-induced resistivity increase for low-voltage epitaxial layers occurs at an order of magnitude higher fluence level than for high-voltage epi. The combination of the information from Figs. 2, 3, and 4 into Fig. 5 shows the two-order-of-magnitude advantage enjoyed by low-voltage VDMOS power MOSFETs. It is assumed in Fig. 5 that channel surface mobility is not a strong function of neutron fluence at the high inversion levels commonly employed for $r_{DS}(on)$ characterization. There has been some experimental verification of this about the 1E14 fluence level.

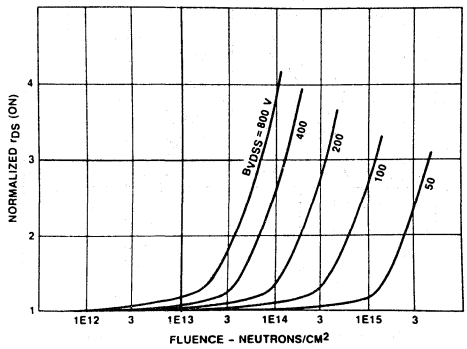


Fig. 5 Power MOSFET on resistance increases as a function of neutron fluence and breakdown voltage.

Circuit arrangements favoring low BV_{DSS} devices are encouraged. These arrangements may include low supply voltage, bridge-output circuitry and/or series-connected MOSFETs.

P-channel VDMOS power MOSFETs behave similarly to the above discussion.

Total Dose — Gamma

Exposure to gamma irradiation is generally provided by a Co^{60} source at a fixed dose rate for a chosen length of time, thereby providing a total dose. Total dose is expressed in units of rads(Si), and is applied under device bias conditions. Various first-order approximations assume the device behavior to be independent of dose rate and annealing after cessation of exposure. These approximations are marginally valid.

Gamma radiation, when absorbed, generates hole-electron pairs in the silicon and silicon dioxide. If bias is applied, a current flow will result where the holes migrate toward the negative potential and electrons toward the positive potential. The total-dose exposure can result in trapped holes in oxides and dangling bonds at the silicon-silicon dioxide interface, a situation that continues to modify the device long after cessation of exposure.

Trapped Holes

Trapped holes in the oxide create a field at the silicon-silicon dioxide interface that attracts electrons. The result in an inversion layer at the channel of the MOS if the oxide is gate oxide and the MOS is an n-channel. A negative gate bias must be applied to overcome this inversion layer. The threshold voltage is thought of as shifting negative. If the oxide is the thick field oxide commonly used to fabricate the high-voltage edge termination, the electrons will produce an accumulation layer that will modify the pre-rad design for high-voltage termination.

The electrons in the oxide rapidly recombine, but the holes move much more slowly and become trapped. If we assume a gate is biased positively during the gamma exposure, the positive trapped charge forms very close to the silicon; a considerable negative gate bias is then required to offset the effect of the positive trapped charge. However, a negative *in situ* gate bias encourages hole trapping very close to the gate electrode and far from the silicon. As a consequence, the threshold voltage appears to shift negatively very little. The above discussion applies to p-channel as well as n-channel MOS. Of course, a negative shift in threshold voltage will cause an n-channel MOS to increase conduction, whereas a negative threshold voltage shift in a p-channel MOS will drive is further from conduction.

Fig. 6 compares a nonrad-hard power MOSFET to the GRK6766H rad-hard power MOSFET at 100 krads(Si) with +10 volts *in situ* gate bias and zero volts drain bias. The

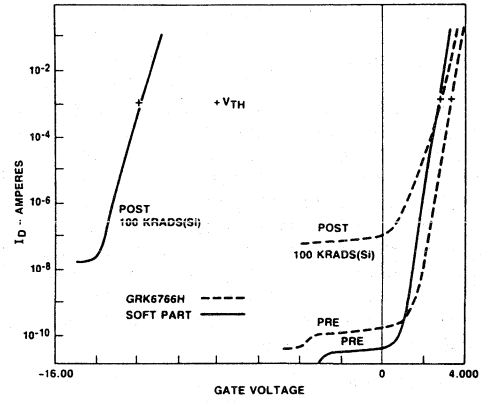


Fig. 6 Log drain current vs gate voltage; drain voltage is 5 volts. The soft part and the GRK6766H are both irradiated to 100 krads (Si) with +10 volts *in situ* bias on the gate.

curves are a plot of log drain current vs linear gate voltage with 5 volts on the drain, and show pre and post-rad behavior. There are subtle changes in subthreshold slope and leakage current that will be discussed later, but the major feature is the great difference in threshold voltage shift. Threshold voltage is arbitrarily defined as the gate voltage where $I_D = 1$ mA. The commonly used method of measuring threshold voltage by connecting gate and drain together will result in an erroneous reading of tens of millivolts positive for the nonrad-hard part of Fig. 6 rather than many volts negative, hence this method must be used with discretion.

Fig. 7 compares the Harris GRK6766H rad-hard power MOSFET in two different *in situ* bias conditions, +10-volt gate and −10-volt gate; drain voltage is zero in both cases. Again, this comparison is for pre and post-rad at 100 krads(Si).

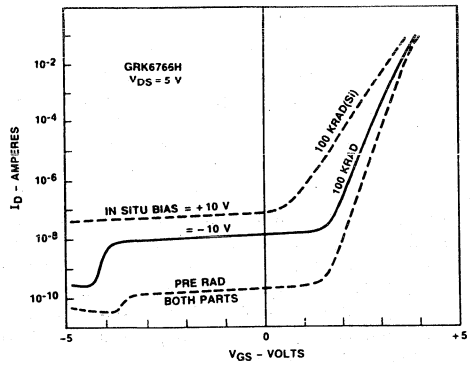


Fig. 7 Comparison of −10V to +10V *in situ* bias for the GRK6766H.

Interface Trapped Charge

Interface trapped charge (interface states, surface states) results in a more positive threshold voltage for the n-channel and a more negative threshold voltage for the p-channel MOSFET. It is clear that a cancellation may result in the n-channel, where the threshold voltage will not appear to shift even though the MOSFET is only moderately hard. Threshold-voltage shifts caused by trapped oxide holes and interface states are additive for p-channel MOSFETs. With sufficient temperature and time, both trapped holes and interface damage will anneal. However, unless they anneal at the same rate, the moderately hard n-channel device with cancelling effects will show itself to be non-hard. This phenomenon is one of various forms of "rebound," where additional damage appears to occur after cessation of irradiation.

Further examination of Fig. 7 reveals a change in the subthreshold slope, which is measured in units of millivolts per decade of current. This change reflects the increased Q_{ss} brought about by the interface damage. The subthreshold slope change will not impair normal circuit operation, provided the I_{DSS} drain leakage current is not influenced.

It should be further noted in Fig. 7 that a "shelf" exists where the drain current does not vary with gate bias. As the gate voltage is made sufficiently negative, the drain current is reduced one or two orders of magnitude below the "shelf" level. This condition is probably caused by the interface damage in the neck region of the power MOSFET, as shown in Fig. 1, where the lightly doped n^- epi reaches the surface. This interface inverts and is ohmically connected to the p body under sufficient negative gate bias.

The leakage current was measured, pre and post rad, for various devices exposed to 1 Mrad(Si) and various *in situ* bias conditions. The gate was established at zero volts.

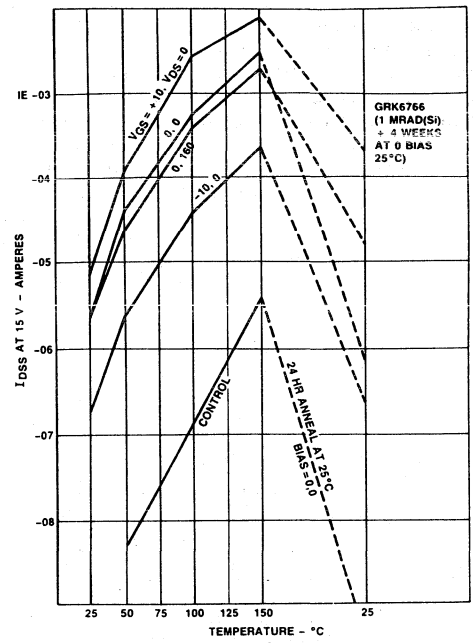


Fig. 8 Leakage current vs temperature for various *in situ* bias conditions. Note the 24-hour recovery, and see the measurement disclaimer in text.

The drain voltage was varied from several volts to 80% rated BV_{DSS} and the temperature from +25°C to +150°C and back to +25°C.

The data seemed to normalize, but was unreliable in that annealing apparently caused a reduction in drain current during the 30 seconds or so required for the junction temperature to stabilize at the increased temperature. The reading the next day at 25°C showed some rebound. The results, plotted in Fig. 8, indicate the high-temperature dependence of leakage current.

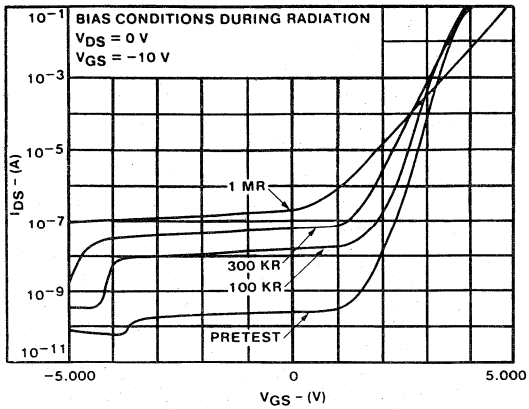
Fig. 9 shows the log drain current, linear gate-voltage plot for the GRK6766H under conditions of pre-rad, 100, 300, and 1000 krads(Si). All five of the *in situ* bias conditions described below are displayed:

Bias Conditions

(1)	$V_{GS} = -10V$,	$V_{DS} = 0V$
(2)	$V_{GS} = +10V$,	$V_{DS} = 0V$
(3)	$V_{GS} = 0V$,	$V_{DS} = 0V$
(4)	$V_{GS} = 0V$,	$V_{DS} = +160V$
(5)	$V_{GS} = -10V$,	$V_{DS} = +160V$

Bias conditions (2) and (4) are probably sufficient to assure hardness, although all five should be examined.

A plot of typical threshold voltage vs total dose is shown in Fig. 10 for all five *in situ* bias conditions. Fig. 11 shows the value of typical BV_{DSS} vs total dose in a composite of all five *in situ* bias conditions; these results are already substantially improved.



I_{DS} VERSUS V_{GS} AT A FIXED V_{DS} = 5 V

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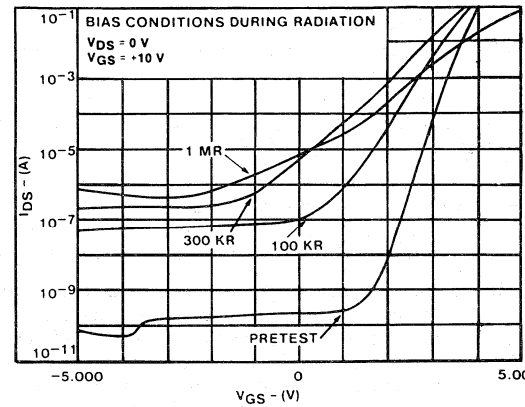

I_{DS} VERSUS V_{GS} AT A FIXED V_{DS} = 5 V

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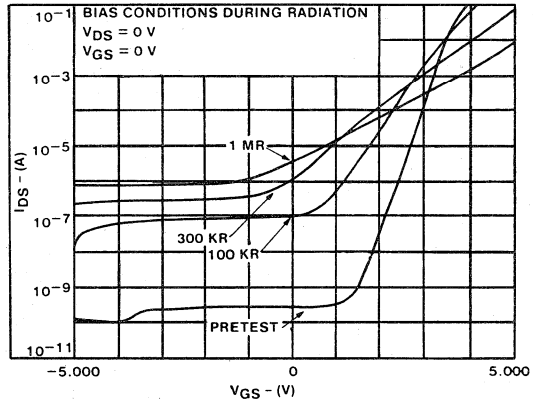

I_{DS} VERSUS V_{GS} AT A FIXED V_{DS} = 5 V

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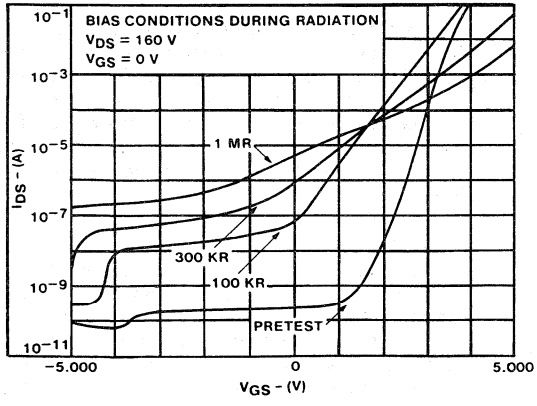

I_{DS} VERSUS V_{GS} AT A FIXED V_{DS} = 5 V

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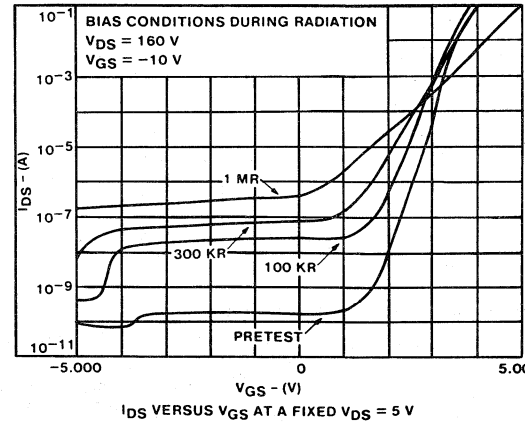


I_{DS} VERSUS V_{GS} AT A FIXED V_{DS} = 5 V

92CS-43408

Fig. 9 Log drain current vs gate voltage of the GRK6766H for five *in situ* bias conditions at various total dose exposures.

Conduction Losses

Conduction losses are expected to increase with total dose as the interface trapped charge builds. An increase in $r_{DS}(on)$ is to be expected, but not a severe change so long as the MOSFET has a sufficiently high gate drive. This condition is well illustrated in Fig. 12.

Transconductance or g_{fs} shows degradation with total dose; however, if the gate drive voltage is sufficient to maintain low conduction losses consistent with the curves of Fig. 12, the performance of switching curcuits is unimpaired.

Switching losses are essentially unchanged with g_{fs} changes provided adequate gate voltage is available to maintain low conduction losses. Generally, the performance of a power-MOSFET drive-circuit appears as a close approximation to a sink current and a source current at the gate during transition with upper and lower compliance-voltage values, rather than that of the commonly measured R_{gen} drive circuit. As a consequence, changes in threshold voltage will not result in a significant change in switching time. Switching times are relatively independent of total dose in a practical drive circuit where voltage compliance values are consistent with low conduction losses and low blocking losses.

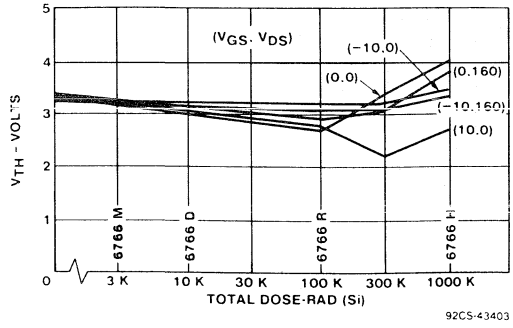


Fig. 10 Threshold voltage at 1mA for the GRK6766H as a function of *in situ* bias and total dose.

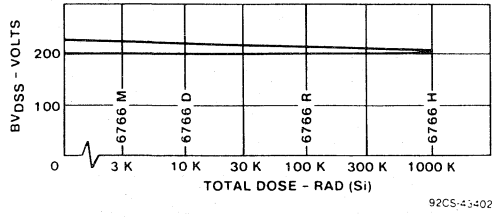


Fig. 11 B_{VDSS} of the GRK6766H as a function of *in situ* bias and total dose.

Dose Rate – Gamma Per Second

Dose rate, prompt gamma, and gamma dot, all terms that describe the quantity of gamma irradiation per unit of time, are expressed in units of rads(Si) per second. A power MOSFET may see a dose rate of several millirads(Si) per second in space, several hundred rads(Si) per second when being tested with Co^{60}, 10^8 rads(Si) when being tested for photocurrent, and 10^{12} rads(Si) when being tested for survival.

Photocurrent

An understanding of the photocurrent in a power MOSFET will help explain dose-rate failures. If a p-n junction is reverse biased and irradiated with 10^9 rads(Si) per second, a current I_{PP} is observed. The unit of choice for I_{PP} is commonly nanoampere second/rads(Si), which becomes nanocoulomb/rads(Si) or nC/rads(Si).

I_{PP} varies with the active p-n junction volume, which is the diode area times the sum of the depletion width and the diffusion length, or the epi thickness if smaller. As a consequence, a given device is much less dependent of applied voltage than approximations neglecting the diffusion length would predict. I_{PP} may be minimized by reducing the device area, reducing the epi thickness, which generally results in a reduced B_{VDSS}, and reducing the minority lifetime. A VDMOS power MOSFET contains a parasitic n-p-n bipolar transistor in which the source of the MOS is also the emitter of the bipolar, the body of the MOS is the base of the bipolar, and the MOS drain is the bipolar collector, as is apparent in Fig. 1. It is the intent in a transistor of this type that the n^+ source and the p-body be shorted or coupled with zero resistance. This goal is accomplished to varying degrees of effectiveness, and is schematically represented in Fig. 13.

If the photocurrent flowing through resistor R produces a 0.7-volt drop, any additional photocurrent becomes multiplied by a factor equal to the current gain of the bipolar. As a consequence, primary and secondary photocurrents are experienced as simple circuit functions, and are not attributable to device physics. This situation is demonstrated in Fig. 14, where the dashed line represents secondary photocurrent. The onset of secondary photocurrent as described in the figure may move to the left or right as temperature is varied or as device layout and processing vary. The secondary photocurrent usually favors a common location from die to die in a given design, a condition that represents a weak link in the design.

In the case of VDMOS power MOSFETs, the parasitic transistor for an n-channel device will have a V_{CEO} approximately one third of B_{VDSS}. A p-channel MOSFET has a parasitic p-n-p transistor that should have a V_{CEO} approximately two thirds of B_{VDSS}. In fact, there are processing conditions that cause the p-n-p V_{CEO} to approximate B_{VDSS}. For the reasons given above, then, the onset of secondary photocurrent will be much more likely to precipitate failure in an n-channel than in a p-channel device at high drain voltages.

Gamma-Dot Failures

Gamma-dot failures of earlier power MOSFETs followed the course of the above discussion. Failures tended to be common about the source pad and occasionally about the gate pad. The causes of these failures were readily corrected. Other device structure and process adjustments are of a proprietary nature and are not discussed in this Note. Some have been applied to the existing Harris GR series of rad-hard power MOSFETs; more will be applied to future types.

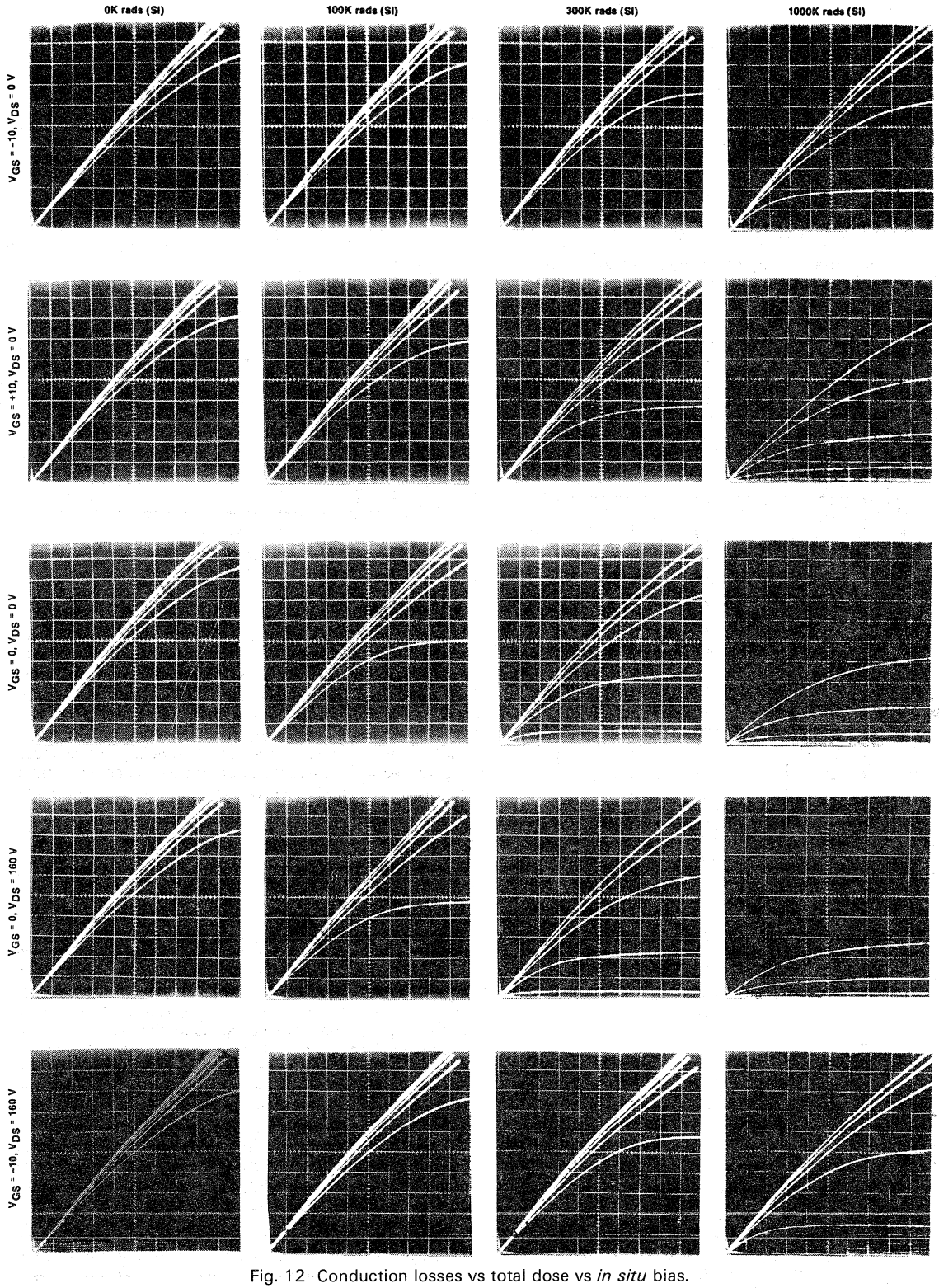


Fig. 12 Conduction losses vs total dose vs *in situ* bias. All photos: I_D = 5A/div., V_{DS} =0.5V/div., V_{GS} = 8, 10, 12, 14, 16V

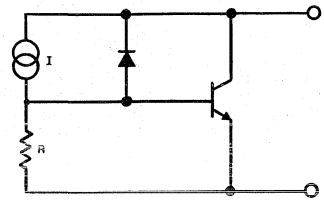


Fig. 13 When the primary photocurrent of the diode, I, produces sufficient IR drop to turn on the bipolar, secondary photocurrent results.

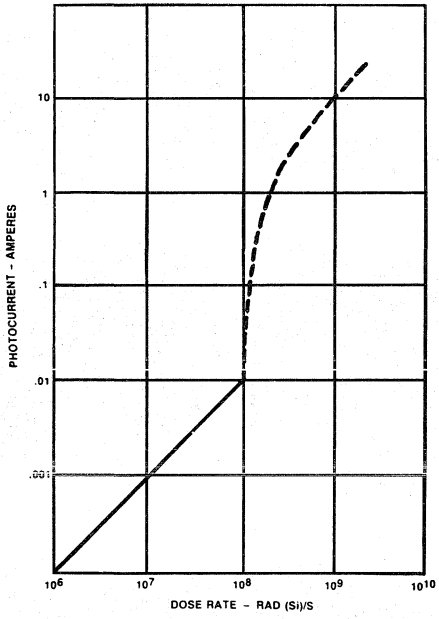


Fig. 14 Response of power device showing arbitrarily chosen onset of secondary photocurrent at 10^8 rads(Si)/s.

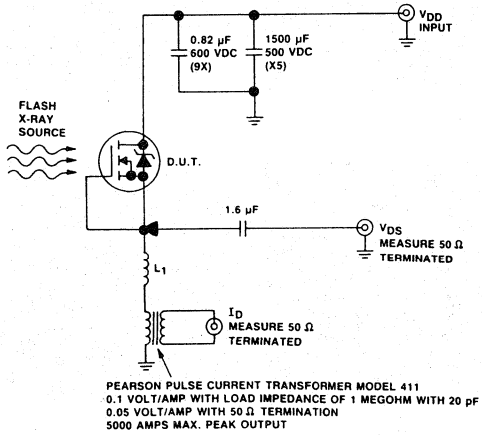


Fig. 15 High-dose-rate (gamma-dot) test circuit.

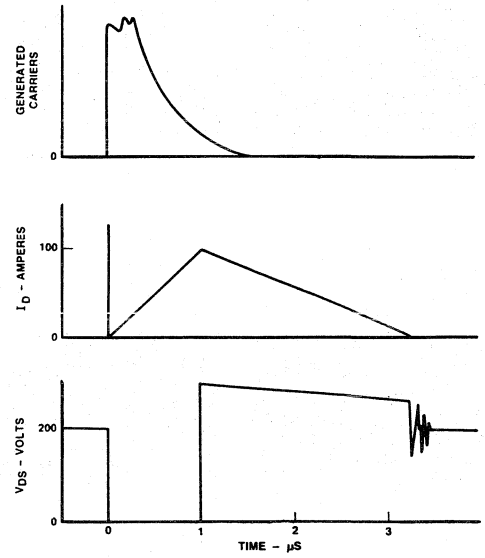


Fig. 16 Idealized power MOSFET waveforms during gamma-dot exposure.

Dose-Rate Testing

Dose-rate testing is very circuit dependent where the level is as high as 1 E12 rads(Si)/s. In order to obtain a dose rate this high, 40 or 50 krads(Si) is applied in 40 nanoseconds. If the drain voltage were maintained at rated B_{VDSS}, the resultant photocurrent density would be of the order of 10^4 amperes per cm^2, assuming that the onset of secondary photocurrent did not occur. Wiring and package inductances exclude testing of this sort for practical devices. But even if it were possible, survival would be unlikely. The testing circuit approach, then, is to control the inductances by defining a readily achievable drain inductor, as shown in Fig. 15. The onus is then placed upon the circuit designer to properly safeguard against failure by limiting circuit currents to those levels permitted in the testing period.

Dose-Rate Waveforms

Dose-rate waveforms are shown in Fig. 16. The prepulse minority carriers are essentially zero, the drain voltage is V_{DD}, and the drain current is zero. At the instant of pulse, hole-electron pairs rise very quickly toward a very large value, drain current increases so as to discharge drain and stray capacitances, and drain voltage rapidly decreases. Before the pulse has ended 40 nanoseconds later, both drain voltage and capacitive displacement current have reached zero, resulting in zero drain current (with the exception of a slight inductor current). The holes and electrons continue to rise to a maximum as the inductor current increases linearly. After the pulse, the number of recombining carriers rapidly decreases as the inductor current continues to rapidly increase.

At the propitious moment, when the carriers (predominately holes) just support the inductor current, the p-n junction (body-drain) receives an inductive "kick," which drives it into avalanche breakdown. The holes rapidly recombine,

and the inductive current is supported totally by avalanche current. When the inductive current is zero, the drain voltage reverts to V_{DD}. Of course there is some ringing associated with the drain and stray capacitances. The transition time for this event is typically 1 or 2 microseconds.

If failure occurs, it will most likely be during the inductive kick, or about two-thirds into the avalanche conduction. This discussion assumes that a moderately hard part was under test.

Single Particle Destruct, SEU

Atoms of many types, stripped of a number of electrons, travel through space with high velocity and high energy. If one collides with a silicon die, it will penetrate to a range determined by the atom's mass and energy. Shedding energy in accordance with its linear energy transfer (LET) factor, it leaves a highly ionized path in several picoseconds, forming a small path of hole-electron pairs. If the strike is at a critical location in a low-voltage logic circuit, and if it occurs at a certain time, the logic will be upset, but little additional damage will result. This problem became known as SEU, single event upset, and methods of analysis became well known. Testing is done with a cyclotron or Van de Graaff generator.

But assumptions valid for logic devices are not always valid for power MOSFETs. If the silicon die is a VDMOS power MOSFET and high drain voltage is present, the problem becomes one of destruction rather than upset. In addition, a large portion of the power MOSFET die is vulnerable to a destructive strike.

If a power MOSFET is placed in a fluence of 10^5 ions per cm^2 when biased at rated B_{VDSS} with the gate at source potential, and if the ions have an LET greater than 30 MeV/mg/cm^2 and a range greater than 30 microns, and the part survives, it is considered hard. This assumes the die surface perpendicular of the ion beam. The energy of the ion beam will typically be several hundred MeV. If the maximum applied drain voltage is derated from B_{VDSS} and all other parameters are maintained constant, MOSFETs of less hardness will withstand a similar fluence.

If the part is sufficiently hard, degrading of the gate may appear as gate-to-source leakage. The condition appears for B_{VDSS} values very much greater than the gate rupture voltage. The defect does not seem to be sufficient to impair normal circuit performance. The gate-damage may be a result of the test method.

Many of the methods used for gamma-dot hardening are effective in combating single-particle destruct (SEU).

Acknowledgments

The author is grateful for the inputs received from many people. Particular thanks are extended to Donald Burke, Donald Burton, and Gary Dolny.

References

1. M.G. Buehler, "Design Curves for Predicting Fast-Neutron-Induced Resistivity Changes in Silicon," Proc. IEEE 56, 1741 (1968).

Thoughts on Radiation Hardness Assurance Sampling and Testing of Harris Rad Hard Power Vertical DMOS MOSFETs

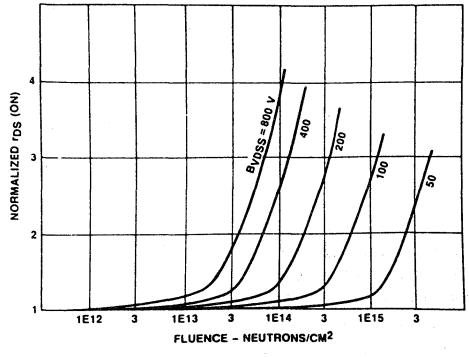
Donald I. Burton and C. Frank Wheatley

Often a customer will require that a sample of a given product lot be tested and the entire lot be rejected if the statistics indicate that the lot percent defective (LTPD) exceeds a chosen level. This is especially true where the test is destructive, and/or quite costly such that 100% testing would be onerous or impossible. In addition to choosing the desired LTPD, a sample size and rejection criteria must be ascertained, thereby providing a confidence level that the desired quality assurance is achieved. As an example a sample size of 22 with no rejects will give a 90% confidence level that the lot has less than a 10% defective content (LTPD x 10). Alternatively, a sample size of 38 with no more than one reject will accomplish the same objective. The sample size increases to 231 and 390 if the LTPD desired is 1. Clearly, low values of LTPD become extremely burdensome for small lots, such that LTPD = 10 is commonly used.

This note will express the authors opinions of when radiation testing of a sample of Harris "second generation" rad hard power MOSFETs is not required, may be required, or is required, based upon their familiarity with the product line, the testing results to date, and the process issues. This guidance is offered as a best effort to respond to many varying radiation criteria, many huge "safety factors," and an inability to discuss technical requirements due to security classification.

Neutron Effects

There are fundamental issues of physics relating to neutron fluence effects upon VDMOS MOSFET's which are not amenable to device design change as discussed in Reference 1. Fig. 5 of that reference is reproduced as Fig. 1 showing the effect of neutron fluence upon the RDS (ON). Although not shown, experimental data exists which closely conforms to Fig. 1, but displaced by a factor of 1.2 higher neutron fluence than shown. If the test criteria fluence level is a factor of three lower than the capability of Fig. 1, sampling is probably not necessary. For a factor of ten below Fig. 1 capability, sampling is not necessary.



Power MOSFET on resistance increases as a function of neutron fluence and breakdown voltage.

Heavy Ions

The section from Reference 1 dealing with heavy ions is reproduced in entirety.

SINGLE PARTICLE DESTRUCT, SEU

Atoms of many types, stripped of a number of electrons, travel through space with high velocity and high energy. If one collides with a silicon die, it will penetrate to a range determined by the atom's mass and energy. Shedding energy in accordance with its linear energy transfer (LET) factor, it leaves a highly ionized path in several pico-seconds, forming a small path of hole-electron pairs. If the strike is at a critical location in a low-voltage logic circuit, and if it occurs at a certain time, the logic will be upset, but little additional damage will result. The problem became known as SEU, single event upset, and methods of analysis became well known. Testing is done with a cyclotron or Van de Graaff generator.

But assumptions valid for logic devices are not always valid for power MOSFETs. If the silicon die is a VDMOS power MOSFET and high drain voltage is present, the problem becomes one of destruction rather than upset. In addition, a large portion of the power MOSFET die is vulnerable to a destructive strike.

If a power MOSFET is placed in a fluence of 10^5 ions per cm^2 when biased at rated BVdss with the gate at source potential and if the ions have an LET greater than 30 MeV/mg/cm^2 and a range greater than 30 microns, and the part survives, it is considered hard. This assumes the die surface perpendicular to the ion beam. The energy of the ion beam will typically be several hundred MeV. If the maximum applied drain voltage is derated from BVdss and all other parameters are maintained constant, MOSFETs of less hardness will withstand a similar fluence.

If the part is sufficiently hard, degrading of the gate may appear as gate-to-source leakage. The condition appears for BVdss values very much greater than the gate rupture voltage. The defect does not seem to be sufficient to impair normal circuit performance. The gate-damage may be a result of the test method.

Many of the methods used for gamma-dot hardening are effective in combating single-particle destruct (SEU).

Measurements have been reported[2] with excellent capability to survive heavy ion bombardment. The "second generation" rad hard Power MOSFET offered by Harris uses a process nearly identical to "process B" of Ref. (2).

Recent measurement[3] (Dec. 1989 and Jan. 1990) demonstrate immunity to single event drain burnout (SEB)

for an LET of 38 or higher when biased at voltages of approximately rated BVdss (both with a zero and a -10 volt gate potential).

Evidence of potential single event gate rupture (SEGR) were observed[3] at the nano-ampere gate leakage level which would not have been observed using the test methods of Ref. (2). It is not known whether circuit malfunction or reliability issues would be indicated from these very low level observations.

The energy used in Ref. (2) and Ref. (3) was 250 to 350 MEV. The resultant range is satisfactory for VDMOS's rated at BVDSS up to 250 volts. Although devices were measured for 500 volt BVdss rating, the range was not sufficient to reach through the active device. As a consequence, the good results of devices rated above 250 volts may not be valid.

If the test criteria for SEB is set at a drain voltage below 80% of rated BVdss with an LET of 35 or less and an ion energy of approximately 300 MEV, sampling is probably not necessary for the second generation rad hard Power MOSFET product. If the drain voltage is set at 50% of rated voltage with an LET of 35 or less and an ion energy of approximately 300 MEV, sampling is not necessary for the second generation rad hard Power MOSFET product.

Total Dose Gamma

The RHAP Power MOSFET devices are guaranteed to meet all pre rad specifications after 10K Rad(Si) and sampling is not necessary. This product is fabricated using the "second generation" rad hard Power MOSFET process.

All other criteria should be sampled. This is an easy thing to do and it is encouraged. Total dose exposure beyond 100K Rad(Si) will generally require post rad specifications slightly different than pre rad. With proper derating, exposures as high as 3000K Rad(Si) are acceptable.

Rebound Effects

Recent observations[4] were made on the 200 volt and 250 volt N channel "second generation" rad hard devices. The 100 volt and 500 volt devices use the same process and are expected to have similar behavior.

Devices were exposed to 300K and 1000K Rad(Si) with biases applied of Vgs = +10, 0, and -10, Vds = 0. Bias was maintained during exposure and annealing except during testing time and an eight week room temperature zero bias period after exposure and prior to the decision to test for rebound. Annealing was done at 100°C with bias, and testing was done at ½, 2, 8, 24, 76, 178, 336, and 504 hours. The following measurements were obtained:

V_{TH} where I_D = 1mA and 10mA; $V_G = V_D$
I_{DON} where V_{GS} = 8, 10, 12 and 14; V_D = 5

Rebound was observed, but was acceptable with high gate drive for 1000K, less pronounced at 300K, and probably could be ignored for most 100K requirements.

If the circuit application has little excess gate drive capability, rebound should be evaluated and specified, particularly for 1000K requirements.

Dose Rate - Gamma Per Second, Prompt Gamma, Gamma-dot

A typical photo current is cited on the data sheet. It is referred to as nano ampere per (Rad(Si) per second) which is dimensionally nC/Rad(Si). If the drain voltage is maintained constant, a plot[1] of photo current vs. dose rate will be linear for increasing dose rate until a parasitic bipolar transistor of the Power MOSFET is biased on. (i.e., If the product of the photo current and the base-emitter shorting resistor of the parasitic bipolar transistor exceeds 0.7 volts, less at high temperatures, the transistor is turned on). This will typically occur for the "second generation" Harris rad hard Power MOSFET at dose rates in excess of 1E10 rad(Si)/sec.

Survival at dose rates below 3E9 for a constant drain voltage up to 80% of rated BVdss probably will not require sampling. (A 100% test is performed at a current level 3 times the rated current (ID1 or IDC) from a 100uH inductor driving the MOSFET into the avalanche mode. The time period is typically tens of micro-seconds). Survival at dose rates equal to or below 1E9 for a constant drain voltage of 80% rated BVdss will not require sampling.

Exposures beyond the above criteria will probably require current limiting, such as an inductor to keep the circuit current below that of the 100% test cited above. If this is done, sampling is probably not required, where assurance is implied by the 100% test.

References

1. Wheatley, C. Frank; "Radiation Hardening of Vertical DMOS (VDMOS) Power MOSFETs; Harris Application Note AN-8831; Oct. 1988.

2. Titus, J. L., Jamiolkowski, L. S. and Wheatley, C. F., "Development of Cosmic Ray Hardened Power MOSFET's". IEEE Trans. Nucl. Sci., NS-36, pp2375-2382. 1989.

3. Titus, J. L., Wheatley, C. F., private communications

4. Macdonald, J.; "Annealing of Harris TA17652 and TA17653 Power MOSFETs" (MEMO #1D52-116), GE SPACE DIVISION, PHILADELPHIA. 4/13/90.

Development of Cosmic Ray Hardened Power MOSFET's

Jeffrey L. Titus
Naval Weapons Support Center
Advanced Technology Division
Building 2087, Code 60541
Crane, IN 47522-5060

Linda S. Jamiolkowski (M)
and
C. Frank Wheatley (SM)
Harris Semiconductor
125 Crestwood Road
Mountaintop, PA 18707-2189

Abstract

Developmental power DMOS (Double-diffused Metal-Oxide Semiconductor) FET's (Field Effect Transistors) were thoroughly characterized in a simulated cosmic ray environment using heavy ions at the Brookhaven National Laboratory's tandem Van de Graaff accelerator facility. The primary failure mode encountered on FET's in this environment was susceptibility to single event burnout. Burnout of the power DMOS FET was catastrophic. Another failure mode was single event gate rupture. Although gate rupture is not as severe as burnout, its long-term effects are not known. Single event gate rupture causes performance degradation due to increased gate leakage current. An increase in current can pose serious problems to applications that cannot compensate for the added performance degradation. Long-term reliability of the gate oxide may be affected resulting in premature device failure. Each failure mode will be discussed. Numerous processing lots were fabricated to experimentally verify that each failure mode could be successfully minimized. Test results have shown that an n-channel, 150-volt DMOS FET was fabricated that survived exposures to ions with LET's up to 80 MeV-cm^2/mg. Finally, hardening approaches will be discussed, including the advantages and disadvantages of each approach on the FET's performance.

Introduction

The effects of a cosmic ray environment on power DMOS FET's were researched and documented extensively. Two failure modes were identified. The main failure mode observed was single event burnout (SEB), which was catastrophic, resulting in drain-to-gate and drain-to-source resistive shorts. The other failure mode observed was single event gate rupture (SEGR), which was detrimental to the device's performance and resulted in an increase of gate and drain leakage currents. Hypothetically, single event burnout is caused by avalanche breakdown of the parasitic NPN bipolar transistor inherent in the MOSFET structure [1-3]. Single event gate rupture was reported to be caused by the internal gate capacitance discharging through the ion track, resulting in high localized joule heating, thus producing a peramanent defect (short) in the dielectric [3]. This research indicated that single event gate rupture is caused when the depletion field which normally isolates the high-voltage drain potential from the gate is locally collapsed by the very high current density associated with the ion track. The permanent defect is felt to be the direct result of joule heating.

In general, power DMOS FET's are desirable devices for space system applications; however, the devices are susceptible to SEB and SEGR. The most commonly used method to safeguard against device burnout was to derate the device's blocking voltage (BVdss), providing a safe margin for operation. A typical derating example would be an application that required devices with a BVdss of 150 volts, but used devices with a BVdss of 300 volts. However, derating the device's blocking voltage resulted in devices with higher on-resistance, total power, and die area than was required. This paper describes a developmental effort to harden a power DMOS FET toward these failures without sacrificing performance.

Processing/Design Techniques

To prevent single event burnout, process and design modifications were directed at reducing the parasitic NPN transistor bipolar effects and suppressing the turn-on of said bipolar. To prevent single event gate rupture, process and design modifications were directed toward reducing the electric fields along the gate oxide interface. However, only those changes that were thought to reduce the probability of a cosmic-ray-induced failure were implemented. Burnout threshold voltage and gate rupture effects were evaluated on devices which had been fabricated with specific changes and, subsequently, were exposed to heavy ions. One design variation implemented to suppress the burnout and gate rupture mechanisms resulted in a major redesign of the typical power DMOS cell and will be designated as the "New Structure" (NS). The layout of that design is not shown.

Experimental Test Samples

Numerous experimental devices incorporating process and design modifications were fabricated to investigate the approaches that were thought to be the most promising for immunity to single event burnout and single event gate rupture without degrading the overall electrical performance. Delidded devices with eighteen different process and/or structure variations were characterized during exposure to heavy ions in an effort to develop a technology capable of manufacturing power DMOS transistors for space applications. The eighteen lots were broken down into five distinct test groups: original test coupon devices, original full-up devices, four-terminal devices, NS test coupon devices, and NS full-up devices.

Original Test Coupon and Full-Up Devices

Representative of the DMOS cross section depicted in Figure 1 are the original test coupon (0.256 cm by 0.256 cm) and full-up (0.436 cm by 0.513 cm) devices. The test coupon devices were scaled-down versions of the full-up devices. That is, the test coupon devices were identical to the full-ups, except the test coupon devices had fewer calls replicated, reducing the overall die area. Process and design variations implemented in these experimental devices included changes in the device's geometric layout (hexagonal and stripe), process parameters, and gate oxide thickness. Experimental devices were fabricated with three process variations: process A, which was a minimal change to the control (expected to improve SEB threshold, but was not expected to totally suppress burnout); process B, which was a more robust change (expected to suppress burnout); and process C, which was a standard process used as a control. The control devices were fabricated with a gate oxide thickness of 1000 angstroms. The other experimental devices were fabricated with a gate oxide thickness of 500 angstroms. The test coupon devices and full-up devices were designed to conduct 1 and 10 amperes, respectively, with a blocking voltage of 150 volts.

Four-Terminal Devices

The four-terminal structure was a redesign of the original transistor cell design in a stripe layout. The fourth terminal was created by separating the p-body and source contact metal forming two isolated contacts. A cross section of the four-terminal structure is shown in Figure 2. Devices were fabricated with two variations in source length: the normal source diffusion length and a source diffusion that was twice the normal length. Actual devices were implemented using process A and process B variations. These devices were intended to provide information concerning the parasitic NPN transistor and its role in burnout. Unfortunately, the four-terminal devices exhibited a higher on-resistance (about ten times as much) than process C devices due to the changes that were implemented in that design. Higher on-resistance could cause premature device failure compared to similar devices with lower on-resistance due to a larger voltage drop across the body region of the MOSFET. Therefore, these devices will only be discussed briefly; and the data will be used to augment the data from the other test structures. The four-terminal devices were designed to

Power DMOS Cross Section
Original (Hexagonal) Structure

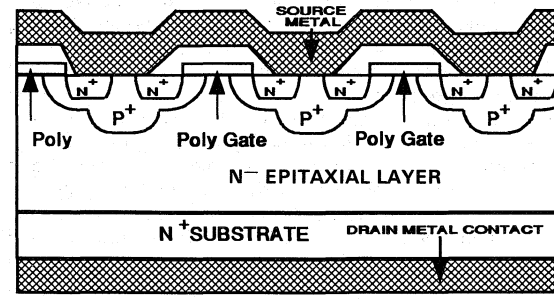


Figure 1.

Power DMOS Cross Section
Four-Terminal Structure

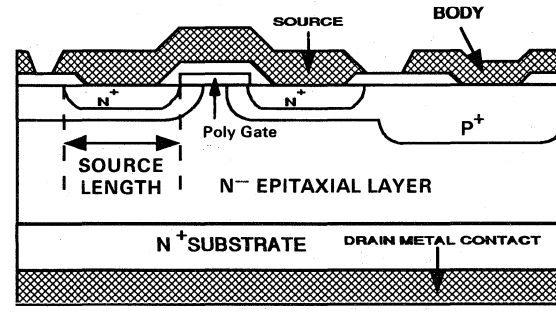


Figure 2.

have electrical characteristics similar to the test coupon devices (conduct 1.0 ampere with a blocking voltage of 150 volts).

NS Test Coupon and Full-Up Devices

The NS test coupon and full-up devices, designed specifically to reduce gate damage, incorporated a total redesign of the power DMOS FET structure. The design and cross section are not shown. Again, the test coupon devices were scaled-down versions of the full-up devices. Process and design variations implemented in these experimental devices were limited to changes in an N+ implant and using two different processes, A and B. Modifications using process A and process B were similar to those used in the more conventional and four-terminal designs that were discussed previously. The N+ implant variation was associated with the NS design. The NS devices were designed to have electrical characteristics similar to the original test coupon and full-up devices (conduct 1 and 10 amperes, respectively, with a blocking voltage of 150 volts).

Test Setup

Single event burnout measurements were performed using a nondestructive test technique, which is shown schematically in Figure 3. The test circuit shown in Figure 3a was only used to monitor burnout, because the resistive gate coupling did not provide the sensitivity necessary to monitor the small increases of gate leakage current. Another potential disadvantage of this circuit was the 50-ohm resistance inserted between the FET's source contact and ground. This impedance was felt to be a potential problem in the measurement of the device's threshold voltage required to induce burnout. The test circuit was modified slightly to alleviate these concerns and to allow in situ measurements, even though no apparent deleterious effects were observed when using this test circuit. The new test circuit is shown schematically in Figure 3b. This design allowed the gate leakage current to be monitored in situ during exposures to mono-energetic ions.

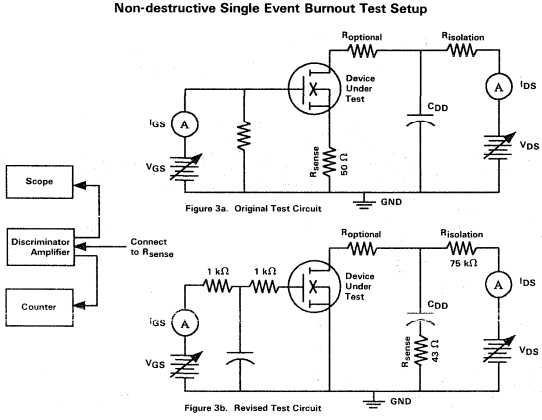


Figure 3.

Both circuits used a stiffening capacitor (C_dd) to support the energy requirements of the DUT, and a sensing resistor (R_sense) was used to monitor and count the actual number of burnout pulses. A discriminator was used to reject low-level noise while passing the signal to the counter, preventing false counts. A resistor (R_optional) was used to limit the available energy to prevent device burnout, allowing an SEB threshold to be determined. The drain and gate power supply currents were monitored in situ to permit early detection of device damage.

Experimental Test Techniques

Twenty-one different device types (eighteen N-channel and three P-channel) were characterized in a simulated cosmic ray environment using heavy ions as the Brookhaven National Laboratory's (BNL) tandem Van de Graaff accelerator facility. Selection of ions and a corresponding energy were chosen to span a linear energy transfer (LET) range between 12 and 80 MeV-cm^2/mg and a penetration depth from 25 to 61 microns. Ion penetration depth was critical to the test measurement and burnout sensitivity of the device. Penetration depth has been shown to be relevant in determining the burnout cross section and drain voltage threshold [1,2]. Ion species selected for this experiment included Chlorine, Nickel, Bromine, Iodine, and Gold. A complete description of each ion is given in Table 1 with necessary penetration depth inferred in Table 3.

Selected Mono-energetic Ions Characteristics

Symbol	Element	Energy (MeV)	LET (MeV-cm^2/mg)	Range (μm)
Au	Gold	328	80	25
I-2	Iodine	307	62	29
I-1	Iodine	281	61	30
Br	Bromine	235	40	30
Ni	Nickel	250	27	40
Cl	Chlorine	220	12	61

Table 1.

All experiments were performed under D.C. bias with the drain voltage set lower than the expected voltage needed to induce device burnout (SEB threshold voltage). The gate voltage was set at either 0 or −10 volts. The gate bias was normally set at 0 volts during burnout characterization to reduce the effects of gate rupture [3]. The device under test was then exposed to a selected ion species until a fluence between 1.0 E+ 05 and 1.0 E+ 06 ions/cm^2 was obtained. After obtaining the desired fluence, the drain voltage was increased by 10 volts and cycle repeated. This test sequence was continued until the drain voltage was within 10 volts of the device's actual breakdown voltage or the calculated burnout cross section, defined as the number of burnout counts divided by the fluence, had saturated (the burnout cross section never dictated the experimental procedure). A few devices were characterized with an applied drain voltage equal to their measured breakdown voltage. Also, a limited amount of data was recorded with the ion beam at angles different from normal (90 degrees with respect to the surface). Most of the test runs were performed with the current limiting resistor (R_optional) to prevent device burnout, however, the burnout threshold voltage was verified by removing this resitor on a few devices and repeating the test sequence until burnout was observed or the test voltage was within a few volts of actual device breakdown.

A total of 624 individual runs were recorded at BNL. From these individual runs, 82 samples were exposed to one or more ion species. A summary of the test results are provided in Table 2. This summary identifies the following key parameters: the actual measured breakdown voltage of each device; the nominal gate oxide thickness; a brief description of the process and design changes; the ion that was selected; the single event burnout threshold voltage or highest voltage successfully tested without burnout; and whether an increase in gate leakage current was observed, indicating possible gate rupture.

Table 2. Summary of SEU Test Results

Device Code	S/N	BVdss	Gate Thickness	Process Mod.	ion Specie	SEB Vth	Gate Damage	Comments
1AA	01	202	500	A	Br	>190	Yes	4-Terminal Test Coupon
1AA	02	204	500	A	Br	110	Yes	(1x) Source Length
1AA	03	218	500	A	Cl	210	No	
1AB	01	249	500	B	Br	>210	Yes	
1AB	02	248	500	B	Br	>240	Yes	
1AB	03	248	500	B	I-1	>240	Yes	
1AB	04	248	500	B	I-1	>240	Yes	
1AC	01	210	500	A	Br	120	Yes	4-Terminal Test Coupon
1AC	02	217	500	A	Br	130	Yes	(2x) Source Length
1AC	03	212	500	A	I-1	100	Yes	
1AC	04	215	500	A	Cl	200	No	
1AD	01	245	500	B	Br	>240	Yes	
1AD	02	244	500	B	Br	>235	Yes	
1AD	03	243	500	B	I-1	>240	Yes	
1AD	04	243	500	B	I-1	>240	Yes	
1AE	01	185	500	A	Br	135	Yes	Original Test Coupon
1AE	03	184	500	A	Br	125	Yes	
1AE	04	195	500	A	Br	130	Yes	
1AE	05	197	500	A	Br	130	Yes	
1AE	06	180	500	A	Cl	>170	No	
1AE	06	180	500	A	Ni	140	No	
1AE	06	180	500	A	Au	110	Yes	
1AE	07	198	500	A	Cl	>170	No	
1AE	10	186	500	A	Ni	150	No	
1AE	16	200	500	A	I-2	95	Yes	
1AE	19	183	500	A	Ni	150	No	
1AE	19	183	500	A	I-2	120	Yes	
1AF	01	220	500	B	Br	>210	Yes	
1AF	03	215	500	B	Br	>210	Yes	
1AF	04	217	500	B	Br	>200	Yes	
1AF	05	203	500	B	Br	>190	Yes	
1AF	06	216	500	B	I-1	>210	Yes	
1AF	07	199	500	B	I-1	>190	Yes	
1AF	08	219	500	B	Cl	>200	No	
1AF	08	219	500	B	Au	>210	Yes	
1AF	08A	217	500	B	I-2	>200	Yes	
1AF	09	199	500	B	Cl	>190	No	
1AF	09A	219	500	B	I-2	>210	Yes	
1AN	61	144	500	A	I-2	90	Yes	(NS) Test Coupon
1AN	65	152	500	A	I-2	85	Yes	No N^+ implant
1AN	67	140	500	A	I-2	90	Yes	
1ANG	01	139	500	A	Br	130	Yes	
1ANG	02	139	500	A	Cl	>130	No	
1ANG	03	152	500	A	Br	<135	Yes	
1ANG	04	140	500	A	Br	120	Yes	
1ANG	07	130	500	A	Br	110	Yes	
1ANG	10	144	500	A	Cl	>130	No	
1AP	15	148	500	B	I-2	>145	Yes	
1AP	15	148	500	B	Au	>145	Yes	
1AP	16	180	500	B	I-2	>175	Yes	
1AP	17	160	500	B	I-2	>155	Yes	
1AP	17	150	500	B	Au	>150	Yes	
1APG	01	155	500	B	Br	>150	Yes	
1APG	02	150	500	B	Br	>145	Yes	
1APG	03	137	500	B	I-1	>130	Yes	

Table 2. Summary of SEU Test Results (Cont.)

Device Code	S/N	BVdss	Gate Thickness	Process Mod.	ion Specie	SEB Vth	Gate Damage	Comments
1APF	02	203	500	B	Br	>200	No	(NS) Test Coupon
1APF	03	200	500	B	I-1	>195	No	N^+ implant
1APF	04	198	500	B	I-1	>195	No	
1APF	05	200	500	B	I-1	>195	No	
1AGP	03	190	500	A	Au	>185	Yes	Original Full-up, P-channel
1AGP	15	189	500	A	Au	>180	Yes	Die Size IV
1AJP	14	150	500	A	Au	>145	Yes	
1AHP	09	174	500	B	Au	>165	Yes	
1AHP	11	170	500	B	Au	>165	Yes	
1AGS	07	183	500	A	Br	145	Yes	Original Full-up, N-channel
1AGS	08	159	500	A	Br	150	Yes	Die Size IV
1AGS	10	149	500	A	Br	>145	Yes	
1AGH	10	173	500	A	Br	120	Yes	
1AH	12	197	500	B	Ni	>190	No	
1AH	12	197	500	B	I-2	>190	Yes	
1AH	12	197	500	B	Au	>190	Yes	
1AH	13	185	500	B	Ni	>170	No	
1AH	13	185	500	B	I-2	>170	Yes	
1AH	13	185	500	B	Au	>180	Yes	
1AH	14	209	500	B	Ni	>200	No	
1AH	14	209	500	B	I-2	>200	Yes	
1AH	14	209	500	B	Au	>200	Yes	
1AQ*	05	180	500	A	I-2	>175	Yes	(NS) Full-up, N-channel
1AQ	05	180	500	A	Au	<175	Yes	N^+ implant
1AQ	16	177	500	A	I-2	>170	Yes	
1AQ	24	201	500	A	Ni	>190	No	
1AQ	24	201	500	A	I-2	180	Yes	
1AQ	24	201	500	A	Au	<195	Yes	
1AR*	12	180	500	B	I-2	>155	Yes	
1AR	12	180	500	B	Au	>160	Yes	
1AR	13	170	500	B	I-2	>165	Yes	
1AR	14	170	500	B	Ni	>165	No	
1AR	14	170	500	B	Au	>165	Yes	
GRM6756H	01	>100	1000	C	Br	80	No	Original Full-up, N-channel
GRM6756H	02	>100	1000	C	Br	80	No	Die Size IV
GRM6756H	03	>100	1000	C	Cl	>100	No	Commercial Rad-Hard
GRM6756H	04	>100	1000	C	Cl	124	No	
GRM6756H	01	>200	1000	C	Br	135	No	
GRM6756H	02	>200	1000	C	Br	130	No	
GRM6756H	03	>200	1000	C	Cl	>200	No	
GRM6756H	04	>200	1000	C	Cl	235	No	
TA9700	10	>300	500	B	I-1	>320	Yes	Original Full-up, N-channel
TA9768	10	>300	500	B	Cl	>320	Yes	Die Size VI
TA9768	19	>300	500	B	I-1	>320	Yes	High-Voltage, Rad-Hard
TA9768	19	>300	500	B	Cl	>320	Yes	
TA9768	37	>300	500	B	I-1	>320	Yes	
TA6768	37	>300	500	B	Cl	>320	Yes	
TA6768	41	>300	500	B	I-1	>320	Yes	
TA6768	41	>300	500	B	Cl	>320	Yes	

* These device are not as good as the test coupon devices as anticipated (Pre-Rad). Test results may be misleading.

Notes: Gate oxide thickness is in Angstroms — Gate Damage refers to gate leakage current.

Test Results and Discussion

The test results revealed that some of the process and design variations were capable of suppressing device burnout. Devices fabricated with these changes were not observed to burn out, demonstrated by a single count, when placed in a simulated cosmic ray environment under worst-case D.C. bias. Devices were biased within 5 to 10 volts of their actual breakdown voltage and subjected to ions with LET's between 12 and 80 MeV-cm^2/mg. No device that used process B burned out, even when the actual breakdown voltage was applied during exposure to ions with LET's between 12 and 80 MeV-cm^2/mg. Also, devices implemented with process A exhibited higher SEB threshold voltages than devices using process C, but not as high as those of process B. This effect was consistent with expectations.

Every experimental device fabricated with a process or design change to suppress SEB indicated some degree of improvement in SEB threshold voltage. The results can be compared to data on similar commercial DMOS transistors that were manufactured by different vendors [1-2]. SEB in commercial devices was induced with an applied drain voltage approximately equal to 50 percent of the device's actual breakdown voltage when exposed to ions with an LET of 30 MeV-cm^2/mg. Test data from our experimental devices exhibited SEB threshold voltages that were between 50 and 100 percent of the device's actual breakdown voltage when exposed to ions with LET's as high as 60 to 80 MeV-cm^2/mg, depending upon the process and design variation implemented.

As previously stated, some experimental devices were not observed to burn out under worst-case bias (maximum drain voltage applied) when exposed to ions with LET's of 80 MeV-cm^2/mg because the burnout failure mechanism was totally suppressed. These robust devices were fabricated using the process and design changes that redistributed the electric fields within the device, reduced the parasitic NPN transistor bipolar effects, or incorporated both techniques. The four-terminal devices, using the same fabrication techniques, did not burn out, either. Additionally, the four-terminal devices indicated that the source length does have an impact on the SEB mechanism, although the improvement in their SEB threshold voltage was minor. A 50 percent decrease in source length translated to a 10-20 percent increase in the SEB threshold. This observation was consistent with similar studies that were previously reported on DMOS devices characterized in a gamma-dot (transient) environment [5].

The experimental NS devices were also characterized in a simulated cosmic ray environment. The test results indicated that this design, which used similar process and design enhancements as the original test structures (previously discussed), suppressed the single event burnout mechanism. The NS design had been implemented to suppress the burnout mechanism, but was further designed to suppress the gate rupture mechanism. To suppress burnout, the NS design reduced the voltage drop across the sensitive region under the source, delaying the turn-on of the parasitic NPN transistor. To suppress gate rupture, the NS design addressed the voltage from the drain that could collapse onto the dielectric during a heavy ion strike. Devices were exposed to heavy ions with LET's between 12 and 61 MeV-cm^2/mg. The NS design exhibited higher SEB threshold voltages than their more conventional design counterparts with similar enhancements (process A).

One NS design variation that used process B with an N+ implant variation showed neither signs of gate rupture damage nor signs of burnout. Experimental lots using this N+ implant yielded full-up devices (process A) that exhibited higher SEB threshold voltages than their NS test coupon counterparts without the N+ implant variation (SEB threshold increased from 63 to 94 percent with respect to the device's breakdown voltage). Two of the three samples using an N+ implant variation exhibited no signs of burnout when exposed to Iodine with an LET of 62 MeV-cm^2/mg.

Improvements in the DMOS performance, when exposed to a cosmic ray environment, are clearly shown using two histogram bar charts (Figure 4). The histogram plots are representative of the experimental devices using process A and process B with several variations in design. The first histogram bar chart (process A) is the average normalized data of the SEB threshold voltage for devices that did exhibit signs of burnout. The other histogram bar chart (process B) is the average normalized data of the maximum test voltage applied for those devices that did not exhibit any signs of burnout. These bar charts only provide data from experimental devices characterized using Bromine and Iodine ions.

SEB Testing Issues

The test data were extremely difficult to obtain, because the geometries of the power DMOS device invalidated the assumption of an effective LET with angles [4]. That is, the depth of the sensitive region was much more than the width and length of the critical surface area (gate area). Under this geometric condition, the effective LET can no longer be computed from the simple relationship of (LET(eff) = LET(norm) x (1/cos θ)). Therefore, to characterize a device adequately, a test sample must undergo several exposures using different ion species that encompassed a wide range of LET(norm) values.

Another issue to consider is the ion penetration depth. Penetration depth is recognized as a serious problem that must be considered in acquiring the data. A cross section of typical layer thicknesses for the DMOS structures similar to those tested are given in Table 3. If the ion can not transverse the sensitive region as defined by the peak electric field in the epitaxial layer, the SEB threshold voltage can be affected. If an ion is used that does not penetrate through this region, the SEB threshold voltage could test optimistically high. Unfortunately, there are only a few facilities that can provide mono-energetic ions with LET's greater than 30 MeV-cm^2/mg with the capability to penetrate this region (range greater than 30-40 microns).

Topological Cross-Section of DMOS Structures
Typical Layer Thicknesses

Layer	Thickness
Possivation Glass	0.5 - 1.0 μm
Source Metal	4.0 - 6.0 μm
Isolation Oxide	0.7 - 1.0 μm
Gate Poly	0.5 - 1.0 μm
Gate Oxide	*0.05 μm
N^+ Source Diffusion	1.2 - 1.5 μm
P^+ Body	5.0 - 8.0 μm
Epitaxial Layer	**15 - 40 μm
Drain Metal	1.5 - 2.0 μm

*Nominal Gate Thickness Provided in Table 2
**Epi varies from 15 μm for 100-volt to 40 μm for 400-volt vertical DMOS

Table 3.

Summary and Conclusions

The data clearly showed that specific process and design changes were capable of suppressing single event burnout in power DMOS transistors. The susceptability of DMOS devices to burnout, given a specific process and design change, was predicted and verified. Devices that were fabricated using minimal process and design enhancements were still susceptible to burnout, but with SEB threshold voltages increased substantially over similar commercial devices. Devices that were fabricated using the more aggressive process and design enhancements were not susceptible to SEB. The only exception to this data was a NS design with an N+ implant variation and minimal process enhancements that did not burn out when exposed to Iodine. One N+ implant variation suppressed SEGR in addition to SEB. Results from the four-terminal devices were similar to those obtained from the other test structures. The test results have shown that reducing the source length does increase the SEB threshold voltage, but the increase was only a minor improvement. Also, the data clearly showed that oxide thickness did affect the degree of gate rupture damage. Thinner (500 angstrom) oxides were more susceptible to gate rupture than the thicker (1000 angstrom) oxides.

The major disadvantage of process A and process B enhancements (excluding NS design) was its negative effect on the device's electrical performance. This technique caused a small but inherent increase in the device's on-resistance. Increases of 20 percent were noted over the standard commercial processes. Although the on-resistance of the NS design was higher than its commercial counterpart (about a 50 percent increase in on-resistance, this difference was attributed to the non-optimized structure. Theoretically, this structure should have an on-resistance, which is less than their commercial counterpart when the design is optimized (given similar die areas). The NS design can be used to suppress SEB and SEGR. This was successfully demonstrated by the fabrication of a power DMOS FET that was immune to SEB and SEGR when exposed to mono-energetic ions.

The enhancements to the conventional structure are manufacturable. The ability to mass produce the NS structure is not yet assured.

Acknowledgements

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Test Result Summary of Experimental Processes

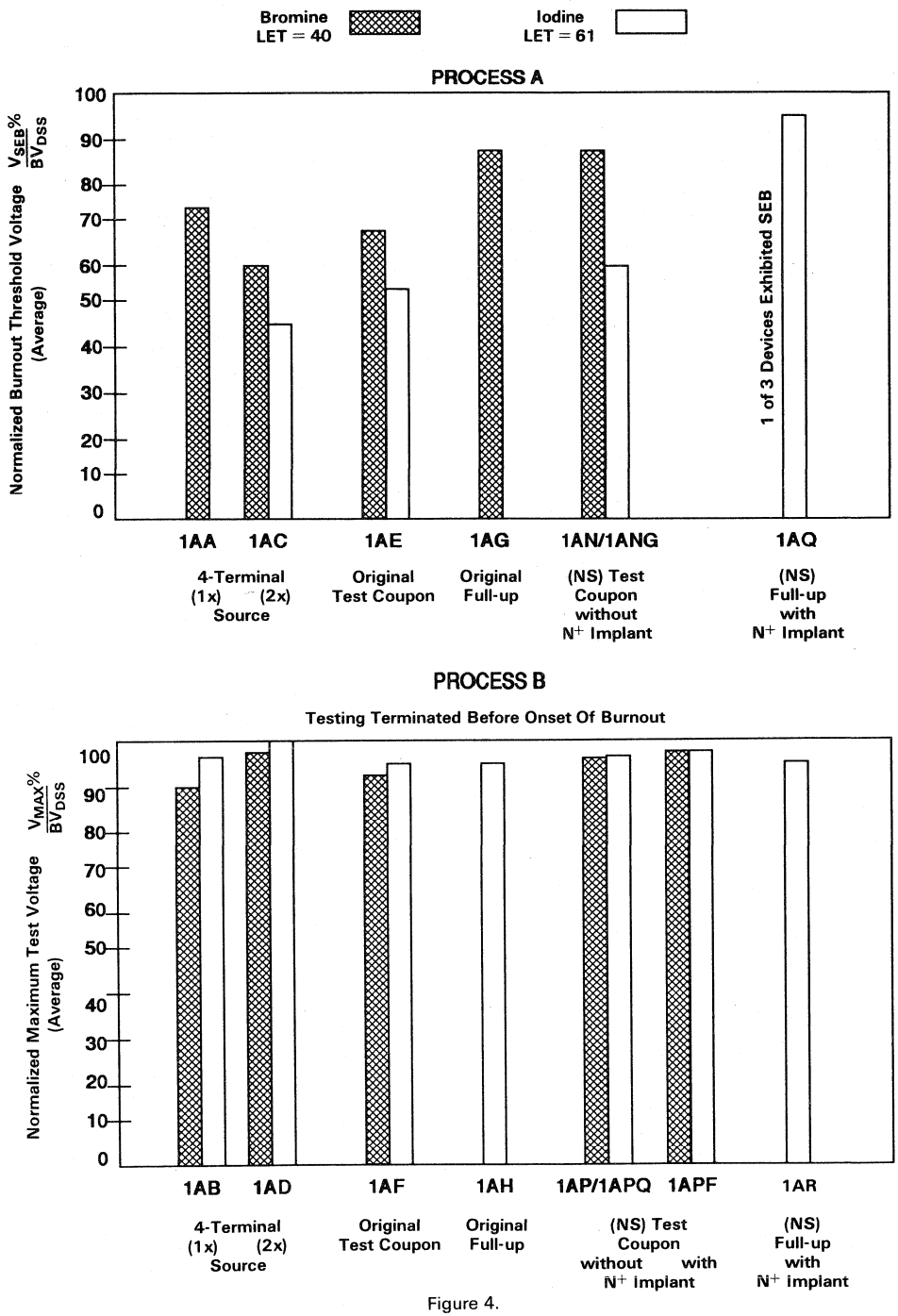


Figure 4.

RAD-HARD 14

QUALITY AND RELIABILITY

Quality and Reliability

Introduction

The needs of the military and aerospace community for a wide variety of specialized, hi-rel microcircuits are filled by the Harris Military and Aerospace Division. These circuits are typically manufactured to Mil-M-38510 and Mil-Std-883, as well as to unique customer requirements. In all cases, Harris is committed to continue its tradition of supplying only the highest quality devices for hi-rel applications.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force — from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. This group facilitates the development of Statistical Process Control (SPC) and Design of Experiments (DOX) programs and works with manufacturing to establish control charts. In addition, Quality professionals are involved in the measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

"Total Quality" at Harris requires ownership and responsibility by each person at every level of the organization. At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures in other organizations — through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs — with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress. (See Figure 3 and Table 4.)

The Improvement Process

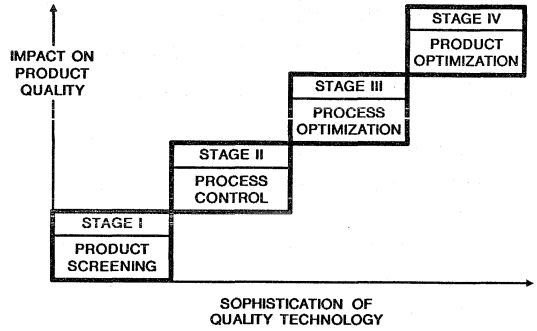


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage II to Stage III, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	– Room/Hood Particulates	X	X
	– Temperature/Humidity	X	X
	– Water Quality		X
	• Product		
	– Junction Depth	X	
	– Sheet Resistivities	X	
	– Defect Density	X	X
	– Critical Dimensions	X	X
	– Visual Inspection	X	X
	– Lot Acceptance		X
	• Process		
	– Film Thickness	X	X
	– Implant Dosages	X	
	– Capacitance Voltage Changes	X	X
	– Conformance to Specification	X	X
	• Equipment		
	– Repeatability	X	X
	– Profiles	X	X
	– Calibration		X
	– Preventive Maintenance	X	X
Assembly	• JAN Self-Audit		X
	• Environmental		
	– Room/Hood Particulates	X	X
	– Temperature/Humidity	X	X
	– Water Quality		X
	• Product		
	– Documentation Check		X
	– Dice Inspection	X	X
	– Wire Bond Pull Strength/Controls	X	X
	– Die Sear Controls		X
	– Pre-Seal Visual	X	X
	– Fine/Gross Leak	X	X
	– PIND Test	X	
	– Lead Finish Visuals, Thickness	X	X
	– Die Shear		X
	– Solderability		X
	• Process		
	– Operator Quality Performance	X	X
	– Saw Controls	X	
	– Die Attach Temperatures	X	X
	– Seal Parameters	X	
	– Seal Temperature Profile	X	X
	– Sta-Bake Profile	X	
	– Temp Cycle Chamber Temperature	X	X
	– ESD Protection	X	X
	– Plating Bath Controls	X	
	– Mold Parameters	X	X
Test	• JAN Self-Audit		X
	• Temperature/Humidity	X	X
	• ESD Controls	X	
	• Temperature Test Calibration	X	
	• Test System Calibration	X	
	• Test Procedures		X
	• Control Unit Compliance	X	
	• Lot Acceptance Conformance	X	
	• Group A Lot Acceptance		X
Probe	• JAN Self-Audit		X
	• Wafer Repeat Correlation	X	
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (CONTINUED)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Burn-In	• JAN Self-Audit		X
	• Functionality Board Check	X	
	• Oven Temperature Controls	X	
	• Procedural Conformance		X
Brand	• JAN Self-Audit		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	X
	• Procedural Conformance		X
QCI Inspection	• JAN Self-Audit		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment.

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

Harris Semiconductor Standard Process Flows

Harris Semiconductor offers a variety of Mil-Std-883 compliant and non-compliant standard screening flows for cost-effective support of the customer's specific testing and reliability requirements. These flows include environmental stress testing, burn-in and electrical testing at room, high and low temperatures. The flows shown on pages 14-32 to 14-40 indicate the Harris Standard Screening processes. The Mil-Std-883/JAN Quality Conformance Inspections are shown on pages 14-5 to 14-12. In addition, Harris can supply products tested to customer specifications for both electrical requirements and non-standard environmental stress screening. Consult your field sales representative for details.

TABLE 2. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

TABLE I. *MIL-STD-883/JAN* QUALITY CONFORMANCE INSPECTIONS
GROUP A ELECTRICAL TESTS FOR CLASSES S AND B DEVICES
(NOTE 1)

SUBGROUPS (NOTE 2) QUALITY/ACCEPT NO. = 116/0 (NOTES 3, 4, 5)	
Subgroup 1	Static tests at +25°C
Subgroup 2	Static tests at maximum rated operating temperature
Subgroup 3	Static tests at minimum rated operating temperature
Subgroup 4	Dynamic tests at +25°C
Subgroup 5	Dynamic tests at maximum rated operating temperature
Subgroup 6	Dynamic tests at maximum rated operating temperature
Subgroup 7	Functional tests at +25°C
Subgroup 8A	Dynamic tests at maximum rated operating temperature
Subgroup 8B	Dynamic tests at minimum rated operating temperature
Subgroup 9	Switching tests at +25°C
Subgroup 10	Switching tests at maximum rated operating temperature
Subgroup 11	Switching tests at minimum rated operating temperature

NOTES:

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2. At the manufacturer's option, the applicable tests required for group A testing (see Note 1) may be conducted individually or combined into sets of tests, subgroups (as defined in Table 1), or sets of subgroups. However, the manufacturer shall predesignate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.

3. The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in Note 2, shall be 116/0.

4. A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

5. If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicalbe. For class S only, if this testing results in a percent defective greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent devective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

TABLE IIA. *MIL-STD-883/JAN* QUALITY CONFORMANCE INSPECTIONS
***GROUP B* TESTS FOR CLASS S DEVICES (NOTE 1)**

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY/ (ACCEPT NO.) OR LTPD
SUBGROUP 1			
A. Physical dimensions (Note 2) B. Internal water-vapor content (Notes 2, 3)	2016 1018	 5,000 ppm maximum water content at +100°C	2(0) 3(0) or 5(1) (Note 4)
SUBGROUP 2 (Note 5)			
A. Resistance to solvents B. Internal visual and mechanical C. Bond Strength 1. Thermo compression 2. Ultrasonic 3. Flip-chip 4. Beam lead D. Die shear test	2015 2013, 2014 2011	 Failure criteria from design and construction requirements of applicable acquisition document 1. Test condition C or D 2. Test condition C or D 3. Test condition F 4. Test condition H In accordance with Method 2019 for the applicable die size	4(0) 2(0) LTPD = 10 (Note 6) 3(0)
SUBGROUP 3			
Solderability (Note 7)	2003 or 2022	Soldering temperature of 245°C ± 5°C	LTPD = 10
SUBGROUP 4 (Note 2)			
A. Lead integrity (Note 8) B. Seal a. Fine b. Gross C. Lid torque (Note 9)	2004 1014 2024	Test condition B_2, lead fatigue As applicable As applicable	2(0)
SUBGROUP 5 (Note 10)			
A. End-point electrical parameters (Notes 11, 12) B. Steady state life (Note 13) C. End-point electrical parameter (Note 11)	 1005	As specified in the applicable device specification Test condition C, D or E As specified in the applicable device specification	 LTPD = 5
SUBGROUP 6			
A. End-point electrical parameters B. Temperature cycling C. Constant acceleration D. Seal a. Fine b. Gross E. End-point electrical parameters	 1010 2001 1014	As specified in the applicable device specification Condition C, 100 cycles minimum Test condition E: Y_1 orientation only As specified in the applicable device specification	LTPD = 15
SUBGROUP 7 (Note 14)			
A. Electrical parameters B. Electrostatic discharge sensitivity C. Electrical parameters	 3015	Group A, and delta limits in accordance with method 3015 Group A, and delta limits in accordance with method 3015	3(0) with repeat for cumulative effects 15(0)

See Notes Next Page

NOTES:

1. Post burn-in electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
2. Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot.
3. This test is required only if it is a glass-frit-sealed package. Unless handling precautions for beryllia packages are available and followed method 1018, procedure 3 shall be used. See Note 6 of Table 4.
4. Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., 3 or 5 devices) fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions are submitted to the qualifying activity along with five additional devices from the same lot.
5. Resistance to solvents testing required only on devices using inks or paints as a marking medium.
6. Unless otherwise specified, the LTPD sample size for conditions C and D is the number of bond pulls selected from a minimum number of four devices, and for condition F or H is the number of dice (not bonds).
7. All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.
8. For leadless chip carrier packages only, use test condition D. For pin grid array leads and rigid leads use method 2028.
9. Lid torque test shall apply only to glass-frit-sealed packages.
10. The alternate removal-of-bias provisions of 3.3.1 of method 1005 shall not apply for test temperatures above 125°C.
11. Read and record group A subgroups 1, 2 and 3.
12. For qualification, read and record data for all group A subgroups satisfies the data requirement of Mil-M-38510, 4.4.2.1.6A.
13. The same test temperature that was used for burn-in shall be used for the steady-state life test.
14. Unless otherwise specified, test shall be performed for initial qualification and product redesign as a minimum.

TABLE IIB. *MIL-STD-883/JAN* QUALITY CONFORMANCE INSPECTIONS
***GROUP B* TESTS FOR CLASS B DEVICES** (NOTES 1, 2)

TEST	MIL-STD-883		QUANTITY/ (ACCEPT NO.) OR LTPD
	METHOD	CONDITION	
SUBGROUP 2 (Note 3)			
A. Resistance to solvents	2015		4(0)
SUBGROUP 3			
A. Solderability (Note 4)	2022 or 2003	Soldering temperatures of 245°C ± 5°C	10
SUBGROUP 5			
A. Bond Strength (Note 5) 1. Thermocompression 2. Ultrasonic or wedge 3. Flip-chip 4. Beam lead	2011	 1. Test condition C or D 2. Test condition C or D 3. Test condition F 4. Test condition H	15

NOTES:

1. Post burn-in electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
2. Subgroups 1, 4, 6, 7 and 8 have been deleted from this table. For convenience, the remaining subgroups will not be renumbered.
3. Resistance to solvents testing required only on devices using inks or paints as the marking or contrast medium.
4. All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure to burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.
5. Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see method 2011).

TABLE III. *MIL-STD-883/JAN* QUALITY CONFORMANCE INSPECTIONS
GROUP C DIE-RELATED TESTS FOR CLASS B ONLY

TEST	MIL-STD-883		QUANTITY/ (ACCEPT NO.) OR LTPD
	METHOD	CONDITION	
SUBGROUP 1			
A. Steady-state life test B. End point electrical parameters	1005	Test condition to be specified (1,000 hours at 125°C) As specified in the applicable device specification	5

TABLE IV. *MIL-STD-883/JAN* QUALITY CONFORMANCE INSPECTIONS
***GROUP D* PACKAGE RELATED TESTS FOR ALL CLASSES**

(NOTE 1) TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY/ (ACCEPT NO.) OR LTPD
SUBGROUP 1 (Note 2)			
A. Physical dimensions	2016		15
SUBGROUP 2 (Note 2)			
A. Lead integrity (Note 3) B. Seal (Note 4) 1. Fine 2. Gross	2004 1014	Test condition B_2 (lead fatigue) As applicable	15
SUBGROUP 3 (Note 5)			
A. Thermal shock B. Temperature cycling C. Moisture resistance (Note 6) D. Seal 1. Fine 2. Gross E. Visual examination F. End-point electrical parameters (Note 7)	1011 1010 1004 1014 	Test condition B as a minimum, 15 cycles minimum Test condition C, 100 cycles minimum As applicable In accordance with visual criteria of method 1004 and 1010 As specified in the applicable device specification	15
SUBGROUP 4 (Note 5)			
A. Mechanical shock B. Vibration, variable frequency C. Constant acceleration D. Seal 1. Fine 2. Gross E. Visual examination F. End-point electrical parameters	2002 2007 2001 1014 Note 8 	Test condition B minimum Test condition A minimum Test condition E minimum (see 3), Y_1 orientation only As applicable As specified in the applicable device specification	15
SUBGROUP 5 (Note 2)			
A. Salt atmosphere (Note 6) B. Seal 1. Fine 2. Gross C. Visual examination	1009 1014 	Test condition A minimum As applicable In accordance with visual criteria of method 1009	15(0)
SUBGROUP 6 (Note 2)			
A. Internal water-vapor content	1018	5,000 ppm maximum water content at 100°C	3(0) or 5(1) (Note 9)
SUBGROUP 7 (Note 2)			
A. Adhesion of lead finish (Notes 10, 11)	2025		15(0)
SUBGROUP 8			
A. Lid torque (Notes 2, 12)	2024		5(0)

See Notes Next Page

NOTES:

1. In-line monitor data may be substituted for subgroups D1, D2, D6, D7 and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. This in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.
2. Electrical reject devices from that same inspection lot may be used for samples.
3. For leadless chip carrier packages only, use test condition D. For pin grid array and other rigid leads use method 2028.
4. Seal test (subgroup 2B) need be performed only on packages having leads exiting through a glass seal.
5. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
6. Lead bend stress initial conditioning is not required for leadless chip carrier packages.
7. At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.
8. Visual examination shall be in accordance with method 1010 or 1011.
9. Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions are submitted to the qualifying activity along with 5 additional devices from the same lot.
10. The adhesion of lead finish test shall not apply for leadless chip carrier packages.
11. Quantity/(accept number) based on number of leads.
12. Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., wherever frit seal establishes hermiticity or package integrity).

TABLE V. *MIL-STD-883/JAN* QUALITY CONFORMANCE INSPECTIONS
***GROUP E* RADIATION HARDNESS ASSURANCE TESTS** (NOTE 1)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	CLASS S QUANTITY/ (ACCEPT NUMBER)	CLASS S NOTES	CLASS B QUANTITY/ (ACCEPT NUMBER)	CLASS B NOTES
SUBGROUP 1 (Note 2)						
Neutron irradiation A. Qualification B. QCI Endpoint electrical parameters	1017	25°C As specified in accordance with detail specification	 A. 11(0) B. 11(0)	 3 3	 A. 11(0) B. 11(0)	 4 4
SUBGROUP 2 (Note 5)						
Steady-state total dose irradiation A. Qualification B. QCI Endpoint electrical parameters	1019	25°C Maximum supply voltage As specified in accordance with detail specification	 A. 4(0) 2(0) B. 4(0) 2(0)	 A. 6 8 B. 6 8	 A. 22(0) B. 22(0)	 7 7
SUBGROUP 3 (Note 9)						
Transient ionizing irradiation Endpoint electrical	1021 1023	25°C 25°C As specified in accordance with detail specification	11(0)	3	11(0)	4

NOTES:

1. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method. Group E tests may be performed prior to device screening (see 3.5.3).
2. Waive neutron tests for MOS devices except for charge coupled devices or where, by design, bipolar elements are an integral part of the device function.
3. In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
4. In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
5. Class B devices shall be inspected using either the class B quantity/accept number criteria as specified, or by using the class S criteria on each wafer.
6. In accordance with wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius, and spaced uniformly around this radius.
7. In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).
8. In accordance with wafer for device types with greater than 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.
9. Upset testing during qualification on first QCI shall be conducted when specified in purchase order or contract. When specified, the same microcircuits may be tested in more than one subgroup.

TABLE III. GROUP A INSPECTION (NOTE 1)

SUBGROUPS	JANS SAMPLING PLAN (N/C)	JAN, JANTX, JANTXV SAMPLING PLAN
SUBGROUP 1 (PPM-3)		
Visual and mechanical inspection (Note 2) (Mil-Std-750, method 2071)	15 devices c = 0	LTPD = 5 (Note 3)
SUBGROUP 2 (PPM-2)		
DC (static) tests at 25°C	116 devices c = 0 (Notes 4, 5)	116 devices (Note 4) c = 0
SUBGROUP 3 (PPM-2)		
DC (static) tests at maximum rated and minimum rated operating temperatures	116 devices c = 0 (Notes 4, 5)	116 devices (Note 4) c = 0
SUBGROUP 4 (PPM-2)		
Dynamic tests at 25°C	116 devices c = 0 (Notes 4, 5)	116 devices (Note 4) c = 0
SUBGROUP 5		
Safe operating area test (for power transistors only): a. DC b. Clamped inductive c. Unclamped inductive End-point electrical measurement	LTPD = 10 (Notes 3, 6)	LTPD = 5 (Note 3)
SUBGROUP 6 (Note 7)		
Surge current (for diodes/rectifiers only) End-point electrical measurements	LTPD = 10 (Notes 3, 6)	LTPD = 10 (Note 3)
SUBGROUP 7		
Selected static and dynamic tests	LTPD = 10 (Notes 3, 6)	LTPD = 10 (Note 3)

NOTES:

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable associated detail specification. Where no parameters have been specified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements. A single sample may be used for all subgroup testing. These tests are considered nondestructive and devices may be shipped.
2. PPM-3 applies only to mechanical inspection.
3. For these subgroups, the maximum accept number (c) shall be two.
4. If a device in the sample fails one or more test(s) in the subgroup or subgroups being sampled, each device in the (sub) lot represented by the sample may be screened for the test(s) for which the sample failed. Alternatively, an engineering evaluation shall be performed to determine an appropriate 25°C electrical screen(s) necessary to remove the failure mode. A second sample shall be tested to the failed subgroup. If the second sample fails, the same subgroup 100 percent rescreen of the failed subgroup shall be performed or the lot shall be rejected.
5. All devices required by the specified LTPD shall be subjected to subgroups 2, 3 and 4 combined.
6. All devices required by the specified LTPD shall be randomly selected from the devices subjected to subgroups 2, 3 and 4, and shall be subjected to subgroups 5, 6 and 7 combined.
7. Not applicable when performed as a 100 percent screen.

TABLE IVA. GROUP B INSPECTIONS FOR JANS DEVICES

INSPECTIONS	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	QUALIFICATION AND LARGE LOT QUALITY CONFORMANCE INSPECTION SAMPLING PLAN	SMALL LOT QUALITY CONFORMANCE INSPECTION N/C
SUBGROUP 1 (Note 1)				
Physical dimensions	2066	Dimensions per case outline specified	10	8 devices c = 0
SUBGROUP 2 (Note 1)				
Solderability	2026	Separate samples may be used for each test. The LTPD applies to the number of leads inspected. A minimum of 3 devices shall be tested	15	6 devices c = 0
Resistance to solvents	1022			
SUBGROUP 3				
Temperature cycling (air-to-air)	1051	No dwell is required at 25°C. Test condition C3, (100 cycles) except step 3 at 175°C + 5° - 0°C for t(extreme) ≥ 10 min.	10	6 devices c = 0
Surge (Note 2)	4066	As specified		
Hermetic seal	1071			
a. Fine		Not required for double plug diodes. Test condition G or H, max leak rate = 5×10^{-8} atm cc/s, except 5×10^{-7} atm cc/s for devices with internal cavity > 0.3 cc		
b. Gross				
Electrical measurements		As specified		
Decap-internal visual (design verification) (Note 3)	2075	Visual criteria in accordance with qualified design and internal visual precap criteria	6 devices c = 0	
SEM (when specified)	2077		6 devices c = 0	
Bond strength (wire or clip bonded devices only)	2037	The sampling plan applies to the number of wires pulled. The sample shall include a minimum of 3 devices and shall include all wire sizes		6 devices c = 0
Die shear (excluding axial leaded devices)	2017	Only devices previously subjected to the bond strength test shall be used for this test		
SUBGROUP 4				
Intermittent operation life	1037	2,000 cycles, as specified	10	8 devices c = 0
Electrical measurements	1042	Condition D Thermal response and other electrical measurements as specified		
Thermal shock (liquid-to-liquid) (For axial lead glass diodes only)	1056	25 cycles condition A		

TABLE IVA. GROUP B INSPECTIONS FOR JANS DEVICES (CONTINUED)

INSPECTIONS	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	QUALIFICATION AND LARGE LOT QUALITY CONFORMANCE INSPECTION SAMPLING PLAN	SMALL LOT QUALITY CONFORMANCE INSPECTION N/C
SUBGROUP 5				
Accelerated steady-state operation life		Bias conditions as specified	10	12 devices c = 0
	1027	Eutectic die attached semiconductors: T_J = 275°C min (for 96 hours min)		
	1027	Soft solder die attached power semiconductors: T_J = 225°C min (for 168 hours min) For Schottky diodes: T_J = 175°C min (for 240 hours min)		
	1042	Power MOSFETs: T_J = 200°C min (for 120 hours min); condition C; (see 4.6.4)		
Electrical measurements		Thermal response and other electrical measurements as specified		
Bond strength (Al-Au interconnects only)	2037	As specified. Bond strength samples shall have passed accelerated steady-state operation life	LTPD = 10, c = 0	LTPD = 10, c = 0
SUBGROUP 6				
Thermal resistance		As specified	10	8 devices c = 0
Diodes	3101			
Transistors (bipolar)	3131			
Transistors (POWERFETs)	3161			
Thyristors	3181			
IGBT	3103			
GaAs	3104			

NOTES:

1. Electrical reject devices (and X-Ray for JANS) and PIND rejects from the same inspection lot may be used for all subgroups when electrical end-point measurements are not required. Post burn-in electrical rejects may be used.
2. Surge shall be performed on rectifiers and reverse surge for transient suppressors.
3. For axial lead diodes a lead pull to destruction shall be performed.

TABLE IVB. GROUP B INSPECTIONS FOR JAN, JANTX AND JANTXV DEVICES

INSPECTIONS	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	SAMPLING PLAN	SMALL LOT QUALITY CONFORMANCE INSPECTION N/C
SUBGROUP 1 (Note 1)				
Solderability	2026	Separate samples may be used for each test. The sampling plan applies to the number of leads inspected. A minimum of 3 devices shall be tested.	15	4 devices c = 0
Resistance to solvents	1022			
SUBGROUP 2				
Temperature cycling (air-to-air) except for axial lead glass diode	1051	No dwell is required at 25°C. Test condition C, except step 3 at 175°C +5°C, -0°C, (45 cycles including screening, t(extreme) > 10 min	10	6 devices c = 0
Thermal shock (liquid-to-liquid) (for axial lead glass diodes only)	1056	10 cycles, condition A		
Surge (Note 2)	4066	As specified		
Hermetic seal				
a. Fine leak	1071	Not required for double plug diode. Test condition G or H, max leak rate = 5×10^{-8} atm cc/s, except 5×10^{-7} atm cc/s for devices with internal cavity > 0.3 cc		
b. Gross leak				
Electrical measurements		As specified		
SUBGROUP 3 (Note 3)				
		A separate sample may be used for each test. 340 hours min	5	12 devices c = 0
Steady-state operation life or intermittent operation life (Note 4)	1027 1037 1042	Bias conditions as specified Condition D, 2,000 cycles		
Electrical measurements		As specified		
Bond strength (wire or clip bonded devices only) (Rectifiers only)	2037	The sample shall include a minimum of 3 devices and shall include all wire sizes	10 (c = 1)	LTPD = 10 (c = 1)
Steady-state DC blocking life	1048	340 hours (as specified)	5	12 devices c = 0
Electrical measurements		As specified		
Bond strength (wire or clip bonded devices only)	2037	The sample shall include a minimum of 3 devices and shall include all wire sizes	10 c = 1	LTPD = 10, c = 1
SUBGROUP 4 (Notes 1, 5)				
Decap internal visual (design verification)	2075	Visual criteria in accordance with qualified design	1 device c = 0	1 device c = 0
SEM (when specified)	2077		6 devices c = 0	6 devices c = 0
SUBGROUP 5				
Thermal resistance:		Thermal resistance may be performed on group E frequency whenever 100 percent thermal response is performed. As specified	15	6 devices c = 0
Diodes	3101			
Transistors (Bipolar)	3131			
Transistors (POWERFETs)	3161			
Thyristors	3181			
IGBT	3103			
GaAs	3104			

See Notes Next Page

TABLE IVB. GROUP B INSPECTIONS FOR JAN, JANTX AND JANTXV DEVICES (CONTINUED)

INSPECTIONS	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	SAMPLING PLAN	SMALL LOT QUALITY CONFORMANCE INSPECTION N/C
SUBGROUP 6				
High-temp life (Nonoperating)	1032	340 hours min, $T_{STG\ (max)} = T_A$	7	12 devices c = 0
Electrical measurements		As specified		
SUBGROUP 7 (Note 6)				
Constant acceleration	2006	1 minute min in each orientation, X1, Y1 and Z1 at 20,000 G min, except at 10,000 G min for devices with power rating of ≥ 10 watts. $T_C = 25^oC$	10	6 devices c = 0
Particle impact noise detection	2052	Condition A (see 4.3.4.2.1)		
Electrical measurements		As specified		

NOTES:

1. Electrical reject devices (and X-Ray for JANS) and PIND rejects from the same inspection lot may be used for all subgroups when electrical end-point measurements are not required. Post burn-in electrical rejects may be used.
2. Surge shall be performed on rectifiers and reverse surge for transient suppressors.
3. If a given inspection lot undergoing group B inspection has been selected to satisfy group C inspection requirements, the 340-hour or 2,000 cycle life tests may be continued on test to 1,000 hours or 6,000 cycles, as applicable, in order to satisfy the group C life test requirements and bond pull may be performed after group C life test. In such cases, either the 340-hour or 2,000 cycle, as applicable, end-point measurements.
4. Intermittent operation life shall be performed on all case mounted devices.
5. For axial lead diodes a lead pull to destruction shall be performed.
6. Not applicable to any devices with external and internal pressure contacts (die to electrical contacts), optical coupled isolators, double plug diodes. Subgroup 7 is applicable to JANTX and JANTXV only.

TABLE V. GROUP C PERIODIC INSPECTIONS (ALL QUALITY LEVELS)

INSPECTIONS	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	SAMPLING PLAN	SMALL LOT QUALITY CONFORMANCE INSPECTION N/C
SUBGROUP 1				
Physical dimensions (Note 1)	2066	Dimensions per case outline specified	15	6 devices c = 0
SUBGROUP 2				
Thermal shock (glass strain)	1056	Test condition A, except test condition B for devices with power rating of > 5 watts at $T_C = 25^oC$	10	6 devices c = 0
Terminal Strength	2036	As specified		
Hermetic seal a. Fine leak	1071	Not required for double plug diodes. Test condition G or H, max, leak rate = 5×10^{-8} atm cc/s, except 5×10^{-7} atm cc/s for devices with internal cavity > 0.3 cc		
b. Gross leak				
Moisture resistance	1021	Omit initial conditioning		
Electrical measurements		As specified		
SUBGROUP 3				
		Not required for disc packages. Nonoperating, 1500 G's, 0.5ms		
Shock	2016	5 blows in each orientation: X1, Y1 and Z1. (Y1 only for axial glass diodes)	10	6 devices c = 0
Vibration, variable frequency	2056			
~~Constant acceleration (see~~ 4.6) (not required when performed in group B)	~~2006~~	1 minute min in each orientation, X1, Y1 and Z1 at 20,000 G min, except at 10,000 G min for devices with power rating of ≥ 10 watts. $T_C = 25^oC$		
Electrical measurements		As specified		
SUBGROUP 4				
Salt atmosphere (corrosion) (Note 1)	1041		15	6 devices c = 0
SUBGROUP 5				
Not applicable				
SUBGROUP 6 (Notes 2, 3)				
		Not required for disc packages. 1000 hours min at max operating junction temperature		
Steady-state-operation life or	1026	Condition D, 6000 cycles min	λ = 10	12 devices c = 0
Intermittent operation life or	1036			
Blocking life	1042			
Electrical measurements		As specified		

NOTES:

1. Electrical reject devices (and X-Ray for JANS) and PIND rejects from the same inspection lot may be used for all subgroups when electrical end-point measurements are not required. Not required for JANS.
2. If a given inspection lot undergoing group B inspection has been selected to satisfy group C inspection requirements, the 340-hour or 2,000 cycles life tests may be continued on test to 1,000 hours or 6,000 cycles, as applicable, in order to satisfy the group C life test requirements. In such cases, either the 340-hour or 2,000-cycle, as applicable, end-point measurements are optional and acceptance shall be determined by the 1,000-hour or 6,000-cycle, as applicable, end-point measurements.
3. Intermittent operation life shall be performed on all case mounted devices.

TABLE VI. GROUP D (RADIATION HARDNESS ASSURANCE TESTS) (NOTE 1)

TEST	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	JANS QUANTITY/ ACCEPT NUMBER	JANS NOTE	JANTXV QUANTITY/ ACCEPT NUMBER	JANTXV NOTE
SUBGROUP 1 (Note 2)						
Neutron irradiation	1017	25°C				
a. Qualification			(a) 11(0)	3	(a) 11(0)	4
b. QCI			(b) 11(0)	3	(b) 11(0)	4
End-point electrical parameters		As specified in accordance with associated detail specification				
SUBGROUP 2 (Note 5)						
Steady-state total dose irradiation	1019	25°C Maximum supply voltage				
a. Qualification			(a) 4(0) 2(0)	(a) 6 8	(a) 22(0)	7
b. QCI			(b) 4(0) 2(0)	(b) 6 8	(b) 22(0)	7
End-point electrical parameters		As specified in accordance with associated detail specification				
SUBGROUP 3 (Note 9)						
Gamma dot	3478	25°C	11(0)	3	11(0)	4
Single event upset		25°C				
End-point electrical parameters		As specified in accordance with associated detail specification				

NOTES:

1. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method. Group D tests may be performed prior to device screening (see 4.7.7).
2. Waive neutron tests for MOS devices except for charge coupled devices or where, by design, bipolar elements are an integral part of the device function.
3. In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
4. In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
5. JANTXV devices shall be inspected using either the JANTXV quantity/accept number criteria as specified, or by using the JANS criteria on each wafer.
6. In accordance with wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius, and spaced uniformly around this radius.
7. In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).
8. In accordance with wafer for device types with greater than 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.
9. Upset testing during qualification on first QCI shall be conducted when specified in purchase order or contract. When specified, the same devices may be tested in more than one subgroup.

TABLE VII. GROUP E INSPECTIONS (ALL QUALITY LEVELS) FOR QUALIFICATION ONLY (NOTE 1)

INSPECTIONS	MIL-STD-750		SAMPLING PLAN
	METHOD	CONDITION	
SUBGROUP 1			
Thermal shock Electrical measurements	1051	500 cycles min or as specified	As specified
SUBGROUP 2			
Dynamic AC intermittent operating life Electrical measurements or steady-state DC intermittent operating life Electrical measurements or steady-state DC blocking life Electrical measurements		As specified	As specified
SUBGROUP 3			
Destructive physical analysis	2101 2102	As specified	3 devices c = 0
SUBGROUP 4			
Thermal resistance Transistors: POWERFETs Bipolar Diodes IGBT GaAs	 3161 3131 3101 3103 3104	As specified	15
SUBGROUP 5 (Note 2)			
Barometric pressure (reduced) (required only on devices with rated voltage > 200V)	1001	As specified	15

NOTES:

1. Group E is required prior to shipping whenever group E is added to the associated detail specification. Manufacturers currently qualified to an associated detail specification shall also perform group E when the associated detail specification is revised to include group E.
2. The barometric pressure test shall be performed on a subgroup of the highest voltage type device for each barometric pressure group to accept that type and all other types of the same or lower voltage rating at that barometric pressure. In the event that a subsequent lot contains a higher voltage type, that type shall be tested to subgroup 5 of group C prior to acceptance of the lot.

TABLE 3. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion – Junction Depth – Sheet Resistivities – Oxide Thickness – Implant Dose Calibration – Uniformity	• Thin Film – Film Thickness – Uniformity – Refractive Index – Film Composition	• Photo Resist – Critical Dimension – Resist Thickness – Etch Rates	• Measurement Equipment – Critical Dimension – Film Thickness – 4 Point Probe – Ellipsometer
ASSEMBLY			
• Pre-Seal – Die Prep Visuals – Yields – Die Attach Heater Block – Die Shear – Wire Pull – Saw Blade Wear – Pre-Cap Visuals	• Post-Seal – Internal Package Moisture – Tin Plate Thickness – PIND Defect Rate – Solder Thickness – Leak Tests – Module Rm. Solder Pot Temp. – Seal – Temperature Cycle	• Measurement – XRF – Radiation Counter – Thermocouples – GM-Force Measurement	
TEST			
	– Handlers/Test Systems – Defect Pareto Charts – Lot % Defective – ESD Failures per Month	– Monitor Failures – Lead Strengthening Quality – After Burn-In PDA	
OTHER			
• IQC – Vendor Performance – Material Criteria – Quality Levels	• Environment – Water Quality – Clean Room Control	• IQC Measurement/Analysis – XRF – ADE – 4 Point Probe – Chemical Analysis Equipment	

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use over 1,000 Shewhart control charts to determine the normal variabilities in processes, materials, and products. Critical process variables are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a trend toward the limit. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost.

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process, and optimizing the procedures or design to yield

TABLE 4. HARRIS I.C. DESIGN TOOLS

	PRODUCTS	
DESIGN STEP	ANALOG	DIGITAL
Functional Simulation	Slice	Silos Proteous Socrates
Parametric Simulation	Slice Monte Carlo	Slice
Schematic Capture	Note 1	Daisy SDA-Mass Comp
Functional Checking	Note 1	SDA-LVS
Rules Checking	Calma-DRC	Harris Dash
Parasitic Extraction	Note 1	SDA-LVS

NOTE 1. Tools are in Development.

the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in MIL-STD-883 and MIL-M-38510 are used by our quality inspectors. The focus on this quality parameter has resulted in a continuous improvement over the past three years.

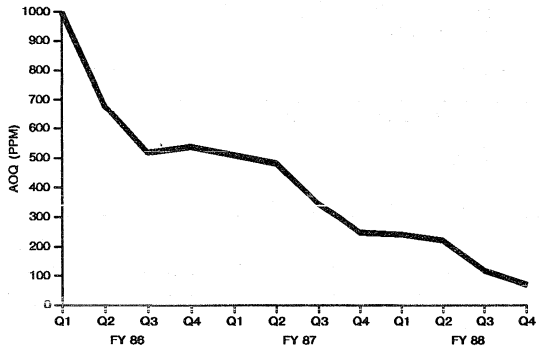


FIGURE 2. DEFECTIVE PARTS PER MILLION

AOQ has decreased from 1,000 PPM to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of the University of Tennessee, private consultants, and internally developed programs, training of over 2,000 engineers, supervisors, and operators/technicians has been completed.

Nearly 1,000 operators, 100 supervisors, and more than 800 engineers have been trained in SPC methods, providing them with tools to improve the overall level of uniformity of Harris products. Almost 300 engineers have received training in DOX methods: learning to evaluate changes in process operations, set up new processes, select or accept new equipment, evaluate materials, select vendors, compare two or more pieces of equipment, and compare two or more process techniques.

Over the past four years, Harris has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	LENGTH	TOPICS COVERED
SPC	Manufacturing Operators	8 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts
SPC	Manufacturing Supervisors	21 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts, Testing for Inspector Agreement, Cause & Effect Diagrams, 1 & 2 Sample Methods
SPC	Engineers and Managers	48 Hours	Basic Philosophy, Graphical Methods, Control Charts, Rational Subgrouping, Variance Components, 1 & 2 Sample Methods, Pareto Charts, Cause & Effect Diagrams
DOX (Design of Experiments)	Engineers and Managers	88 Hours	Factorial Designs, Fractional Factorial Designs, Blocking Designs, Variance Components, Computer Usage, Normal Probability Plotting
RSM (Response Surface Methods)	Engineers and Managers	40 Hours	Steepest Ascent, Central Composite Designs, Box-Behnken Designs, Computer Usage, Contour Plotting, Second Order Response Surfaces
Continuous Improvement Methods	Manufacturing Supervisors	12 Hours	Basic Philosophy, Pareto Analysis, Imagineering, Run Charts, Cause & Effect Diagrams, Histograms, Ideas of Control Charts
SPC- The Essentials	Department-Level Work Groups	20 Hours	Basic Philosophy, of Continous Improvement, Imagineering Pareto Charts, Cause & Effect Diagrams, Flow Charts, Graphical Display, Control Charts, Ideas of Experiment

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris' manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials. Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts – Oxygen – Resistivity • Control Charts Related to – Enhanced Gettering – Total Thickness Variation – Total Indicated Reading – Particulates • Certificate of Analysis for all Critical Parameters • Control Charts from On-Line Processing
Chemicals/Photoresists/ Gases	• Chemicals – Assay – Major Contaminants • Molding Compounds – Spiral Flow – Thermal Characteristics • Gases – Impurities • Photoresists – Viscosity – Film Thickness – Solids – Pinholes	• Certificate of Analysis on all Critical Parameters • Control Charts from On-Line Processing • Control Charts – Assay – Contaminants – Water – Selected Parameters • Control Charts – Assay – Contaminants • Control Charts on – Photospeed – Thickness – UV Absorbance – Filterability – Water – Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts – Assay – Contaminants – Dimensional Characteristics • Certificate of Analysis for all Critical Parameters
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Lead Integrity • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Manufacturing Science - CAM, JIT

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened — in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

A key adjunct to the CAM activity is Just In Time (JIT) material management. This is more than an inventory reduction technique: in many cases it involves reorganization of facilities and people. The essential concept is to form work units that are responsible for doing the whole job rather than bits of it. An employee has control over equipment, maintenance, cleanliness, scheduling, material, quality, and improvements.

In one Harris example, a photoresist flow consisting of several steps was previously organized in the classical departmentalized way. The inspection and etch areas were in different serial locations from the deposition and alignment areas. Work piled up at the slowest operation (inspection), and quality problems detected there were decoupled from the areas producing them by 20 to 30 feet and at least one day. Rework rates were very high; scrap was unacceptable.

When the area was reorganized into GT (group technology) cells (a basic concept of JIT), the inspection and alignment areas were physically coupled and people were organized into teams. The whole job (finished, defect-free wafers) was assigned to the GT cell (see Figure 3). Rework rates decreased 70%, scrap rates decreased 45%, and probe yields increased by 50%. This is only one of hundreds of examples of how JIT has improved our factory performance.

The JIT program/system works. This cultural change is vital and the benefits derived are impressive.

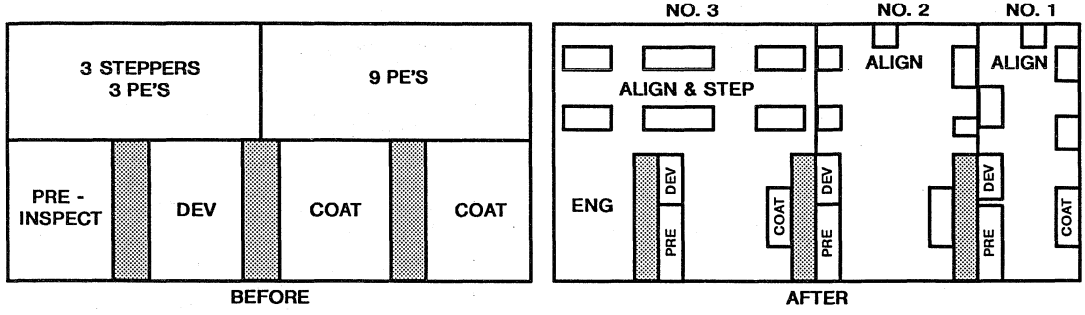


FIGURE 3. GROUP TECHNOLOGY CELL

Measurement

Analytical Services Laboratory

The Harris Analytical Laboratory is a company-wide technical resource for the physical and chemical characterization of microelectronic materials and products. Harris Facilities, Engineering, Manufacturing, and Quality are supported by the laboratory. Organized as chemical or microbeam analysis methodology, staff and instrumentation from both areas cooperate in fully integrated approaches necessary to complete any analytical study.

The lab is widely staffed and equipped to provide all manufacturing and operational functions with the following:

- Real time materials and process analyses to support routine manufacturing and development.
- Cooperative planning of all analytical investigations.
- Development of new techniques and method refinements as necessary to support internal and external customer requirements.
- Maintenance of awareness and accessibility to outside plant capabilities at commercial and university laboratories.
- Materials analyses with ultimate concern for product yield, quality and reliability.

The Microbeam Laboratory equipment is engaged principally in high resolution imaging and localized chemical analysis of microcircuits. The equipment includes:

- Electron Beam Analysis - Scanning Auger Microprobe, Scanning Electron Microscopes, and Transmission Electron Microscope.
- Ion Beam Analysis - Ion Microprobe, Secondary Ion Mass Spectrometer, and Ion Scattering Spectrometer.
- X-Ray Analysis - Energy Dispersive X-Ray (SEM), Wavelength Dispersive X-Ray (SEM), X-Ray Photoelectron Spectrometer, X-Ray Diffraction, and X-Ray Fluorescence.

The Chemistry Laboratory equipment affords a wide variety of analyses, capable for solid, liquid, and gaseous materials.

- Spectroscopy - Emission Spectrograph, Fourier Transform Infrared Spectrophotometer, Ultraviolet-Visible Spectrophotometer, Organic Carbon Analyzer, Mass Spectrometer, Atomic Absorption Spectrophotometer (flame and graphite furnace) and an Inductively Coupled Plasma Emission Spectrophotometer.
- Thermal Analysis - Differential Scanning Colorimeter, Thermogravimetric Analyzer Thermomechanical Analyzer.
- Separation Methods - Gas Chromatograph, Ion Chromatograph, Gas Chromatograph Mass Spectrometer, and Water, Oxygen, and Total Hydrocarbon Analyzers.
- Physical Testing - Profilometer, Microhardness Measurement, and Viscometers.
- Wet Chemistry - Titrimetry, Gravimetry, specific Ion Electrodes, Colorimeters, Bacteria Testing, and other qualitative chemical testing.

Capability for all process/product Mil-Spec test method methodology is maintained by the laboratory.

The department also maintains ongoing working arrangements with commercial, university, and equipment manufacturers' technical service laboratories and can obtain any material analysis in cases where instrumental capabilities are not available in our own facility.

Calibration Laboratory

Another important resource in the product assurance system is Harris Semiconductor's Calibration Lab. This area is responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both the production and engineering areas. The accuracy of instruments used at Harris in calibration is traceable to the National Bureau of Standards. The lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is given a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Failure Analysis Laboratory

The Failure Analysis Laboratory's capabilities encompass the isolation and identification of all failure modes/failure mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. Research vital to understanding the basic physics of the failure is also undertaken.

Failure analysis is a method of enhancing product reliability and determining corrective action. It is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assess effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential.

A general failure analysis procedure has been established in accordance with the current revision of MIL-STD-883, Section 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps for an analysis are determined as the situation dictates. See Figures 4 and 5 that represent the Failure Analysis Flow. Records are maintained by laboratory personnel and contain data, the failure analyst's notes, and the formal Product Analysis Report.

Reliability

Reliability Assessment and Enhancement

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing process. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life. Product reliability is maintained through the following sources.

Qualifications

Qualifications at Harris de-emphasize the sole dependence on production product which is only available late in the development cycle. The focus is primarily on the use of test vehicles to establish design ground rules for the product and the process that will eliminate any wearout mechanisms during the useful life of the product. However, to comply with the military requirements concerning reliability, product qualifications are performed.

In-line Reliability Monitors

In-line reliability monitors provide immediate feedback to manufacturing regarding the quality of workmanship, quality of raw materials, and the ultimate reliability implications. The rudimentary implementation of this monitoring is the "First Line of Defense," which is a pass/fail acceptance procedure based on control charts and trend analysis. The second level of monitoring is referred to as the "Early Warning System" and incorporates extensive diagnostic and characterization capabilities of various components that may impact the device reliability or stability. The quick feedback from these schemes allows more accurate correlation to process steps and corrective actions.

Reliability Fundamentals

Reliability, by its nature, is a mixture of engineering and probability statistics. This combination has derived a vocabulary of terms essential for describing the reliability of a device or system. Since reliability involves a measurement of time, it is necessary to accelerate the failures which may occur. This, then,

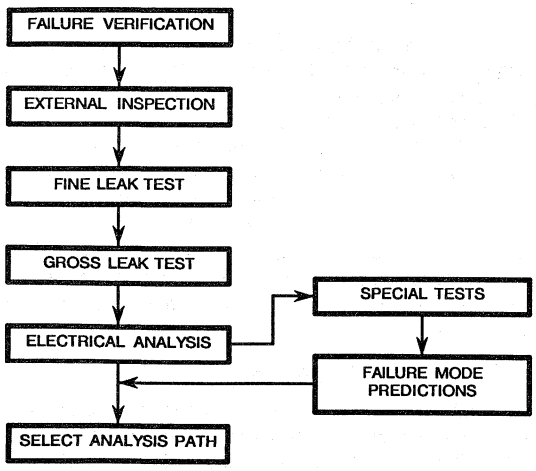


FIGURE 4. NON-DESTRUCTIVE

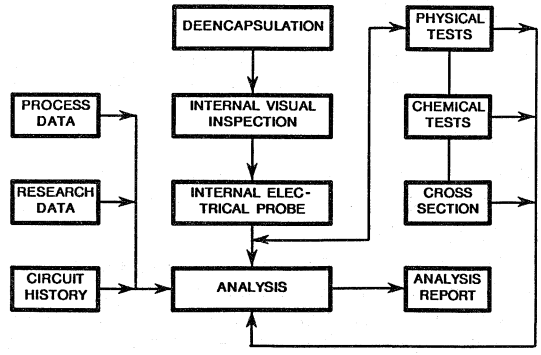


FIGURE 5. DESTRUCTIVE

introduces terms like "activation energy" and "acceleration factor," which are needed to relate results of stressing to normal operating conditions (see Table 7). Also, to assess product reliability requires failures. Therefore, only a statistical sample can be used to determine the model of the failure distribution for the entire population of product.

Failure Rate Primer

Failure Rate Calculations

Reliability data for products may be composed of several different failure mechanisms and requires careful combining of diverse failure rates into one comprehensive failure rate. Calculating the failure rate is further complicated because failure mechanisms are thermally accelerated at varying rates and thereby have differing accelerating factors. Additionally, this data is usually obtained from a variety of life tests at unique stress temperatures. The equation (right) accounts for these considerations and then inserts a statistical factor to obtain the confidence interval for the failure rate.

$$FIT = \left(\sum_{i=1}^{B} \frac{X_i}{\sum_{j=1}^{K} TDH_j \; AF_{ij}} \right) x\,10^9 \quad x\,M$$

B = # of distinct possible failure mechanisms

K = # of life tests being combined

X_i = # of failures for a given failure mechanism i = 1, 2, . . . B

TDG_j = Total device hours of test time (unaccelerated) for Life Test$_j$

AF_{ij} = Acceleration factor for appropriate failure mechanism i = 1, 2, . . . K

M = Statistical factor for calculating the upper confidence limit (M is a function of the total number of failures and an estimate of the standard deviation of the failure rates)

In the failure rate calculation, Acceleration Factors (AFij) are used to derate the failure rate from thermally accelerated Life Test conditions to a failure rate indicative of

TABLE 7. FAILURE RATE PRIMER

GLOSSARY OF TERMS

TERMS/DEFINITION	UNITS/DESCRIPTION
FAILURE RATE λ For Semiconductors, usually expressed in FITs. Represents useful life failure rate (which implies a constant failure rate). FITs are not applicable for infant mortality or wearout failure rate expressions.	FIT – Failure In Time 1 FIT – 1 failure in 10^9 device hours. Equivalent to 0.0001%/1000 hours FITs = $\frac{\text{\# Failures}}{\text{\# Devices x \# hours stress x AF}} \times 10^9 \times m$ m – Factor to establish Confidence Interval 10^9 – Establishes in terms of FITs AF – Acceleration Factor at temperature for a given failure mechanism
MTTF – Mean Time To Failure For semiconductors, MTTF is the average or mean life expectancy of a device. If an exponential distribution is assumed then the mean time to fail of the population will be when 63% of the parts have failed.	Mean Time is measured usually in hours or years. 1 Year = 8760 hours When working with a constant failure rate the MTTF can be calculated by taking the reciprocal of the failure rate. MTTF = $1/\lambda$ (exponential model) Example: =10 FITs at +55°C The MTTF is: MTTF = $1/\lambda = 0.1 \times 10^9$ hours = 100M hours
CONFIDENCE INTERVAL (C. I.) Establishes a Confidence Interval for failure rate predictions. Usually the upper limit is most significant in expressing failure rates.	Example: "10 FITs @ a 95% C. I. @ 55°C" means *only* that you are 95% certain that the FITs <10 at +55°C use conditions.

use temperatures. Though no standards exist, a temperature of +55°C has been popular and allows some comparison of product failure rates. All Harris Semiconductor Reliability Reports will derate to +55°C at both the 60% and 95% confidence intervals.

Acceleration Factors

The Acceleration Factors (AF) are determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and is an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{K}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right]$$

AF = Acceleration Factor

E_a = Thermal Activation Energy in eV from Table 8

K = Boltzmann's Constant (8.62×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature. With the use of the Arrhenius Equation, the thermal Activation Energy (E_a) term is a major influence on the result. This term is usually empirically derived and can vary widely.

Activation Energy

To determine the Activation Energy (E_a) of a mechanism (see Table 8) you must run at least two (preferably more) tests at different stresses (temperature and/or voltage). The stresses will provide the time to failure (Tf) for the populations which will allow the simultaneous solution for the Activation Energy by putting the experimental results into the following equations.

$$\ln (t_{f1}) = C + \frac{E_a}{KT_1}$$

$$\ln (t_{f2}) = C + \frac{E_a}{KT_2}$$

Then, by subtracting the two equations, the Activation Energy becomes the only variable, as shown below.

$$\ln(t_{f1}) - \ln(t_{f2}) = E_a/k(1/T1-1/T2)$$

$$E_a = K^* ((\ln(t_{f1}) - \ln(t_{f2}))/(1/T1-1/T2))$$

The Activation Energy may be estimated by graphical analysis plots. Plotting ln time and ln temperature then provides a convenient nomogram that solves (estimates) the Activation Energy.

Table 9 is a summary of military generic groups by process descriptions.

All Harris Reliability Reports from qualifications and Group C1 (all high temperature operating life tests) will provide the data on all factors necessary to calculate and verify the reported failure rate (in FITs) using the methods outlined in this primer.

TABLE 8. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3 - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3 - 0.5eV	HTOL & voltage stress screens.	Vendor Statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress tesing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5 - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistcal Process Control of assembly processes proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles Statistical Process Control or photoresist-/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test (EWS) and HTOL.	Statistical Process Control of C-V data, oxide/ interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL & oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

Qualification Procedures

New products are reliably introduced to market by the proper use of design techniques and strict adherence to process layout ground rules. Each design is reviewed from its conception through early production to ensure compliance to minimum failure rate standards. Ongoing monitoring of reliability performance is accomplished through compliance to MIL-STD-883 and standard Quality Conformance Inspection as defined in Method 5005.

New process/product qualifications have two major requirements imposed. First is a check to verify the proper use of process methodology, design techniques, and layout ground rules. Second is a series of stress tests designed to accelerate failure mechanisms and demonstrate the reliability of integrated circuits.

From the earliest stages of a new product's life, the design phase, through layout, and in every step of the manufacturing process, reliability is an integral part of every Harris Semiconductor product. This kind of attention to detail "from the ground up" is the reason why our customers can expect the highest quality for any application.

TABLE 9. HIGH TEMPERATURE OPERATING LIFE TEST SUMMARY

MIL-STD-883, GROUP C GENERIC RELIABILITY DATA

GENERIC GROUP	GROUP NAME	PROCESS DESCRIPTION	QUANTITY	QUANTITY FAILURE	HOURS @ 125°C	FAILURE RATE FITs @ 55°C 60% CONFIDENCE INTERVAL
D-49-3	Op. Amplifiers	Std. Linear, DI w/NiCr resistors	3482	6	3,215,708	62
D-49-4	Op. Amplifiers	Std. Linear, DI w/NiCr resistors	324	1	429,945	17
D-53	High Voltage Op. Amplifiers	High voltage DI	315	0	284,943	20
D-56	Data Acquisition	High beta high frequency, DI, NiCr	1022	5	1,868,349	100
F-103	Telecommunications	SAJI IVA	199	0	403,960	5
F-81-3	A/D Converters	SAJI IVA	201	0	183,222	10
F-81-4	A/D Converters	SAJI IVA	217	1	328,000	12
F-82	Switches & Mux	DI Al Gate & Si Gate MOS	121	0	82,836	23
F-99-3	Active Filters	SAJI IVA	196	1	184,262	24
F-99-4	Active Filters	SAJI IVA	407	1	470,324	9
G-85	Op. Amplifiers	Std. Linear, MOS, & High Frequency JFET	532	1	535,728	11
G-86	Comparators	Combination, Std. Linear & MOS	154	0	153,400	25
G-94-3	Switches & Mux	DI Al & Si Gate Linear CMOS	4351	41	7,443,054	103
G-94-4	Switches & Mux	DI Al & Si Gate Linear CMOS	906	0	889,816	20
C-41-4	CMOS RAMs	SAJI CMOS	2418	19	2,247,526	31
C-41-5	CMOS RAMs	SAJI CMOS	1104	10	1,105,094	53
C-42-4	CMOS PROMs & HPALs	SAJI CMOS	2645	28	4,074,728	61
C-105-4	Microprocessor and Peripherals	SAJI CMOS	3638	12	4,099,002	17

NOTE: All infant mortality failures (up to 168 hours or equivalent) have been removed from products sampled.

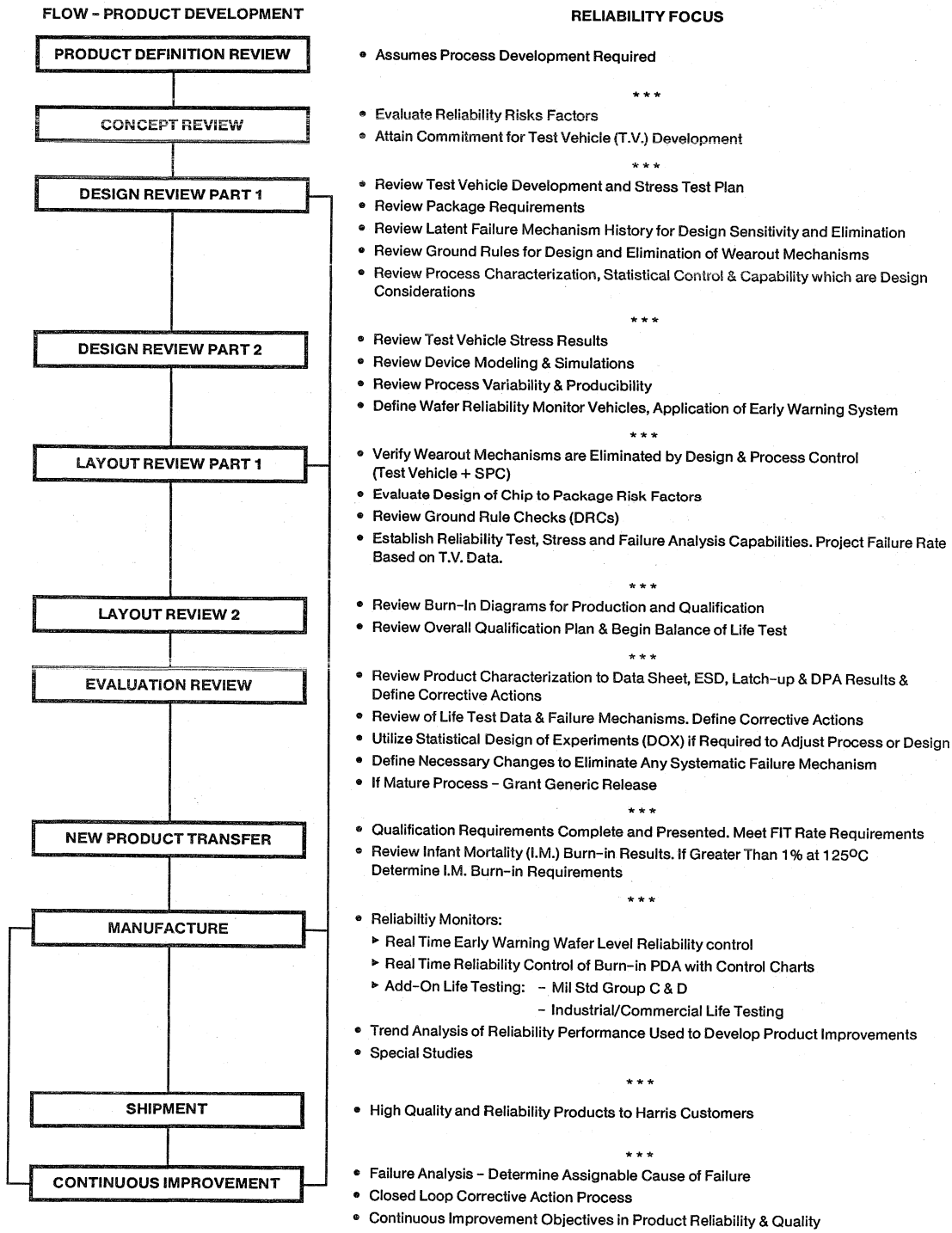


FIGURE 6. NEW PROCESS PRODUCT DEVELOPMENT AND LIFE CYCLE

JAN/SMD Certification

Harris Semiconductor has been an active participant in the JAN program since 1972 when it became the first manufacturer to JAN qualify a PROM. In the years since then, Harris has continued to offer an expanding line of JAN qualified devices including MIL-M-38510 JAN Class S line certification for the manufacture of radiation-hardened products. The complete listing of JAN Class S and Class B devices can be found in Section 16.

Harris is also an active participant in the Standard Military Drawing (SMD) Program. The SMD provides standardized Mil-Std-883 processing in conjunction with compliant, non-JAN devices as specified in paragraph 1.2.1 of Mil-Std-883. Manufacturer's qualified to supply a particular SMD device are listed in the back of the individual DESC drawing.

Radiation Hardening

Military, space and industrial electronic systems are receiving increasing demands for higher immunity from the damage that radiation can inflict upon them. The optimization of radiation hardness is a systems problem which flows through to each subsystem and component integrated circuit. Harris Semiconductor is the leader in providing radiation hardened microcircuits for systems designed to be exposed to space or nuclear events.

An integrated circuit can be classified as radiation hardened, radiation tolerant, or radiation resistant. Radiation hardened devices are guaranteed to meet full parametric levels specified in the data sheets up to the radiation level specified. Functional failure of a radiation hard device can be 10-100 times greater than the parametric levels listed in the respective data sheet. Devices classified as radiation tolerant or radiation resistant typically meet functional failure levels that are not guaranteed.

Hardening is achieved through:

- Design
- Special fabrication processes
- Continuous screening and quality control

Radiation affects circuits primarily through two basic mechanisms: displacement damage and ionization. Displacement damage occurs when high energy neutrons penetrate the semiconductor crystal lattice and physically dislocate atoms within the structure. It permanently affects lifetime, carrier mobility, leakage current, and bipolar device gain. Ionizing radiation effects can cause interface charge accumulation, which modifies MOS device thresholds and induces parasitic leakage paths. Both effects adversely affect IC performance.

After a device technology has been selected, the circuit is designed to take maximum advantage of the hardening options available for that technology.

BIPOLAR:

- Stabilizing expected gain
- Maximum emitter current density
- Guard-banding for increased resistor values

MOS:

- Allowances for changes in threshold voltages and leakage currents
- Dielectric isolation
- P+ guard-bands of N-channel transistors

Processing also lends hardness to these circuits. By minimizing gate oxide thickness, employing "hardened oxides," and utilizing proprietary hardening processes, Harris Semiconductor delivers circuits with higher packing densities and lower redesign costs.

Reliability is an issue that has distinguished Harris Semiconductor as a leader in the design and manufacture of radiation hardened memories, microprocessors, op amps, and full custom devices. Strict lot qualification, screening and testing procedures are maintained, along with stringent radiation screening procedures. All wafers in a run are processed together through all high temperature steps and metallization, and a sample of probed good dice is selected. These dice are assembled and tested for functionality, then subjected to the total dose radiation level guaranteed for each device, using Harris's own Gammacell 220 Cobalt 60 source with conditions specified by Mil-Std-883, method 1019 or customer requirements. The samples are then tested and accepted by previously defined criteria.

***JANTX/JANTXV* Flow Details Per Mil-S-19500**
All Specified Methods Per Mil-Std-750

I. 100% PRE-CONDITIONING (SCREENING):

Operation	Mil-Std-750 Method
1. Pre-Cap Visual (For JANTXV Only)	2072
2. Stabilization Bake	1032
3. Temperature Cycling	1051
4. Constant Acceleration	2006
5. Fine/Gross Leak Test	1071
6. Serialization	-
7. Electrical Tests	As Specified
8. Steady State Reverse Bias, 48 Hours	1039, Condition A
9. Interim Electrical Tests, Deltas (Recorded)	As Specified
10. Power Burn-In, 168 Hours	1039, Condition B
11. Final Electrical Tests, Deltas (Recorded)	As Specified

II. GROUP A INSPECTION - JANTX/JANTXV

Subgroup	Description	Method	Sample	Disposition
1	Visual & Mechanical	2071	77(0)	Non-Destruct
2	DC Static: 25°C		116(0)	Non-Destruct
3	DC Static: High/Low Temperature		116(0)	Non-Destruct
4	Dynamic: 25°C		116(0)	Non-Destruct
5	Safe Operating Area		38(1)	Non-Destruct

TOTAL SAMPLES FOR GROUP A: 193
NON-DESTRUCT: 193
DESTRUCT: 0

II. GROUP B INSPECTION - JANTX/JANTXV

Subgroup	Description	Method	Samples	Disposition
1	Solderability	2026	25(1)	Non-Destruct
	Resistance to Solvents	1022	Same	Non-Destruct
2	Temperature Cycle	1051	38(1)	Non-Destruct
	Hermeticity	1071	Same	Non-Destruct
	Electrical Tests		Same	Non-Destruct
3	Operating Life (340 Hours)	1027	77(1)	Non-Destruct
	Electrical Tests		Same	Non-Destruct
4	Decap: Initial Visual	2075	7(0)	Destruct
	Bond Strength	2037	Same	Destruct
5	Thermal Resistance	3131	38(1)	Non-Destruct
6	High Temperature Storage	1032	55(1)	Non-Destruct
	Electrical Tests		Same	Non-Destruct

TOTAL SAMPLES FOR GROUP B: 240
NON-DESTRUCT: 233
DESTRUCT: 7

***JANTX/JANTXV* Flow Details Per Mil-S-19500 (Continued)**
All Specified Methods Per Mil-Std-750

III. GROUP C INSPECTION - JANTX/JANTXV

Subgroup	Description	Method	Samples	Disposition
1	Physical Dimensions	2066	25(1)	Non-Destruct
2	Thermal Shock	1056	38(1)	Destruct
	Terminal Strength	2036	Same	Destruct
	Hermetic Seal	1071	Same	Destruct
	Moisture Resistance	1021	Same	Destruct
	External Visual	2071	Same	Destruct
	Electrical Tests		Same	Destruct
3	Shock	2016	38(1)	Non-Destruct
	Vibration Variable Frequency	2056	Same	Non-Destruct
	Constant Acceleration	2006	Same	Non-Destruct
	Electrical Tests		Same	Non-Destruct
4	Salt Atmosphere	1041	25(1)	Destruct
5	N/A	-	-	-
6	Operating Life (1,000 Hours)	1026	38(1)	Non-Destruct
	Electrical Tests		Same	Non-Destruct

TOTAL SAMPLES FOR GROUP C: 164
NON-DESTRUCT: 101
DESTRUCT: 63

DATA PACK

Group A: Recorded readings.

Group B: Attributes for inspections recorded readings for Electrical Tests

Group C: Attributes for inspections recorded readings for Electrical Tests

Rad Testing: C or C - No recorded data

Class S Flow Details Per Mil-S-19500
All Specified Methods Per Mil-Std-750

I. PRE-CONDITIONING (SCREENING): 100%

Operation	Mil-Std-750 Method
A. Pre-Cap Visual	2072
B. High Temperature Life (Stabilized Bake)	1032
C. Temperature Cycling	1051
D. Constant Acceleration	2006
E. PIND	2052
F. Fine/Gross Leak	1071
G. Serialization	-
H. Electric Parameters (Recorded)	As Specified
I. High Temperature Reverse Bias	48 Hours at 150°C
J. Electric Parameters and Deltas (Recorded)	As Specified
K. Burn-In, Condition A	1039
L. Electric Parameters and Deltas (Recorded)	As Specified
M. Power Burn-In, Condition C	1039
N. Electric Parameters and Deltas (Recorded)	As Specified
O. Fine/Gross Leak	1071
P. X-Ray	2076
Q. External Visual	2071
R. Solder DIP	-

II. GROUP A INSPECTION - JANS

Subgroup	Description	Method	Sample	Disposition
1	Visual and Mechanical Inspection	2071	15(0)	Non-Destruct
2	DC Static: 25°C		116(0)	Non-Destruct
3	DC Static: High/Low Temperature		116(0)	Non-Destruct
4	Dynamic: 25°C		116(0)	Non-Destruct
5	Safe Operating Area		38(1)	Non-Destruct
7	Selected Dynamic Tests		38(1)	Non-Destruct

TOTAL SAMPLES FOR GROUP A: 131
NON-DESTRUCT: 131
DESTRUCT: 0

Class S Flow Details Per Mil-S-19500
All Specified Methods Per Mil-Std-750

III. GROUP B INSPECTION - JANS

Subgroup	Test	Method	Sample	Disposition
1	Physical Dimensions	2066	38(1)	Non-Destruct
2	Solderability	2026	-	-
	Resistance to Solvents	1022	25(1)	Destruct
3	Temperature Cycle	1051	38(1)	Non-Destruct
	Fine/Gross Leak	1071	38(1)	Non-Destruct
	Electrical Measurements (Recorded)	As Specified	38(1)	Non-Destruct
	Decap	2075	6(0)	Destruct
	SEM	2077	6(0)	-
	Bond Strength	2037	6(0)	-
	Die Shear	2017	6(0)	-
4	Intermittent Operating Life	1037	38(1)	Non-Destruct
	Electrical Measurements (Recorded)	As Specified	-	-
5	Accelerated Steady State Operating Life	1027	38(1)	Destruct
	Electrical Measurements (Recorded)	-	-	-
	Bond Strength	2037	18(1)	-
6	Thermal Resistance	3031	38(1)	Non-Destruct

TOTAL GROUP B SAMPLES: 239
NON-DESTRUCT: 152
DESTRUCT: 87

IV. GROUP C INSPECTION

Subgroup	Test	Method	Sample	Disposition
1	Physical Dimensions	2066	25(1)	Non-Destruct
2	Thermal Shock	1056	38(1)	Destruct
	Thermal Strength	2036	38(1)	Destruct
	Fine/Gross Leak	1071	38(1)	Destruct
	Moisture Resistance	1021	38(1)	Destruct
	Electrical Measurements (Recorded)	-	38(1)	Destruct
3	Shock	2016	38(1)	Destruct
	Vibration Variable Frequency	2056	38(1)	Destruct
	Constant Acceleration	2006	38(1)	Destruct
4	Salt Atmosphere	1041	25(1)	Destruct
6	Intermittent Operating Life	1036	38(1)	Destruct
	Electrical Measurements (Recorded)	-	38(1)	Destruct

TOTAL GROUP C SAMPLES: 164
ON-DESTRUCT: 25
DESTRUCT: 139

Harris Mil-Std-883 Compliant Screening Flows

SCREEN (NOTE 1)	METHOD PER MIL-STD-883	REQUIREMENT	
		CLASS S	CLASS B
Wafer Lot Acceptance	5007	Note 2	No
SEM (Traceable to Diffusion)	2018	Yes	No
Wire Bond Pull Monitor	2011, condition D, LTPD = 10 on number of leads pulled, 2 units minimum	Note 3	No
Die Shear Monitor	2019, 2(0)	Note 3	No
Gamma Radiation Assurance Tests	1019	As required	No
Nondestructive Bond Pull	2023	Yes/No, Note 4	No
Internal Visual Inspection	2010	Condition A	Condition B
Customer Source Inspection	Per detail part drawing	As required	No
Temperature Cycling	1010 condition C, 10 cycles	Yes	Yes
Constant Acceleration	2001, Y_1 orientation, 30Kg	Yes	Yes
Particle Impact Noise Detection	2020, condition A, 20g	Yes	No
Visual Inspection	None, Missing leads, broken packages, lids off	Yes	No
Initial Electrical Test	At Harris' discretion	Yes	Yes
Marking	Per detail part drawing	Yes	No
Serialization	None. No duplication of numbers in a single datecode	Yes	No
Radiographic Inspection	2010, 2 copies, 2 views (Note 5)	Yes	No
+25°C Electrical Test	Per detail part drawing with datalog of selected parameters	Yes	No
Burn-In, Static	1015, condition A or B, 72 hours minimum at 125°C	Yes (Note 6)	No
Burn-In	1015, condition A, B or D, 160 hours at 125°C or equivalent	No	Yes
+25°C Electrical Test	Per detail part drawing with datalog of selected parameters Go/no-go per detail part drawing	Yes No	No Yes
Delta Calculation	Per detail part drawing (Note 7)	Yes	No
Burn-In, Dynamic	1015, condition D, 240 hours minimum at 125°C	Yes	No
Percent Defective Allowable	5% on +25°C DC & W fails combined. 3% on +25°C functional failures. 5004, para 3.5.1, 5% on subgroup 1 (+25°C DC) failures	Yes No	No Yes
-55°C or +125°C Electrical Test	Per detail part drawing with datalog of selected parameters Go/no-go per detail part drawing	Yes No	No Yes
Fine Leak Test	1014, condition A or B	Yes	Yes
Gross Leak Test	1014, condition C	Yes	Yes
Marking	Per detail part drawing	No	Yes
-55°C or +125°C Electrical Test	Go/no-go per detail part drawing	No	Yes
External Visual Inspection	2009	Yes	Yes
Group A Inspection	5005, Table 1, 116/0, each lot. Para 3.5.1 of 5005 exercized	Yes	Yes
Customer Source Inspection	Per detail part drawing	As required	No
Group B Inspection	5005, Table 2A, (Note 8) 5005, Table 2B, (Note 8)	Yes No	No Yes
Group C Inspection	5005, Table 3, every four quarter or as required	No	Yes
Group D Inspection	5005, Table 4, every 52 weeks or as required	Yes	Yes
External Visual Examination	2009 on shippable QCI units	Yes	Yes

See notes next page.

NOTES:

1. Order (sequence) of testing shall be as permitted by Mil-Std-883, method 5004, paragraph 3.1.1 through 3.1.19. Alternate screening shall be as permitted by Mil-Std-883, method 5004, paragraph 3.3.1.
2. Per Mil-Std-883, method 5007 except that separate monitors are used for thermal stability for bipolar linear device types which operate above 5.0V and contain MOS transistor(s) and digital devices that operate above 10.0V and contain MOS structures.
3. Performed at the beginning of each shift/set-up and every two hours thereafter.
4. Nondestructive bond pull will be performed up to 40 wire bonds per device. Therefore, devices with greater than 40 wire bonds will be supplied as noncompliant product.
5. Only one view is required for flatpack and LCC packages which have lead/terminal metal on four sides.
6. This 72-hour static burn-in test is not meant to replace the recommended 72-hour reverse bias static burn-in test of Mil-Std-883, method 5004, screen 3.1.12.
7. Deltas are calculated separately through static burn-in and through dynamic burn-in, not through both burn-in tests combined.
8. End point electrical parameters are performed at +25°C DC only for all subgroups except group B, subgroup 5 which will be screened at -55°C DC, +25°C DC and +125°C DC for both pre- and post-steady state life test.

TABLE II. SCREENING REQUIREMENTS

SCREEN	MIL-STD-750 METHOD	CONDITION	JANS REQUIREMENTS	JANTXV REQUIREMENTS	JANTX REQUIREMENTS
1. Internal visual (pre-cap) inspection (Note 1)					
POWERFETs	2069		100%	100%	-
Microwave transistors	2070				
Transistors	2072				
Diodes	2073		-	When specified	-
	2074				
2. High temperature life Nonoperating life (stabilization bake)	1032	T_{STG} max	Optional	Optional	Optional
3. Temperature cycling	1051	No dwell is required at 25°C. Test condition C, except step 3 at 175°C, +5°C, -0°C, 20 cycles, t(extremes) > 10 min	100%	100%	100%
Surge (as specified) (Note 2)	4066	Condition B, as specified	100%	100%	100%
Thermal response (as specified)		As specified	100%	100%	100%
Transistors, POWERFETs	3161		-	-	-
Bipolar	3131		-	-	-
Diodes	3101		-	-	-
IGBT	3103		-	-	-
GaAs	3104		-	-	-
4. Constant acceleration (see 4.6)	2006	Y_1 direction at 20,000 G min except at 10,000 G min for devices with power rating of ≥ 10 watts at T_C = 25°C. The 1 minute hold time requirement shall not apply	100% except not required for metallurgically bond diodes	Optional (Note 3)	Optional (Note 3)
5. Particle impact noise detection (Note 4)	2052	Condition A	100% See 4.6.4.2	-	-
6. Instability shock test (axial lead diodes only) (Note 5)					
a. Forward instability shock test (FIST)	2081		100%	-	-
b. Backward instability vibration test (BIST)	2082		100%	-	-
7. Hermetic seal					
a. Fine	1071	Test condition G or H, max leak rate = 5 x 10^{-8} atm cc/s except 5 x 10^{-7} atm cc/s for devices with internal cavity > 0.3 cc. Omit for double plug diodes	Optional	100% (Note 6)	100% (Note 6)
b. Gross			-	100% (Note 6)	100% (Note 6)
8. Serialization		See 3.7.9	100%	-	-
9. Interim electrical parameters		As specified	100% (Read and record)	For case mounted rectifiers as specified	For case mounted rectified as specified

See Notes at End of Table

TABLE II. SCREENING REQUIREMENTS (CONTINUED)

SCREEN	MIL-STD-750 METHOD	CONDITION	JANS REQUIREMENTS	JANTXV REQUIREMENTS	JANTX REQUIREMENTS
10. High temperature reverse bias (HTRB)		48 hours min at T_A, (T_C, or T_L is optional) = 150°C (min) and minimum applied voltage as follows:			
a. Transistors	1039	a. Transistors - 80% to 85% (min) of rated V_{CB} (bipolar), V_{GS}(FET), or V_{DS}(FET) as applicable. Test condition A	100%	100%	100%
b. POWERFETs	1042	b. POWERFETs - 80% to 85% of rated V_{GS}. Test condition B	100%	100%	100%
c. For diodes and rectifiers	1038	c. Diodes (except LEDs and zeners) 80% to 85% of rated V_R, or 95%-100% of V_{RWM} when half sine condition is specified. Test condition A	100% (Note 7)	100%	100%
11. Interim electrical and delta parameters for PDA (see 4.6.1) For stud rectifiers as a minimum		As specified but including all delta parameters as a minimum. Leakage current shall be measured on each device before any other test is made	100% (measure all specified parameters within 16 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 13.)	100% (measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 13.)	100% (measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 13.)
12. Power burn-in		As specified	100%	100%	100%
a. Bipolar transistors	1039	a. Transistors. Test condition B	240 hrs (min)	160 hrs (min)	160 hrs (min)
b. POWERFETs	1042	b. POWERFETs (see 4.6.7) Condition C shall precede condition A			
		1. Test condition C	240 hrs (min)		
		2. Test condition A	160 hrs (min)	160 hrs (min)	160 hrs (min)
c. Diodes, zeners and rectifiers	1038	c. Diodes, zeners (except case mounted rectifier packages for JANTX and JANTXV) Test condition B	240 hrs (min)	96 hrs (min)	96 hrs (min)
d. Thyristors (Note 8)	1040	d. Thyristors	240 hrs (min)	96 hrs (min)	96 hrs (min)
13. Final electrical test (See 4.6 and 4.6.5)		As specified	100%	100%	100%
a. Interim electrical & delta parameters for PDA see (4.6.1)	All interim and	delta parameter measurements must be completed within 96 hrs after removal from burn-in conditions	Interim electrical and delta parameters as a min. (Read & record)	Interim electrical and delta parameters as a min. (Read & record) (See 4.6.3.2.)	Interim electrical and delta parameters as a min. (Read & record) (See 4.6.3.2.)
b. Other electrical parameters			Group A, Subgroup 2 & 3	Group A, Subgroup 2	Group A, Subgroup 2
14. Hermetic seal	1071	(Same as 7 above) (Note 9)	100%	Optional (Note 6)	Optional (Note 6)
a. Fine					
b. Gross					
15. Radiography	2076	(Note 9)	100%	-	-
16. External visual examination	2071	To be performed after complete marking	100%	-	-

See Notes Next Page

NOTES:

1. Visual inspection (method 2074) on clear glass diodes shall be performed any time prior to screen 8.
2. Shall be performed any time before screen 13. Surge shall precede thermal response when both tests are performed.
3. Constant acceleration shall be performed on gold bond devices.
4. PIND is not applicable to any device with external and internal pressure contacts (die to electrical contacts) optical coupled isolators, and double plug diodes. PIND screening may be performed any time after screen 4 when imposed by contract or purchase order (see 3.7.6.1).
5. Omit BIST and FIST tests for double plug or case-mounted diodes. Omit FIST test for temperature compensated referenced diodes.
6. Fine and gross seal leak test for JANTX and JANTXV shall be performed in either screen 7 or screen 14.
7. For JANS only, zener diodes shall be subjected to high temperature reverse bias at 80% to 85% of nominal V_Z for $V_Z \geq 10V_Z$. Omit test for devices with $V_Z \leq 10V_Z$.
8. For JANTX and JANTXV levels full wave-blocking test shall replace power burn-in for all thyristors.
9. The radiographic and seal screens for JANS may be performed in any order following final electrical test. Glass diodes shall not be painted until after seal tests. When hermetic seal testing is performed in screen 7 it does not have to be performed again in screen 14 for double plug diode construction.

RAD-HARD 15

PACKAGING AND ORDERING INFORMATION

Packaging and Ordering Information

Packaging Options

Harris Rad-Hard integrated circuits are available in a wide range of hermetically sealed packages of various lead counts and package configurations.

For most devices, materials and assembly conform to Mil-M-38510 specifications. Mil-Std-883C post assembly testing includes temperature cycling (method 1010, condition C), constant acceleration testing (method 2001, condition D or E, Y1 orientation), particle impact noise detection (method 2020, condition A or B), and seal testing (method 1014, condition A, B or C2). Customer-specific materials, assembly, and post-assembly testing are available for standard and custom packaging.

Package availability for a particular device, excluding discretes is shown on the following pages. Power MOSFET availability is included in the discrete chapter, pages 3.3 - 3.8. Package outline drawings and dimension tables for all packages are included on the following pages.

STANDARD PACKAGE SUMMARY CHART

NUMBER OF LEADS/PINS	BRAZE, WELD SEAL DIPS	CERDIP	BRAZE, WELD SEAL FLATPACK	CERPACK	LEADLESS CHIP CARRIER	METAL CAN
8						X
14	X	X	X	X		X
16	X	X	X	X		
18	X		X		X	
20	X	X	X		X	
22	X	X	X			
24	X	X	X		X	
28	X	X	X	X	X	
32					X	
40	X					
44					X	

Rad-Hard Devices Package Options

PART NUMBER	BRAZE, WELD SEAL DIP	CERDIP	BRAZE, WELD SEAL FLATPACK	CERPACK	LEADLESS CHIP CARRIER	METAL CAN
HS-15530RH		E				
HS-1840RH	M	F	EE	W		
HS-245/246/248/249RH	G		X			
HS-302/303/306/307RH	G, H			U, V		
HS-3374RH	K					
HS-3516RH						
HS-3530RH						FF
HS-384/390RH	G, H			U, V		
HS-5104RH						
HS-508ARH	H	B		V		
HS-54C138RH	H					
HS-6504RH/RRH	I		AA		O	
HS-6508RH	H	(B)	Y			
HS-6514RH/RRH	I		AA		O	
HS-65C162RH/RRH	L		DD		S	
HS-65C262RH/RRH	J		DD		S	
HS-65T262RH/RRH	J		DD		S	
HS-65T262RH/RRH	J		DD		S	
HS-65758	M, E		EE			
HS-6551RH	K		DD			
HS-65643RH	L		DD, EE			
HS-65647RH	L		DD, EE			
HS-6617RH	L		DD		S	
HS-80C85RH	N				(T)	
HS-80C86RH	N				(T)	
HS-81C55/56RH	N				(T)	
HS-82C08RH	J					
HS-82C12RH	L					
HS-82C37ARH	N				(T)	
HS-82C54RH	L					
HS-82C55RH	N				(T)	
HS-82C85RH	L					
HS-83C55RH	N				(T)	
HS-6564RH	Module					
HCS/HCTS00	G		X			
HCS/HCTS02	G		X			
HCS/HCTS04	G		X			
HCTS08	G		X			
HCS10	G		X			
HCTS11	G		X			
HCTS14	G		X			
HCTS20	G		X			
HCTS21	G		X			
HCTS27	G		X			
HCTS30	G		X			
HCS32	G		X			
HCTS 32	G		X			
HCS/HCTS109	H		Y			
HCTS112	H		Y			
HCS/HCTS138	H		Y			
HCTS139	H		Y			
HCTS153	H		Y			
HCS154	L		DD			
HCTS157	H		Y			
HCTS160	H		Y			
HCS/HCTS161	H		Y			
HCTS163	H		Y			
HCS164	G		X			
HCS165	H		Y			

(T) Alternate package available on request

Rad-Hard Devices Package Options

PART NUMBER	BRAZE, WELD SEAL DIP	CERDIP	BRAZE, WELD SEAL FLATPACK	CERPACK	LEADLESS CHIP CARRIER	METAL CAN
HCS166	H		Y			
HCS/HCTS190	H		Z			
HCTS191	H		Y			
HCTS240	J		BB			
HCS/HCTS244	J		BB			
HCS/HCTS245	J		BB			
HCS273	J		BB			
HCS/HCTS32	G		X			
HCS/HCTS373	J		BB			
HCS/HCTS374	J		BB			
HCTS390	H		Y			
HCTS540	J		BB			
HCS573	J		BB			
HCTS574	J		BB			
HCS/HCTS74	G		X			
HCTS86	G		X			

(T) Alternate package available on request

CD4000-Series Rad-Hard Package Options

PART NUMBER	BRAZED, WELD SEAL DIP	CERDIP	BRAZED, WELD SEAL FLATPACK
CD4000B	G	A	X
CD4001B	G	A	X
CD4002B	G	A	X
CD4006B	G	A	X
CD4007UB	G	A	X
CD4008B	H	B	Z
CD4009UB	H	B	Z
CD4010B	H	B	Z
CD4011B	G	A	X
CD4012B	G	A	X
CD4013B	G	A	X
CD4014B	H	B	Z
CD4015B	H	B	Z
CD4016B	G	A	X
CD4017B	H	B	Z
CD4018B	H	B	Z
CD4019B	H	B	Z
CD4020B	H	B	Z
CD4021B	H	B	Z
CD4022B	H	B	Z
CD4023B	G	A	X
CD4024B	G	A	X
CD4025B	G	A	X
CD4026B	H	B	Z
CD4027B	H	B	Z
CD4028B	H	B	Z
CD4029B	H	B	Z
CD4030B	G	A	X
CD4031B	H	B	Z
CD4033B	H	B	Z
CD4034B	L	E	DD
CD4035B	L	E	DD
CD4040B	H	B	Z
CD4041UB	G	A	X
CD4042B	H	B	Z

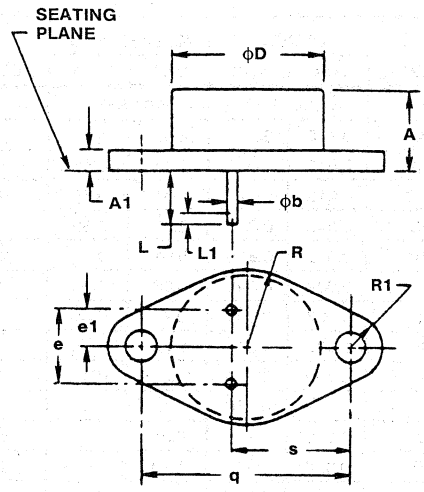
PART NUMBER	BRAZE, WELD SEAL DIP	CERDIP	BRAZE, WELD SEAL FLATPACK
CD4043B	H	B	Z
CD4044B	H	B	Z
CD4046B	H	B	Z
CD4047B	G	A	X
CD4048B	H	B	Z
CD4049UB	H	B	Z
CD4050B	H	B	Z
CD4051B	H	B	Z
CD4052B	H	B	Z
CD4053B	H	B	Z
CD4060B	H	B	Z
CD4063B	H	B	Z
CD4066B	G	A	X
CD4067B	L	E	DD
CD4068B	G	A	X
CD4069UB	G	A	X
CD4070B	G	A	X
CD4071B	G	A	X
CD4072B	G	A	X
CD4073B	G	A	X
CD4075B	G	A	X
CD4076B	H	B	Z
CD4077B	G	A	X
CD4078B	G	A	X
CD4081B	G	A	X
CD4082B	G	A	X
CD4085B	G	A	X
CD4086B	G	A	X
CD4089B	H	B	Z
CD4093B	G	A	X
CD4094B	H	B	Z
CD4095B	G	A	X
CD4096B	G	A	X
CD4097B	L	E	DD
CD4098B	H	B	Z

CD4000-Series Rad-Hard Package Options (Continued)

PART NUMBER	BRAZE, WELD SEAL DIP	CERDIP	BRAZE, WELD SEAL FLATPACK
CD4099B	H	B	Z
CD4502B	H	B	Z
CD4503B	H	B	Z
CD4508B	L	E	DD
CD4510B	H	B	Z
CD4511B	H	B	Z
CD4512B	H	B	Z
CD4514B	L	E	DD
CD4515B	L	E	DD
CD4516B	H	B	Z
CD4517B	H	B	Z
CD4518B	H	B	Z
CD4520B	H	B	Z
CD4527B	H	B	Z
CD4532B	H	B	Z
CD4536B	H	B	Z
CD4555B	H	B	Z
CD4556B	H	B	Z
CD4585B	H	B	Z
CD4724B	H	B	Z
CD14538B			
CD40100B	H	B	Z
CD40101B	G	A	X
CD40102B	H	B	Z
CD40103B	H	B	Z

PART NUMBER	BRAZE, WELD SEAL DIP	CERDIP	BRAZE, WELD SEAL FLATPACK
CD40104B	H	B	Z
CD40105B	H	B	Z
CD40106B	G	A	X
CD40107B	G	A	X
CD40108B	L	E	DD
CD40109B	H	B	Z
CD40110B	H	B	Z
CD40147B	H	B	Z
CD40160B	H	B	Z
CD40162B	H	B	Z
CD40163B	H	B	Z
CD40174B	H	B	Z
CD40175B	H	B	Z
CD40181B	L	E	DD
CD40182B	H	B	Z
CD40192B	H	B	Z
CD40193B	H	B	Z
CD40194B	H	B	Z
CD40208B	L	E	DD
CD40257B	H	B	Z

Discrete Packages

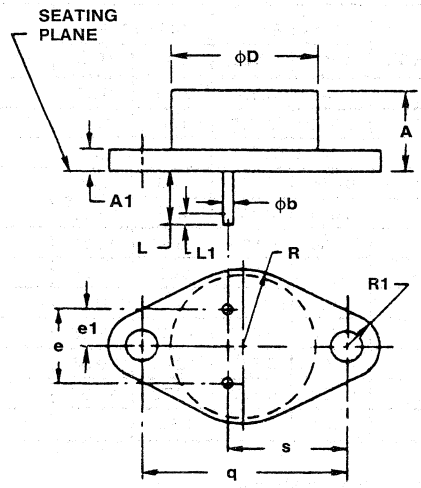


JEDEC TO-204AA

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.250	0.450	6.4	11.4	
A1	–	0.135	–	3.42	
ϕb	0.038	0.043	0.968	1.092	3
ϕD	–	0.875	–	22.22	
e	0.420	0.440	10.67	11.17	
e1	0.205	0.225	5.21	5.71	
L	0.312	–	7.93	–	
ϕP	0.151	0.165	3.84	4.19	
q	1.187 BSC		30.15 BSC		
R	–	0.525	–	13.33	
R1	–	0.188	–	4.77	6
s	0.655	0.675	16.64	17.14	

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5, 1973.
3. Two leads.
4. Square or radius on end of terminal optional.
5. Two holes.
6. Both ends.



JEDEC TO-204AE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.250	0.450	6.4	11.4	
A1	0.060	0.135	1.53	3.42	
ϕb	0.057	0.063	1.45	1.60	3
ϕD	–	0.875	–	22.22	
e	0.420	0.440	10.67	11.17	
e1	0.205	0.225	5.21	5.71	
L	0.440	0.480	11.18	12.19	3
L1	–	–	–	–	
ϕp1	0.151	0.165	3.84	4.19	5
q	1.187 BSC		30.15 BSC		
R	0.495	0.525	12.58	13.33	
R1	0.131	0.188	3.33–	4.77	6
s	0.655	0.675	16.64	17.14	

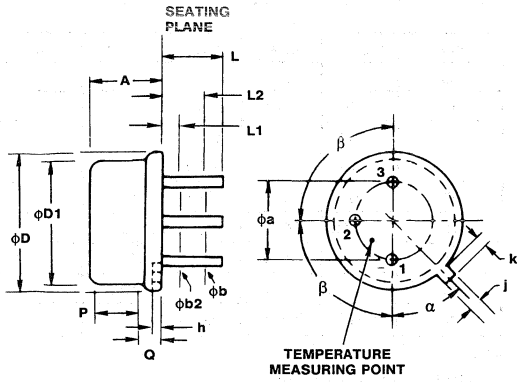
NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5, 1973.
3. Two leads.
4. Square or radius on end of terminal optional.
5. Two holes.
6. Both ends.

BSC = Basic Spacing Between Centerlines

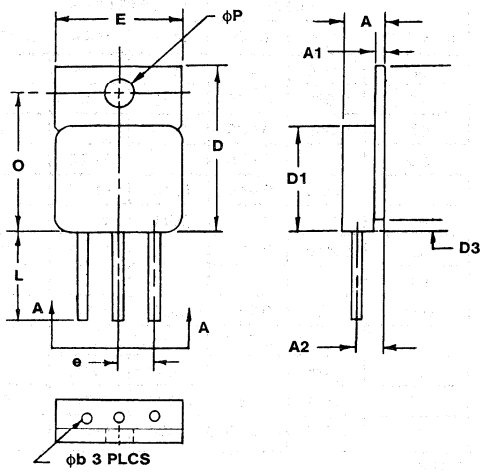
Discrete Packages

JEDEC TO-205AF (TO-39)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
φa	0.200 BSC		5.08 BSC		4
A	0.160	0.180	4.07	4.57	
φb	0.016	0.021	0.41	0.53	5
φb2	0.016	0.019	0.41	0.48	5
φD	0.340	0.370	8.64	9.39	
φD1	0.315	0.355	8.01	9.01	2
h	0.009	0.041	0.23	1.04	
j	0.028	0.034	0.72	0.86	
k	0.029	0.045	0.74	1.14	1
L	0.500	0.750	12.70	19.05	5
L1	-	0.050	-	1.27	5
L2	0.250	-	6.35	-	5
P	0.070	-	1.78	-	2
Q	-	0.050	-	1.27	3
α	45° Nominal				
β	90° Nominal				

JEDEC TO-258



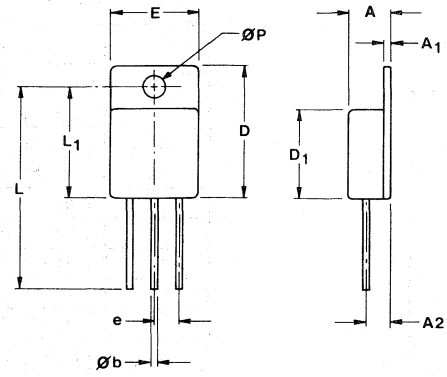
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.240	0.270	6.09	6.85	
A1	0.035	0.045	0.88	1.14	
A2	0.140 BSC		3.55 BSC		
φb	0.055	0.065	1.39	1.65	
D	0.815	0.835	20.70	21.20	
D1	0.530	0.550	13.46	13.97	
D3	0.000	0.092	0.00	2.33	
e	0.200 BSC		5.08 BSC		
E	0.685	0.695	17.39	17.65	
L	0.500	0.750	12.70	19.05	
Q	0.697	0.707	17.70	17.95	
φP	0.155	0.165	3.93	4.19	

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and Tolerancing per ANSI Y14.5.M. 1982.
3. Controlling Dimension: inches, millimeters
4. See MO-078 for same case in 5-lead version.

BSC = Basic Spacing Between Centerlines

Discrete Packages



JEDEC TO-254AA
Flange-Mounted Header Family
(Peripheral Terminals)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.249	0.260	6.32	6.60	
A1	0.040	0.050	1.02	1.27	
A2	0.150 BSC		3.81 BSC		
ϕb	0.035	0.045	0.89	1.14	
D	0.790	0.800	20.07	20.32	3
D1	0.535	0.545	13.59	13.84	
e	0.150 BSC		3.81 BSC		
E	0.535	0.545	13.59	13.84	3
L	1.195	1.235	30.35	31.40	
L1	0.665	0.685	16.89	17.40	
ϕP	0.139	0.149	3.53	3.78	

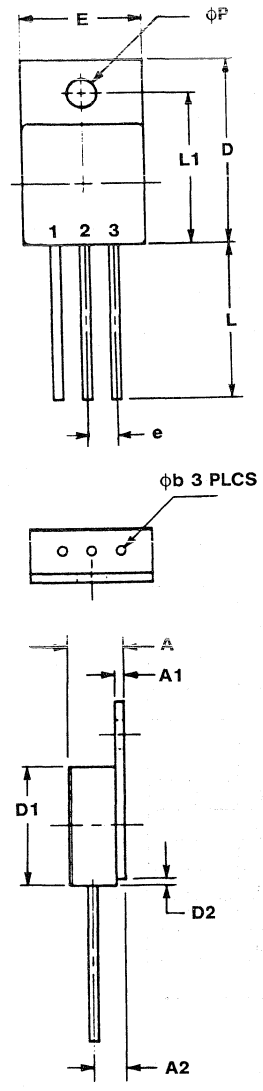
NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M. 1982.
3. Glass meniscus included in Dimensions D and E.
4. Controlling dimension: inch.

BSC = Basic Spacing Between Centerlines

Discrete Packages

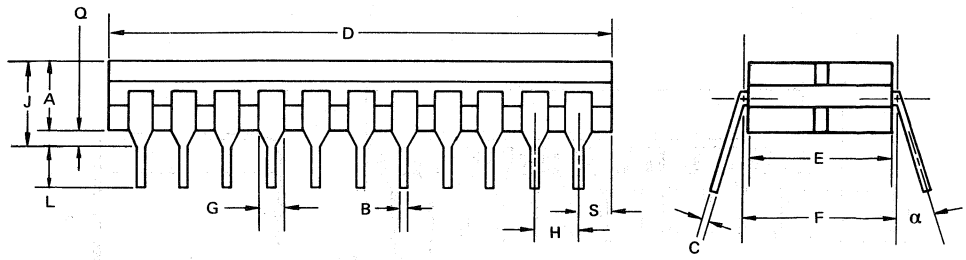
JEDEC TO-257AA
Flange-Mounted Header Family
(Peripheral Terminals)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.190	0.200	4.83	5.08	
A1	0.035	0.045	0.89	1.14	
A2	0.120 BSC		3.05 BSC		
ϕb	0.025	0.035	0.64	0.89	
D	0.645	0.665	16.38	16.89	
D1	0.410	0.430	10.41	10.92	
D2	–	0.038	–	0.97	
e	0.100 BSC		2.54 BSC		
E	0.410	0.420	16.38	16.67	
L	0.500	0.750	12.70	19.05	
L1	0.527	0.537	13.39	13.64	
ϕP	0.140	0.150	3.56	3.81	

BSC = Basic Spacing Between Centerlines

A	B	C	.300 CERAMIC DUAL-IN-LINE
		D	.400 CERAMIC DUAL-IN-LINE
	E	F	.600 CERAMIC DUAL-IN-LINE



PKG CODE	LEAD COUNT	38510 OUTLINE	DIM A	DIM B*	DIM C*	DIM D	DIM E	DIM E1	DIM B1	DIM e	DIM L	DIM Q	DIM S	DIM α
A	14	D-1	– / 0.200	0.16 / 0.018	0.008 / 0.012	0.753 / 0.785	– / 0.285	0.290 / 0.310	0.050 / 0.065	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.098	0° / 15°
B	16	D-2	– / 0.200	0.016 / 0.020	0.008 / 0.012	0.753 / 0.785	– / 0.305	0.290 / 0.320	0.050 / 0.065	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.080	0° / 15°
C	20	D-8	– / 0.200	0.016 / 0.020	0.008 / 0.012	0.940 / 0.970	0.285 / 0.305	0.300 / 0.320	0.050 / 0.065	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.080	0° / 15°
D	22	D-7	– / 0.225	0.016 / 0.020	0.008 / 0.012	1.055 / 1.085	0.375 / 0.395	0.395 / 0.420	0.050 / 0.065	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.080	0° / 15°
E	24	D-3	– / 0.225	0.016 / 0.020	0.008 / 0.012	1.240 / 1.270	0.545 / 0.535	0.595 / 0.615	0.050 / 0.065	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.098	0° / 15°
F	28	D-10	– / 0.225	0.016 / 0.020	0.008 / 0.012	1.440 / 1.470	0.545 / 0.535	0.595 / 0.615	0.050 / 0.065	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.098	0° / 15°

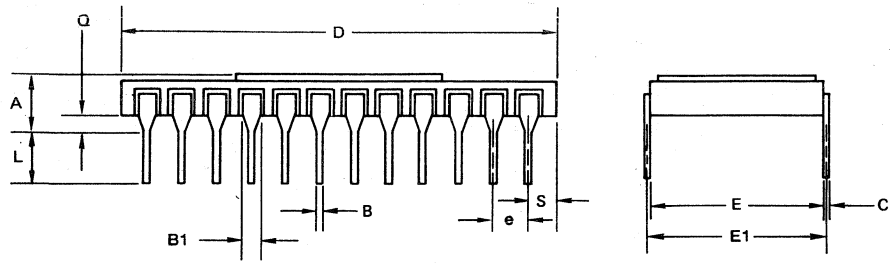
* Dimensions B and C maximum limits are increased by 0.003 for solder DIP finish.

NOTE: All Dimensions Are $\frac{\text{Min}}{\text{Max}}$. Dimensions Are In Inches.

BSC = Basic Spacing Between Centerlines

Package Configurations

G	H	I	J	.300 SIDEBRAZED CERAMIC DUAL-IN-LINE
			K	.400 SIDEBRAZED CERAMIC DUAL-IN-LINE
	L	M	N	.600 SIDEBRAZED CERAMIC DUAL-IN-LINE



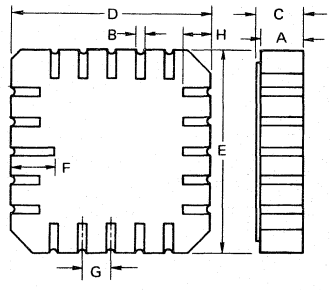
PKG CODE	LEAD COUNT	38510 OUTLINE	DIM A	DIM B*	DIM C*	DIM D	DIM E	DIM E1	DIM B1	DIM e	DIM L	DIM Q	DIM S
G	14	D-1	– / 0.150	0.016 / 0.020	0.008 / 0.012	– / 0.765	0.280 / 0.305	0.290 / 0.310	0.045 / 0.055	0.100 / BSC	-.125 / 0.180	0.015 / 0.060	– / 0.098
H	16	D-2	– / 0.150	0.016 / 0.020	0.008 / 0.012	– / 0.815	0.280 / 0.305	0.290 / 0.310	0.045 / 0.055	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.080
I	18	D-6	– / 0.150	0.016 / 0.020	0.008 / 0.012	– / 0.915	0.280 / 0.305	0.290 / 0.310	0.045 / 0.055	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.098
J	20	D-8	– / 0.150	0.016 / 0.020	0.008 / 0.012	0.990 / 1.015	0.280 / 0.305	0.290 / 0.310	0.045 / 0.055	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.080
K	22	D-7	– / 0.150	0.016 / 0.020	0.008 / 0.012	1.070 / 1.105	0.380 / 0.405	0.390 / 0.410	0.045 / 0.055	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.080
L	24	D-3	– / 0.175	0.016 / 0.020	0.008 / 0.012	1.185 / 1.215	0.580 / 0.605	0.590 / 0.610	0.045 / 0.055	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.098
M	28	D-10	– / 0.175	0.016 / 0.020	0.008 / 0.012	1.380 / 1.420	0.580 / 0.605	0.590 / 0.610	0.040 / 0.055	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.100
N	40	D-5	– / 0.175	0.016 / 0.020	0.008 / 0.012	1.980 / 2.020	0.580 / 0.605	0.590 / 0.610	0.040 / 0.055	0.100 / BSC	0.125 / 0.180	0.015 / 0.060	– / 0.098

* Dimensions B and C maximum limits are increased by 0.003 for solder DIP finish

NOTE: All Dimensions Are $\frac{\text{Min}}{\text{Max}}$. Dimensions Are In Inches.

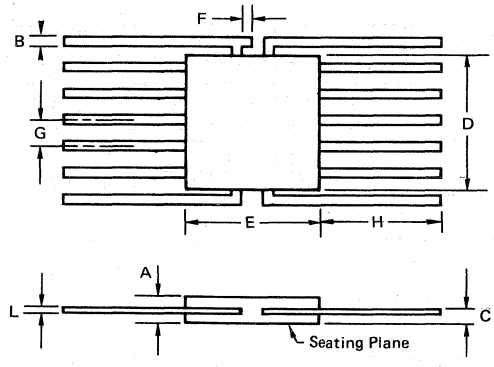
BSC = Basic Spacing Between Centerlines

O | P | Q | R | S | T — CERAMIC LEADLESS CHIP CARRIER



PKG CODE	LEAD COUNT	38510 OUTLINE	DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	DIM H
O	18	N/A	0.040 0.055	0.020 0.030	0.050 0.065	0.340 0.355	0.410 0.425	0.060 0.095	0.050 BSC	0.035 0.055
P	20	C-2	0.050 0.088	0.022 0.028	0.060 0.100	0.342 0.358	0.342 0.358	0.075 0.095	0.050 BSC	0.045 0.055
Q	24	N/A	0.045 0.090	0.017 0.023	– –	0.345 0.360	0.345 0.360	0.077 0.093	0.037 0.043	0.033 0.047
R	28	N/A	0.050 0.088	0.022 0.028	0.064 0.100	0.442 0.460	0.442 0.460	0.075 0.095	0.050 BSC	0.045 0.055
S	32	C-12	0.064 0.076	0.022 0.028	0.074 0.090	0.442 0.458	0.542 0.558	0.065 0.095	0.050 BSC	0.045 0.055
T	44	C-5	0.055 0.075	0.022 0.028	0.065 0.085	0.640 0.660	0.640 0.660	0.060 0.095	0.050 BSC	0.045 0.055

U | V | W — CERPACK*



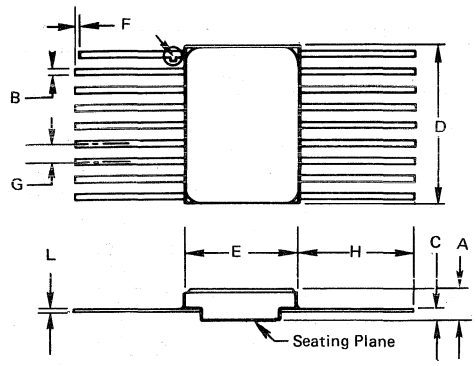
PKG CODE	LEAD COUNT	38510 OUTLINE	DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	DIM H	DIM L
U	14	N/A	– 0.070	0.016 0.019	0.020 0.030	0.240 0.280	– 0.280	0.009 0.011	0.050 BSC	0.250 0.370	0.004 0.007
V	16	N/A	– 0.070	0.017 0.019	0.020 0.030	– 0.440	0.245 0.305	0.009 0.011	0.050 BSC	0.250 0.370	0.004 0.007
W	28	N/A	– 0.070	0.017 0.019	0.020 0.030	0.495 0.525	0.370 0.400	0.009 0.011	0.050 BSC	0.270 0.300	0.004 0.007

* Actual package design may differ slightly from illustration.

NOTE: All Dimensions Are $\frac{\text{Min}}{\text{Max}}$. Dimensions Are In Inches.

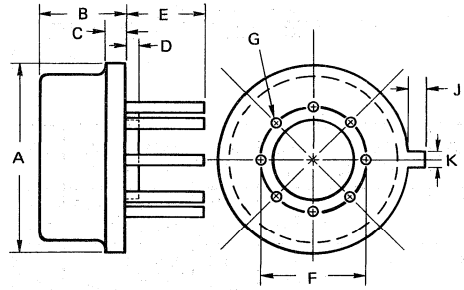
BSC = Basic Spacing Between Centerlines

X | Y | Z | AA | BB | CC | DD | EE — BRAZE, WELD SEAL FLATPACK



PKG CODE	LEAD COUNT	38510 OUTLINE	DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	DIM H	DIM L
X	14	F-2A	0.045 0.115	0.015 0.019	0.029 0.054	– 0.390	0.235 0.260	0.009 0.011	0.050 BSC	0.270 0.370	0.003 0.009
Y	16	N/A	0.070 0.085	0.015 0.019	0.014 0.030	0.380 0.400	0.280 0.300	0.009 0.011	0.050 BSC	0.280 0.320	0.004 0.007
Z	16	F-5A	0.045 0.115	0.015 0.019	0.029 0.054	– 0.440	0.245 0.285	0.009 0.011	0.050 BSC	0.250 0.370	0.003 0.009
AA	18	N/A	0.082 0.100	0.015 0.019	0.027 0.033	0.430 0.450	0.320 0.340	0.009 0.011	0.050 BSC	0.280 0.320	0.004 0.007
BB	20	F-9A	0.045 0.115	0.015 0.019	0.029 0.054	– 0.540	0.245 0.300	0.009 0.011	0.050 BSC	0.250 0.370	0.003 0.009
CC	22	N/A	0.082 0.100	0.015 0.019	0.016 0.030	0.430 0.450	0.320 0.340	0.009 0.011	0.050 BSC	0.280 0.320	0.004 0.007
DD	24	F-6A	0.090 0.110	0.015 0.019	0.030 0.051	0.590 0.610	0.395 0.405	0.009 0.011	0.050 BSC	0.255 0.275	0.004 0.007
EE	28	F-11A	0.045 0.115	0.015 0.019	0.029 0.054	– 0.740	0.460 0.520	0.009 0.011	0.050 BSC	0.250 0.370	0.003 0.009

FF — TO-99 METAL CAN

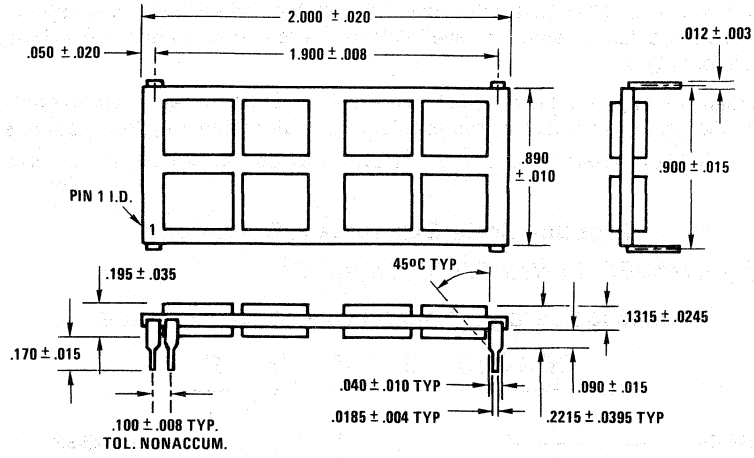


PKG CODE	LEAD COUNT	38510 OUTLINE	DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	DIM J	DIM K
CC	8	A-1	0.355 0.365	0.165 0.185	0.017 0.030	0.010 0.045	0.500 0.560	0.200 TYP	0.016 0.019	0.027 0.045	0.027 0.034

NOTE: All Dimensions Are $\frac{\text{Min}}{\text{Max}}$. Dimensions Are In Inches.

BSC = Basic Spacing Between Centerlines

HS-6564RH MODULE



Ordering Information

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Because such a broad line of product is offered by Harris you may find it necessary to contact the factory in Melbourne, Florida. Please call your factory representative if additional factory information is required.

* Product and(or) technology shipment out of the United States is subject to control by the U.S. Commerce Department and the DOD and may require a special export license.

Product Code Examples & Definitions

High Reliability CD4000-Series CMOS Logic ICs

CD4000 LOGIC STANDARD NOMENCLATURE GUIDE

CD4000 B F S R

PART NUMBER
CD4000

SERIES
A
B

PACKAGE DESIGNATOR
K: Flatpack
Q: Flatpack (Mil-M-38510 Designator "N" or "T")
F: Dual-In-Line (Mil-M-38510 Designator "C" or "E")

CLASS
S: Class S
B: Class B

HARDNESS ASSURANCE LEVEL
R: 10^5 RADs Si
H: 10^6 RADs Si

CD4000 MIL-STD-883 NOMENCLATURE GUIDE

CD4000B D MS H

PART NUMBER
CD4000B

PACKAGE DESIGNATOR
D: Dual-In-Line Metal Seal Ceramic
Q: Flatpack (38510 Outline)
K: Flatpack (Non 38510)
F: Dual-in-Line Frit-Seal Ceramic
J: Leadless Chip Carrier Ceramic

RELIABILITY SCREENING LEVEL
MS: Class S, Condition A Precap Visual and SEM Inspection
3A: Class B
3: Class B, Modified

When Used Indicates Radiation Levels

HARDNESS ASSURANCE LEVEL
R: 10^5 RADs Si
H: 10^6 RADs Si

"D" Package has a solder dipped lead finish (38510 lead finish "A")
"Q" Package has a gold plated lead finish (38510 lead finish "C")
"K" Package has a solder dipped lead finish (38510 lead finish "A")
"F" Package has a solder dipped tin plate (38510 lead finish "A")
"MS" devices are in full compliance with Mil-Std-883C, paragraph 1.2.1 when the optional Group B and Group D conformance tests are performed.

/3A and /3 product in not available in Rad-Hard versions
/3A is in full compliance with Mil-Std-883C, paragraph 1.2.1
/3 are non-compliant to Mil-Std-883, Class B and are available as special orders only

High-Reliability, Rad-Hard High Speed CMOS/SOS ICs

The HCS/HCTS CMOS/SOS Family

A Rad-Hard CMOS Alternative to Bipolar LS Logic

The HCS/HCTS parts are a new family of higher speed, low power, radiation hardened CMOS logic devices that are 20 times faster than the 4000 series. They are SOS based, and are available in a wide choice of logic functions based on the bulk high speed HC/HCT CMOS family.

CMOS/SOS structure uses a sapphire substrate to insulate the n- and p-transistors from each other. This structure is highly resistant to transient radiation, total dose radiation, and single event upsets.

CMOS/SOS technology offers superior radiation tolerance, high speed, low power, good noise immunity, and neutron resistance over the full military temperature range (-55°C to +125°C).

High reliability HCS/HCTS CMOS/SOS devices are manufactured in our continually recertified JAN Class S state-of-the-art factory to Mil-Std-883, Method 5004 standards.

HIGH SPEED CMOS/SOS LOGIC NOMENCLATURE GUIDE

HCS74 K MS R

PART NUMBER
HCS: CMOS Compatible
HCTS: TTL Compatible

PACKAGE DESIGNATOR
K: Flatpack
D: Dual-In-Line
Weld Seal Ceramic

RELIABILITY SCREENING LEVEL
MS: Class S, (Condition A, modified) Pre-Cap and SEM Inspection

HARDNESS ASSURANCE LEVEL
R: 2×10^5 RADs Si
H: 10^6 RADs Si

NOTES:
1. The "CD54" prefix is dropped for Class S HCS/HCTS device types
2. Both the "K" and "D" packages have gold plated lead finish (38510 lead finish "C")

H-Series High Reliability Rad-Hard Products

RAD-HARD HIGH RELIABILITY NOMENCLATURE GUIDE

H S 1 - 6504 RRH -8

PREFIX
H: Harris

FAMILY
S: Rad-Hard/ High-Rel Products

PACKAGE
1: Ceramic DIP
2: TO-99 Metal Can
4: Leadless Chip Carrier (LCC)
5: Ceramic Substrate
9: Flatpack

PART NUMBER

HARDNESS
RH: Radiation Hardened
RRH: SEU Immune Rad-Hard
Blank: Non-Rad-Hard

TEMPERATURE GRADE
-8: -55°C to +125°C Harris Class B Equivalent Devices*
-Q: -55°C to +125°C Harris Class S Equivalent Devices
-BXXXX: Rad-Hard/High Rel Devices - Altered to Customer Specs. B Spec Number is Uniquely Assigned to Specific Customer Requirements

* RRH devices are specified at a temperature range of -20°C to +80°C

High Reliability Rad-Hard MOSFET Semiconductor Devices

RAD-HARD MOSFET NOMENCLATURE GUIDE
FOR RAD-HARD ASSURED PROGRAM (RHAP) TACTICAL APPLICATIONS

FR X XXXX X X

RELIABILITY SCREENING LEVEL
- 1: Non TX (Commercial)
- 2: TX equivalent of Mil-S-19500
- 3: TXV equivalent of Mil-S-19500
- 4: Space equivalent of Mil-S-19500

RADIATION LEVEL ASSURANCE
- D: 10k RADs (Si) and 2×10^{12}
- *R: 100k RADs (Si) Neutrons
- *H: 1 MegaRAD (Si)

DIE DESIGNATION (N-CHANNEL)

VDSS	HEX-3	HEX-4	HEX-5	HEX-6
100V:	130	140	150	160
200V:	230	240	250	260
250V:	234	244	254	264
500V:	430	440	450	460

DIE DESIGNATION (P-CHANNEL)

VDSS	HEX-3	HEX-4	HEX-5	HEX-6
100V:	9130	9140	9150	9160
200V:	9230	9240	9250	9260
500V:	9430	9440	9450	9460

PACKAGE DESIGNATOR
- M: TO-204AA
- K: TO-204AE
- L: TO-205AF
- S: TO-257AA*
- F: TO-254AA*

RAD-HARD MOSFETs

* For strategic applications all MOSFETs 2N7271-2N7233 will be sold as JAN devices. See product line manager for additional devices

Sales Office Headquarters

UNITED STATES
Harris Semiconductor
1301 Woody Burke Road
Melbourne, Florida 32902
TEL: (407) 724-3739

EUROPE
Harris Semiconductor
Mercure Centre
Rue de la Fusee 100
Brussels, Belgium 1130
TEL: (32) 2-246-2111

SOUTH ASIA
Harris Semiconductor H.K. Ltd
13/F Fourseas Building
208-212 Nathan Road
Tsimshatsui, Kowloon
Hong Kong
TEL: (852) 3-723-6339

NORTH ASIA
Harris K.K.
Shinjuku NS Bldg. Box 6153
2-4-1 Nishi-Shinjuku
Shinjuku-Ku, Tokyo 163 Japan
TEL: 81-3-345-8911

HARRIS

RAD-HARD 16

OTHER PRODUCTS

Harris products are designed to meet the needs of military and aerospace users and are designated by the level of compliance to established military standards. These standard products are organized into the following product grades.

JAN MIL-M-38510 ICs

JAN products are fabricated, assembled, and processed completely within the United States. They are fully compliant to all requirements listed in MIL-M-38510 and MIL-STD-883 for Class B and S devices. The JAN Qualified-Parts LIst (QPL) for MIL-M-38510 devices is maintained by DESC and any changes in these specifications must be approved by DESC.

SMD ICs

Harris offers a broad range of Standard Military Drawing (SMD) products that were previously referred to as "DESC Drawings." These devices are processed in full compliance to MIL-STD-883 Class B and are tested to electrical specifications that are issued and controlled by DESC.

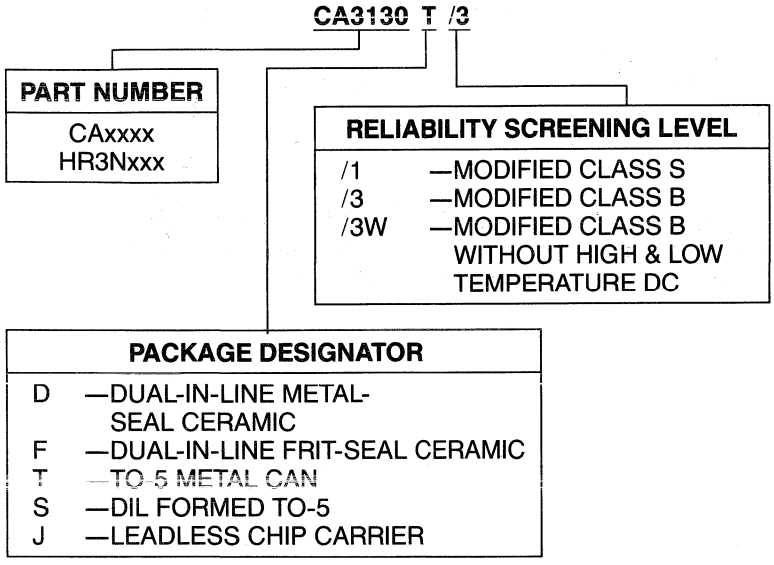
Standard Military Product ICs

Harris offers high-reliability products that are processed to Harris data-sheet requirements. These products are identified by a unique suffix depending on the product type, and may be fully compliant to MIL-STD-883 or MIL-STD "equivalent" product for Class B or S type applications.

CA3000-Series ICs

The CAXXXX "Slash" (/) Series types are high-reliability linear integrated circuits intended for applications in aerospace, military, and industrial equipment. These devices are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for high-reliability microcircuit devices.

CA3000 LINEAR SERIES NOMENCLATURE GUIDE



1—Slash 1 (/1) device options are available as follows upon special request: SEM, PIND testing, Condition A visual and Conformance B, C & D tests.

2—Dual Gate FETS are in TO-72 packages.

3—CA3089F is screened to commercial limits only.

MIL-STD-883 CD4000-Series CMOS Logic ICs

The high-reliability CD4000B series of high-voltage CMOS integrated circuits consists of a broad range of SSI, MSI-1, and MSI-2 (LSI) functions from simple gates to complex counters, registers, and arithmetic circuits. Specific design features for CMOS devices and the performance advantages of CMOS technology — low power consumption, high noise immunity, high speed, high fanout, TTL and DTL logic compatibility, excellent temperature stability, and fully protected inputs and outputs — provide the logic system designer with a capability to achieve outstanding performance, high reliability, and simplified circuitry in a wide variety of equipment designs.

High-reliability CD4000 series parts are in full compliance with MIL-STD-883C, Paragraph 1.2.1. Two different types of product are provided to meet the requirements of this paragraph, Class S and Class B.

Slash MS (.../MS) meets Class S requirements when the optional group B life conformances test is performed.

Slash 3A (.../3A) meets Class B requirements.

The high-reliability CD4000 series also include parts that meet the requirements of MIL-STD-883C, Paragraph 1.2.2 (non compliant). This family of parts has the following designation.

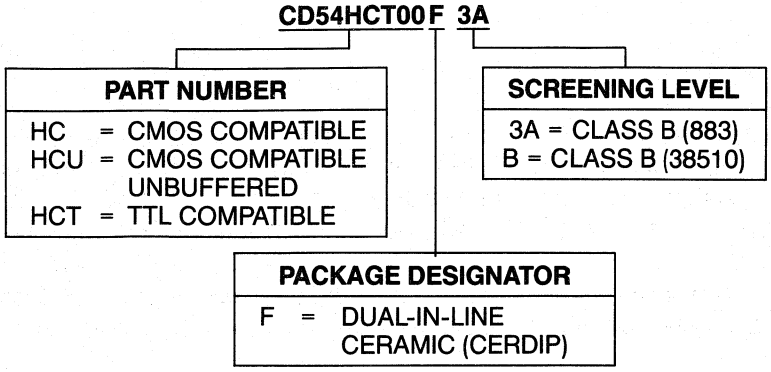
Slash 3 (.../3) meets most of the requirements of a Class B part.

MIL-STD-883 CD54HC/HCT-Series High-Speed CMOS ICs

The 54HC/HCT series of high speed CMOS logic integrated circuits include an extensive line of products that are pin compatible with many existing bipolar 54LSTTL and CMOS 4000 series of digital logic types. The new 54HC/HCT IC's provide high-speed CMOS replacements for the most popular LSTTL devices in existing designs and also offer low-power all-CMOS designs for new digital systems.

The 54HC/HCT high-reliability product line consists primarily of CD54HC-series types, which feature CMOS input-voltage-level compatibility, and CD54HCT-series types, which are input-voltage-level compatible with LSTTL devices. The 54HC/HCT high-reliability line also includes a limited number of single-stage, unbuffered inverter types (CD54HCU-series) for added versatility in oscillator and amplifier applications.

CD54HC/HCT NOMENCLATURE GUIDE



NOTE 1 — 3A is 883 Revision C full compliant, Para 1.2.1.

NOTE 2 — 3A devices are dual marked with the SMD/DESC drawing or standard military drawing.

NOTE 3 — B is JAN38510 Class B Device.

The ACL Family—A Lower-Power Alternative to the Power-Hungry FAST* and AS Bipolar TTL Logic

MIL-STD-883 CD54AC/ACT-Series Advanced CMOS Logic (ACL) ICs

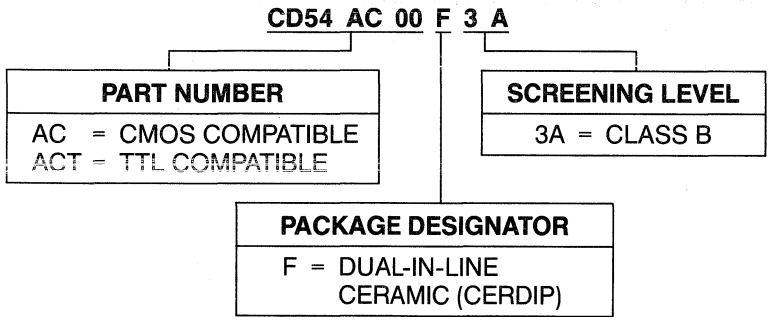
The CD54AC/ACT Advanced CMOS Logic (ACL) ICs include a broad range of MSI and LSI functions from simple gates to complex counters, registers, and arithmetic circuits. These CMOS ICs, featuring 3-ns gate propagation delays, the fastest CMOS logic yet available, match Fairchild's FAST* devices in speed, performance, and logic-type output drive, but at CMOS power levels. Output device capability is 24 milli ampers.

A number of high-reliability 3A fully compliant product are now available together with an ever-increasing number of these types in the Standard Military Drawing format.

*Trademark Fairchild Semiconductor Corp.

V

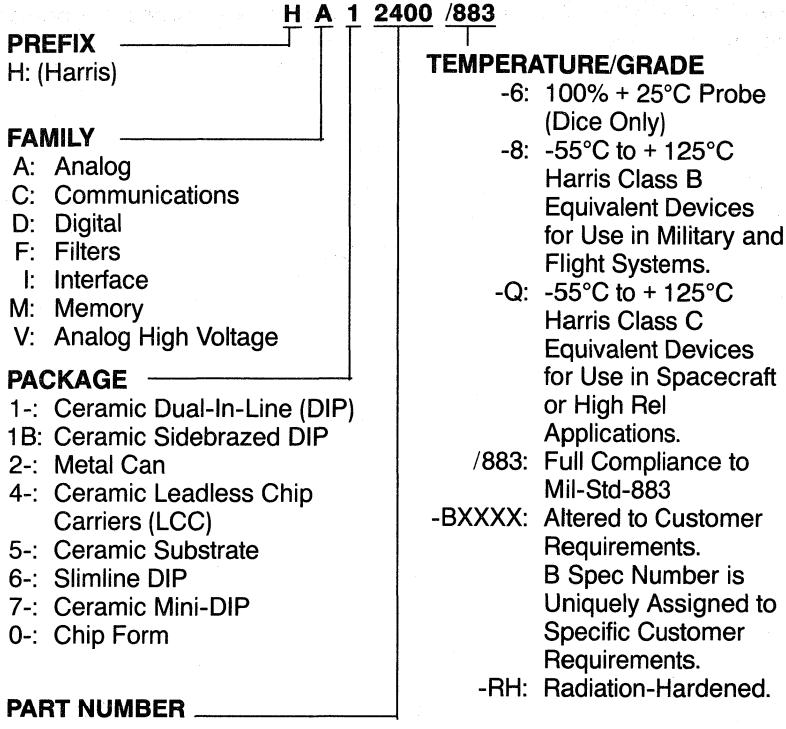
ADVANCED CMOS LOGIC NOMENCLATURE GUIDE



NOTE 1 — 3A devices are dual marked with the DESC or Standard Military Drawing.

"H" SERIES NOMENCLATURE GUIDE

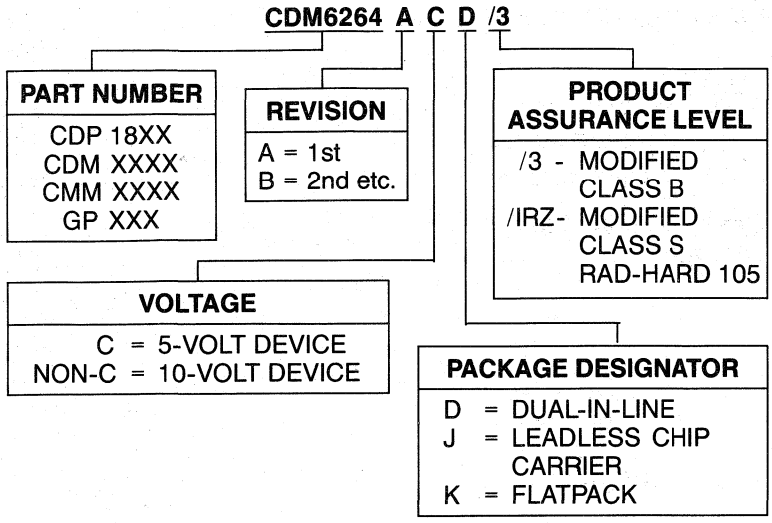
Harris products are designated by "Harris Product Code." These products will always begin with the letter "H" and specific device numbers are isolated by hyphens. An example product code is shown below. When ordering, please refer to products by the full code identification.



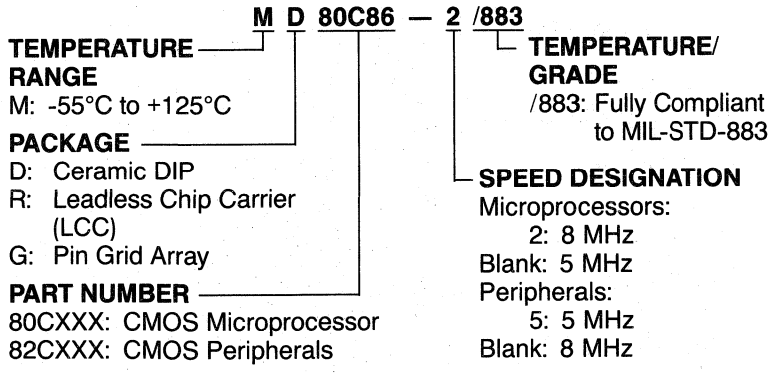
High Reliability CMOS Microprocessors, Memories and Peripherals

The high-reliability slash-series of CMOS LSI microprocessors, memories and peripherals are ideally suited for military applications such as mobile ground equipment that must be battery operated and exposed to harsh environments. Use of a highly reliable all CMOS LSI technology provides low power operation throughout the military temperature range.

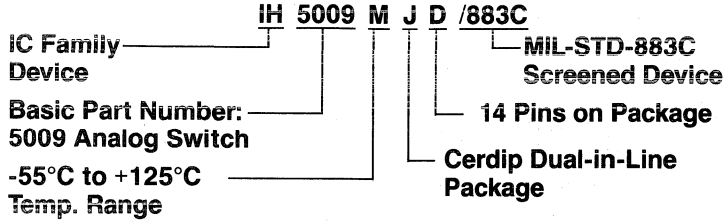
CDM, CDP, CMM, GP CMOS LSI NOMENCLATURE GUIDES



80CXX FAMILY NOMENCLATURE GUIDE



I-SERIES NOMENCLATURE GUIDE



Package Type Designators

A — TO-237
C — TO-220
D — Ceramic Sidebrazed Dual-in-Line
E — Small TO-8
F — Ceramic Flat Pack
H — TO-66
I — 16 Pin (.6 x .7 Pin Spacing) Hermetic Hybrid Dip
J — CERDIP Dual-In-Line
K — TO-3
L — Leadless Ceramic
S — TO-52
T — TO-5 Type (also TO-78, TO-99, TO-100)
U — TO-72 Type (also TO-18, TO-71)
V — TO-39
Z — TO-92

*Exceptions To Package Type Designators

DG SERIES

A — 10 Pin Metal Can
L — 14 Pin Flatpack
P — Ceramic DIP (Special Order Only)
K — CERDIP

AD SERIES

H — TO-52
D — CERDIP, Ceramic DIP
R — TO-92

Pin Count Designator

A — 8
B — 10
C — 12
D — 14
E — 16
F — 22
G — 24
H — 42
I — 28
J — 32
K — 35
L — 40
M — 48
N — 18
P — 20
Q — 2
R — 3
S — 4
T — 6
U — 7
V — 8 (0.200″ Pin Circle Isolated Case)
W — 10 (0.230″ Pin Circle Isolated Case)
Y — 8 (0.200″ Pin Circle Case to Pin 4)
Z — 10 (0.230″ Pin Circle Case to Pin 5)

*Exceptions To Pin Count Designators

DG SERIES

A — 10 Pin Metal Can
L — 14 Pin Flatpack
P — Ceramic DIP (Special Order Only)
K — CERDIP

AD SERIES

D — 20, 18, 16 or 14
H — 3 Pin
N — 20, 18, 16 or 14

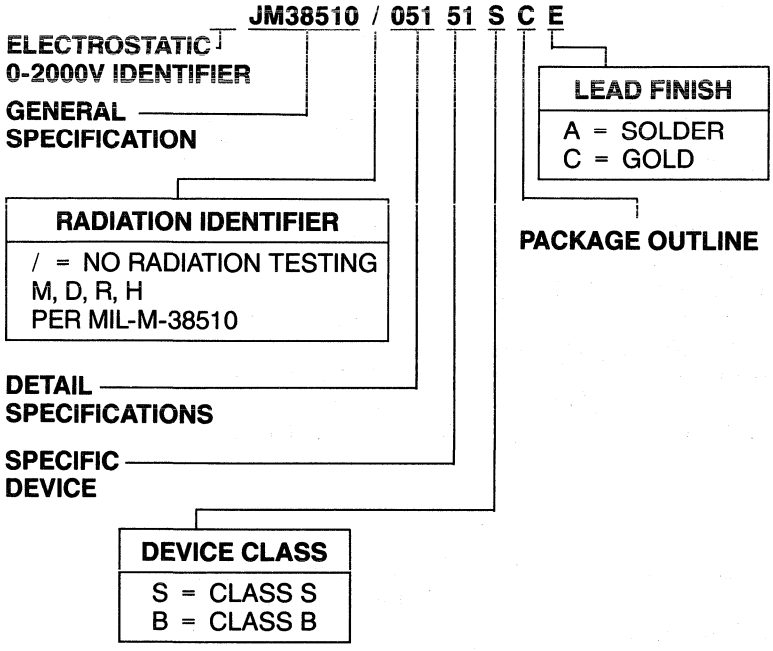
High Reliability Designator

JM38510/XXXXX-XXX — Mil-M-38510 Device
/883C — Mil-STD-883C Screened Device
/HR — High Reliability Device
/BR — Cost Effective High Reliability Device
/BI — Burn-In Only Process Flow

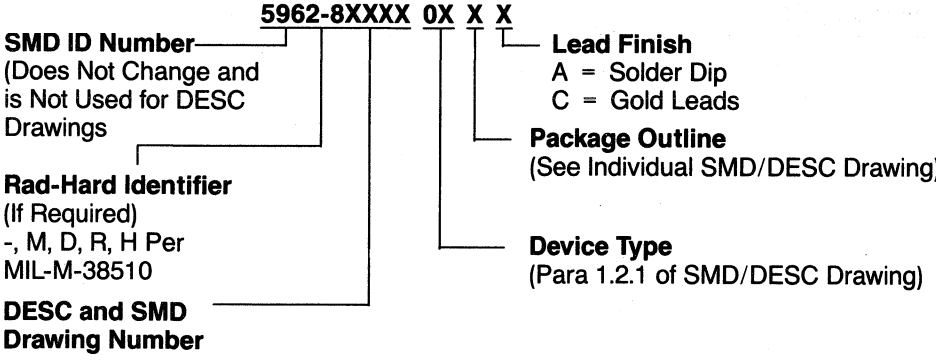
Temperature Range Designators

M — Military -55°C to +125°C

JAN 38510 NOMENCLATURE GUIDE



SMD/DESC NOMENCLATURE GUIDE



Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
2N3439	350V/1A, N-P-N	MIL-S-19500/368	
2N3440	250V/1A, N-P-N	MIL-S-19500/368	
2N3584	250V/2A, N-P-N	MIL-S-19500/384	
2N3585	300V/2A, N-P-N	MIL-S-19500/384	
2N3879	75V/7A, N-P-N hi-speed	MIL-S-19500/526	
2N5038	90V/20A, N-P-N hi-speed	MIL-S-19500/439	
2N5039	75V/20A, N-P-N	MIL-S-19500/439	
2N5302	60V/30A, N-P-N	MIL-S-19500/456	
2N5303	80V/30A, N-P-N	MIL-S-19500/456	
2N5415S	-200V/-1A, P-N-P	MIL-S-19500/485	
2N5416S	-300V/-1A, P-N-P	MIL-S-19500/485	
2N5671	90V/30A, N-P-N	MIL-S-19500/488	
2N5672	120V/30A, N-P-N hi-speed	MIL-S-19500/488	
2N6032	90V/50A, N-P-N	MIL-S-19500/528	
2N6033	120V/50A, N-P-N	MIL-S-19500/528	
2N6211	-275V/-2A, P-N-P	MIL-S-19500/461	
2N6212	-300V/-2A, P-N-P	MIL-S-19500/461	
2N6213	-350V/-2A, P-N-P	MIL-S-19500/461	
2N6283	80V/20A, N-P-N	MIL-S-19500/504	
2N6284	100V/20A, N-P-N	MIL-S-19500/504	
2N6286	80V/-20A, P-N-P	MIL-S-19500/505	
2N6287	-100V/-20A, P-N-P	MIL-S-19500/505	
2N6306	250V/8A, N-P-N	MIL-S-19500/498	
2N6308	350V/8A, N-P-N	MIL-S-19500/498	
2N6383	40V/10A, N-P-N	MIL-S-19500/523	
2N6384	60V/10A, N-P-N	MIL-S-19500/523	
2N6385	80V/10A, N-P-N	MIL-S-19500/523	
2N6546	300V/15A, N-P-N	MIL-S-19500/525	
2N6547	400V/15A, N-P-N	MIL-S-19500/525	
2N6648	-40V/-10A, P-N-P	MIL-S-19500/527	
2N6649	-60V/-10A, P-N-P	MIL-S-19500/527	
2N6650	-80V/-10A, P-N-P	MIL-S-19500/527	
2N6671	300V/10A, N-P-N hi-speed	MIL-S-19500/536	
2N6673	400V/8A, N-P-N hi-speed	MIL-S-19500/536	
2N6674	300V/20A, N-P-N hi-speed	MIL-S-19500/537	
2N6675	400V/20A, N-P-N hi-speed	MIL-S-19500/537	
2N6676	300V/20A, N-P-N hi-speed	MIL-S-19500/538	
2N6678	400V/20A, N-P-N hi-speed	MIL-S-19500/538	
2N6688	200V/20A, N-P-N hi-speed		
2N6756	100V/14A, N-CH MOSFET	MIL-S-19500/542A	

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
2N6758	200V/9A, N-CH MOSFET	MIL-S-19500/542A	
2N6760	400V/5.5A, N-CH MOSFET	MIL-S-19500/542A	
2N6762	500V/4.5A, N-CH MOSFET	MIL-S-19500/542A	
2N6764	100V/38A, N-CH MOSFET	MIL-S-19500/543A	
2N6766	200V/30A, N-CH MOSFET	MIL-S-19500/543A	
2N6768	400V/14A, N-CH MOSFET	MIL-S-19500/543A	
2N6770	500V/12A, N-CH MOSFET	MIL-S-19500/543A	
2N6782	100V/3.5A, N-CH MOSFET	MIL-S-19500/556	
2N6784	200V/2.25A, N-CH MOSFET	MIL-S-19500/556	
2N6786	400V/1.25A N-CH MOSFET	MIL-S-19500/556	
2N6788	100V/6A, N-CH MOSFET	MIL-S-19500/555	
2N6790	200V/3.5A, N-CH MOSFET	MIL-S-19500/555	
2N6792	400V/2A, N-CH MOSFET	MIL-S-19500/555	
2N6794	500V/1.5A, N-CH MOSFET	MIL-S-19500/555	
2N6796	100V/8A, N-CH MOSFET	MIL-S-19500/557	
2N6798	100V/5.5A, N-CH MOSFET	MIL-S-19500/557	
2N6800	400V/3A, N-CH MOSFET	MIL-S-19500/557	
2N6802	500V/2.5A, N-CH MOSFET	MIL-S-19500/557	
2N6849	100V/6.5A, P-CH MOSFET	MIL-S-19500/563	
2N6851	200V/4A, P-CH MOSFET	MIL-S-19500/563	
2N6895	100V/1.5A, P-CH MOSFET	MIL-S-19500/565	
2N6896	100V/6A, P-CH MOSFET	MIL-S-19500/565	
2N6897	100V/12A, P-CH MOSFET	MIL-S-19500/565	
2N6898	100V/25A, P-CH MOSFET	MIL-S-19500/565	
2N6901	100V/1.5A, N-CH MOSFET	MIL-S-19500/566	
2N6902	100V/-12A, N-CH MOSFET	MIL-S-19500/566	

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
2N6903	200V/1.5A, N-CH MOSFET	MIL-S-19500/566	
2N6904	200V/-8A, N-CH MOSFET	MIL-S-19500/566	
2N6966	100V/15A N-CH MOSFET	MIL-S-19500/569	
2N6967	200V/13A N-CH MOSFET	MIL-S-19500/569	
2N6968	400V/7.5A N-CH MOSFET	MIL-S-19500/569	
2N6969	500V/6A N-CH MOSFET	MIL-S-19500/569	
2N7119	100V/14A, N-CH MOSFET		89009
2N7120	200V/9A, N-CH MOSFET		89009
2N7121	400V/5.5A, N-CH MOSFET		89009
2N7122	500V/4.5A, N-CH MOSFET		89009
2N7123	100V/40A, N-CH MOSFET		89007
2N7124	200V/30A, N-CH MOSFET		89007
2N7125	400V/15A, N-CH MOSFET		89007
2N7126	500V/13A, N-CH MOSFET		89007
2N7142	60V/12A, N-P-N hi-speed	MIL-S-19500/TBD	
2N7143	80V/12A, N-P-N hi-speed	MIL-S-19500/TBD	
2N7144	60V/12A, N-P-N hi-speed	MIL-S-19500/TBD	
2N7145	80V/12A, N-P-N hi-speed	MIL-S-19500/TBD	
2N7146	60V/12A, N-P-N hi-speed	MIL-S-19500/TBD	
2N7147	80V/12A, N-P-N hi-speed	MIL-S-19500/TBD	
2N7224	100V/30A, N-CH MOSFET		89026
2N7225	200V/27A, N-CH MOSFET		89026
2N7226	400V/14A, N-CH MOSFET		89026
2N7227	500V/12A, N-CH MOSFET		89026
2N7241	100V/14A, N-CH MOSFET		89025
2N7242	200V/9A, N-CH MOSFET		89025

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
2N7243	400V/5.5A, N-CH MOSFET		89025
2N7244	500V/4.5A, N-CH MOSFET		89025
AD7520UD	CMOS 10-bit multiplying D/A	MIL-M-38510/12702	
AD7521UD	CMOS 10-bit multiplying D/A	MIL-M-38510/12703	
AD7541TD	CMOS 12-bit multiplying D/A	MIL-M-38510/12704	
CA0723	Voltage regulator		
CA0741	Amplifier		
CA0747	Amplifier		
CA0748	Amplifier		
CA1558	Amplifier		
CA3001	DC amplifier		
CA3003	DC amplifier		
CA3015	Wideband amplifier		
CA3018	Transistor array		
CA3020	Wideband power amplifier		
CA3028	Differential/cascade amplifier		
CA3045	Transistor array		
CA3049	Dual hi-freq diff amp		
CA3058	Zero voltage switch		
CA3060B	Triple transconductance amp		
CA3080	Single transconductance amp		
CA3081	Transistor common emitter array		
CA3082	Transistor common collector array		
CA3083	Transistor array		
CA3085	Positive voltage regulator		
CA3089	FM IF system		
CA3094A	Power switch amplifier		
CA3100	Wideband operational amp		
CA3130	Wideband operational amp		
CA3140	Wideband operational amp		
CA3160	Wideband operational amp		
CA3260	Wideband dual amp		
CA3280	Dual variable op. amp		
CA3290	BiMOS voltage comparator		
CA6741	CA0741 & popcorn test		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CA30153	Wideband amplifier		
CA30191	Diode array		
CA30193	Diode array		
CA30261	Differential amplifier		
CA30263	Differential amplifier		
CA30391	Diode array		
CA30393	Diode array		
CA30451	Transistor array		
CA3078A	Micropower op amp		
CD4000A	Dual 3 input NOR gate plus inverter	MIL-M-38510/05201	
CD4000B	Dual 3 input NOR gate plus inverter	MIL-M-38510/05251	
CD4000UB	Dual 3 input NOR gate plus inverter		
CD4001A	Quad 2 input NOR gate	MIL-M-38510/05202	
CD4001B	Quad 2 input NOR gate	MIL-M-38510/05252	
CD4001UB	Quad 2 input NOR gate		
CD4002A	Dual 4 input NOR gate	MIL-M-38510/05203	
CD4002B	Dual 4 input NOR gate	MIL-M-38510/05253	
CD4002UB	Dual 4 input NOR gate		
CD4006A	18 stage static shift register	MIL-M-38510/05701	
CD4006B	18 stage static shift register	MIL-M-38510/05751	
CD4007A	Dual complementary pair plus inverter	MIL-M-38510/05301	
CD4007UB	Dual complementary pair plus inverter	MIL-M-38510/05351	
CD4008B	4 bit full adder with parallet carry out.	MIL-M-38510/05451	
CD4009UB	Hex buffer/converter (inverting)		
CD4010B	Hex buffer/converter (Non Inverting)		
CD4011A	Quad 2-input NAND gate	MIL-M-38510/05001	
CD4011B	Quad 2-input NAND gate	MIL-M-38510/05051	
CD4011UB	Quad 2-input NAND gate		
CD4012A	Dual 4-input NAND gate	MIL-M-38510/05002	
CD4012B	Dual 4-input NAND gate	MIL-M-38510/05052	
CD4012UB	Dual 4-input NAND gate		
CD4013A	Dual "D" flip-flops with set/reset capability	MIL-M-38510/05101	
CD4013B	Dual "D" flip-flops with set/reset capability	MIL-M-38510/05151	
CD40147B	10-Line to 4-line BCD priority encoder		
CD4014A	8-stage static shift register	MIL-M-38510/05702	

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD4014B	8-stage static shift register	MIL-M-38510/05752	
CD4015A	Dual 4 stage static shift register	MIL-M-38510/05703	
CD4015B	Dual 4 stage static shift register	MIL-M-38510/05753	
CD4016A	Quad bilateral switch		
CD4016B	Quad bilateral switch		9064002EA
CD4017A	Decode Counter/divider	MIL-M-38510/05601	
CD4017B	Decode Counter/divider	MIL-M-38510/05651	
CD4018A	Presettable divide by "N" counter		
CD4018B	Presettable divide by "N" counter	MIL-M-38510/05652	
CD4019A	Quad AND/OR select gate	MIL-M-38510/05302	
CD4019B	Quad AND/OR select gate	MIL-M-38510/05352	
CD4020A	14-stage binary ripple counter	MIL-M-38510/05603	
CD4020B	14-stage binary ripple counter	MIL-M-38510/05653	
CD4021A	8-stage static shift register	MIL-M-38510/05704	
CD4021B	8-stage static shift register	MIL-M-38510/05754	
CD4022A	Divide-by-8 counter/ divider	MIL-M-38510/05604	
CD4022B	Divide-by-8 counter/ divider	MIL-M-38510/05654	
CD4023A	Triple 3-input NAND gate	MIL-M-38510/05003	
CD4023B	Triple 3-input NAND gate	MIL-M-38510/05053	
CD4023UB	Triple 3-input NAND gate		
CD4024A	7-stage binary ripple counter	MIL-M-38510/05605	
CD4024B	7-stage binary ripple counter	MIL-M-38510/05655	
CD4025A	Triple 3-input NOR gate	MIL-M-38510/05204	
CD4025B	Triple 3-input NOR gate	MIL-M-38510/05254	
CD4025UB	Triple 3-input NOR gate		
CD4026A	Decade counter/divider		
CD4026B	Decade counter/divider		
CD4027A	Dual "J-K" flip-flop with set/reset capability	MIL-M-38510/05102	
CD4027B	Dual "J-K" flip-flop with set/reset capability	MIL-M-38510/05152	
CD4028A	BCD-to-decimal decoder	MIL-M-38510/05901	

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD4028B	BCD-to-decimal decoder	MIL-M-38510/05951	
CD4029A	Presettable up/down counter		
CD4029B	Presettable up/down counter		8101601EA
CD4030A	Quad exclusive-OR gate		
CD4030B	Quad exclusive-OR gate	MIL-M-38510/05353	
CD4031A	64-stage static shift register	MIL-M-38510/05705	
CD4031B	64-stage static shift register		
CD4033B	Decade counter/divider		
CD4034B	8-Stage static shift register	MIL-M-38510/05756	
CD4035B	4-Stage parallel in/ parallel out shift register		8101701EA
CD4040A	12-stage binary ripple counter		
CD4040B	12-stage binary ripple counter		
CD4041A	Quad true/complement buffer		
CD4041UB	Quad true/complement buffer	MIL-M-38510/05555	
CD4042A	Quad clocked "D" latch		
CD4042B	Quad clocked "D" latch		
CD4043A	Quad NOR R/S latch (3-state outputs)		
CD4043B	Quad NOR R/S latch (3-state outputs)		
CD4044A	Quad NAND R/S latch (3-state outputs)		
CD4044B	Quad NAND R/S latch (3-state outputs)		
CD4046A	Micropower phase-locked loop		
CD4046B	Micropower phase locked loop		
CD4047B	Monostable/A-stable multivibrator		8102001CA
CD4048A	Multifunctional expand-able 8-input gate		
CD4048B	Multifunctional expand-able 8-input gate		
CD4049A	Hex buffer/converter (inverting)	MIL-M-38510/05503	
CD4049UB	Hex buffer/converter (inverting)	MIL-M-38510/05553	
CD4050A	Hex buffer/converter (non-inverting)	MIL-M-38510/05504	

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD4050B	Hex buffer/converter (non-inverting)	MIL-M-38510/05554	
CD4051B	8 channel analog multiplexer/ demultiplexer		
CD4052B	4 channel analog multiplexer/ demultiplexer		7901501EA
CD4053B	Triple 2-channel anlog multiplexer demultiplexer		8101801EA
CD4054B	4-segment display driver		
CD4055B	BCD-to-7-segment decoder/driver with "display frequency" output		
CD4056B	BCD-to-7-segement decoder driver with strobed-latch function		
CD4059A	Programmable divide-by-"N" counter		
CD4060A	14-stage binary ripple counter/divider and oscillator		
CD4060B	14-stage binary ripple counter/divider and oscillator		
CD4063B	4-bit magnitude comparator		
CD4066A	Quad bilateral switch		
CD4066B	Quad bilateral switch	MIL-M-38510/05852	
CD4067B	16 channel analog multiplexers/ demultiplexers		
CD4068B	8-input NAND/AND gate		
CD4069UB	Hex inverter	MIL-M-38510/17401	
CD4070B	Quad exclusive-OR gate	MIL-M-38510/17203	
CD4071B	Quad 2-input OR gate	MIL-M-38510/17101	
CD4072B	Dual 4-input OR gate	MIL-M-38510/17102	
CD4073B	Triple 3-input AND gate	MIL-M-38510/17003	
CD4075B	Triple 3-input OR gate	MIL-M-38510/17103	
CD4076B	4-bit "D" flip-flop (3-state outputs)		
CD4077B	Quad exclusive-NOR GATE	MIL-M-38510/17204	
CD4078B	8-bit NOR/OR gate		7704402CA
CD4081B	Quad 2-input AND gate	MIL-M-38510/17001	
CD4082B	Dual 4-input AND gate	MIL-M-38510/17002	
CD4085B	Dual 2-wide, 2-input AND/OR/INVERT (AOI) gate	MIL-M-38510/17201	

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD4086B	Expandable 4-wide, 2-input AND/OR INVERT (AOI) gate	MIL-M-38510/17202	
CD4089B	Binary rate multiplier		
CD4093B	Quad 2-input NAND Schmitt Trigger		7704602CA
CD4094B	8-stage shift-and-store bus register		7702501EA
CD4095B	Gated "J-K" flip-flop (non-inverting)		
CD4096B	Gated "J-K" flip-flop (inverting and non-inverting)		
CD4097B	8 channel analog multiplexer/ demultiplexer		
CD4098B	Dual monostable multivibrator	MIL-M-38510/17504	
CD4099B	8-bit addressable latch	MIL-M-38510/17601	
CD4502B	Strobed hex inverter/ buffer	MIL-M-38510/17403	
CD4503B	Hex buffer (non-inverting)		
CD4508B	Dual 4-bit latch		
CD4510B	Presettable 4-bit BCD up/down counter		
CD4511B	BCD-to-7-segment latch decoder/driver		
CD4512B	8 channel data selector (3-state output)		
CD4514B	4-Bit latch/4-to-16-line decoder (outputs low)		
CD4515B	4-Bit latch/4-to-16-line decoder (outputs low)		7703201JA
CD4516B	Presettable 4-bit binary up/down counter		
CD4517B	Dual 64-bit shift register		
CD4518B	Dual BCD up counter		
CD4520B	Dual binary up counter		7702301EA
CD4527B	BCD rate multiplier		
CD4532B	8-Input priority encoder		
CD4536B	Programmable timer		
CD4538B	Dual precision monostable multivibrator		9055701EA
CD4541B	CMOS programmable timer		
CD4543B	CMOS BCD-to-7-segment latch/decoder/ driver for liquid-crystal displays		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD4555B	Dual 1-of-4 decoder/ demultiplexer (outputs high)		7704701EA
CD4556B	Dual 1-of-4 decoder/ demultiplexer (outputs low)		7704801EA
CD4585B	4-Bit magnitude comparator		7703701EA
CD4724B	8-Bit addressable latch		
CD40100B	32-bit left/right shift register		
CD40101B	9-bit parity generator/ checker		
CD40102B	Presettable 2-decade BCD down counter		
CD40103B	Presettable 8-bit binary down counter		
CD40104B	4-bit bidirectional universal shift register		
CD40105B	4-bit x 16 word FiFo buffer register		
CD40106B	Hex Schmitt Trigger		
CD40107B	Dual 2-input NAND buffer/driver		
CD40108B	4 x 4 multiport register		
CD40109B	Quad low-to-high voltage interface	MIL-M-38510/17404	
CD40110B	Decade up-down counter/decoder/latch/ display driver		
CD40116B	CMOS high-speed 8-bit bidirectional CMOS/TTL interface level converter		
CD40160B	Decade counter with synchronous clear		
CD40161B	Binary counter with asynchronous clear		
CD40162B	Decade counter with synchronous clear		
CD40163B	Binary counter with synchronous clear		
CD40174B	Hex "D" flip-flop		
CD40175B	CMOS Quad D-type flip-flop		
CD40181B	4-bit arithmetic logic unit		
CD40182B	Look-ahead-carry block		
CD40192B	Presettable 4-bit BDC up/down counter		
CD40193B	Presettable 4-bit binary up/down counter		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD40194B	4-Bit bidirectional universal shift register		
CD40208B	4 x 4 multiport register		
CD40257B	Quad 2-line-to-1-line data selector	MIL-M-38510/17803	
CD54AC/ACT00	Quad 2-input NAND gate		5962-8754901CA 5962-8769901CA
CD54AC/ACT02	Quad 2-input NOR gate		
CD54AC/ACT04	Hex inverter buffer		5962-8760901CA
CD54AC/ACT05	Hex inverter/buffer with open-drain outputs		
CD54AC/ACT08	Quad 2-input AND gate		5962-8761501CA
CD54AC/ACT10	Triple 3-input NAND gate		
CD54AC/ACT20	Dual 4-input NAND gate		
CD54AC/ACT32	Quad 2-input OR gate		5962-8761401CA
CD54AC/ACT74F	Dual D flip-flop w/set and reset		5962-8852001CA 5962-8752501CA
CD54AC/ACT112	Dual J-K flip-flop w/set and reset		
CD54AC/ACT138	3-to-8 line decoder/ demultiplexer, inverting		5962-8762201EA
CD54AC/ACT139	Dual 2-of-4 line decoder/demultiplexer		5962-8762301EA 5962-8755301EA
CD54AC/ACT151	8-input multiplexer		
CD54AC/ACT153	Dual 4-input multiplexer		
CD54AC/ACT157	Quad 2-input multiplexer		
CD54AC/ACT158	Quad 2-input multiplexer, inverting		
CD54AC/ACT161	Synchronous 4-bit binary counter, asynchronous reset		
CD54AC/ACT163	Synchronous 4-bit binary counter, synchronous reset		
CD54AC/ACT164	8-bit serial-in parallel-out shift register		
CD54AC/ACT174	Hex D-type flip-flop w/reset		5962-8762601EA 5962-8775701EA
CD54AC/ACT191	Synchronous 4-bit binary up/down counter		
CD54AC/ACT193	Synchronous 4-bit binary up/down counter		
CD54AC/ACT238	3-to-8 line decoder/ demultiplexer		
CD54AC/ACT240	Octal buffer line driver, 3-state, inverting		5962-8755001RA 5962-8775901RA
CD54AC/ACT241	Octal buffer line driver, 3-state		5962-8755101RA
CD54AC/ACT244	Octal buffer line driver, 3-state		5962-8755201RA 5962-8776001RA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD54AC/ACT245	Octal-bus transceiver, 3-state		5962-8775801RA 5962-8766301RA
CD54AC/ACT251	8-input multiplexer, 3-state		
CD54AC/ACT253	Dual 4-input multiplexer, 3-state		
CD54AC/ACT257	Quad 2-input multiplexer, 3-state		
CD54AC/ACT258	Quad 2-line to 4-line data selector		
CD54AC/ACT273	Octal D-type flip-flop w/reset		5962-8775601RA 5962-8755501RA
CD54AC/ACT280	8-bit odd/even parity generator/checker		
CD54AC/ACT283	4-bit full adder w/fast carry		
CD54AC/ACT299	8-bit universal shift register, 3-state		
CD54AC/ACT323	8-bit universal shift register, 3-state, (with synchronous reset)		
CD54AC/ACT373	Octal D-type flip-flop, 3-state		
CD54AC/ACT374	Octal D flip-flop, 3-state		5962-8769401RA
CD54AC/ACT533	Octal transparent latch, 3-state, inverting		
CD54AC/ACT534	Octal D flip-flop, 3-state, inverting		
CD54AC/ACT540	Octal buffer line driver, 3-state, inverting		5962-8769501RA
CD54AC/ACT541	Octal buffer line driver, 3-state		
CD54AC/ACT563	Octal inverting transparent latch, 3-state		
CD54AC/ACT564	Octal D-type flip-flop, 3-state inverting		
CD54AC/ACT573	Octal transparent latch, 3-state		
CD54AC/ACT574	Octal D-type flip-flop, 3-state		
CD54AC/ACT623	Octal bus transceiver 3-state		5962-8752501CA
CD54AC/ACT86F	Quad 2-input exclusive-OR gate		
CD54HC/HCT00	Quad 2-input NAND gate	MIL-M-38510/65001	8403701CA 5962-8683101CX
CD54HC/HCT02	Quad 2-input NOR gate	MIL-M-38510/65101	8404101CA 5962-8995101EA
CD54HC/HCT03	Quad 2-input NAND gate with open collector		5962-8764701CA
CD54HC/HCT04	Hex inverter	MIL-M-38510/65701	8409801CA 5962-89704701CA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD54HC/HCT08	Quad 2-input AND gate	MIL-M-38510/65203	8404701CA 5962-8688301CX
CD54HC/HCT10	Triple 3-input NAND gate	MIL-M-38510/65002	8403801CA 5962-8984301CA
CD54HC/HCT11	Triple 3-input AND gate		8404801CA 5962-8970901CA
CD54HC/HCT14	Hex inverting Schmitt Trigger		8409101CA 5962-8689001EX
CD54HC/HCT20	Dual 4-input NAND gate		8403901CA
CD54HC/HCT21	Dual 4-input AND gate		5962-8857601CA
CD54HC/HCT27	Triple 3-input NOR gate		8404201CA 5962-8970301CA
CD54HC/HCT30	8-input NAND gate		8404001CA 5962-894601CA
CD54HC/HCT32	Quad 2-input OR gate	MIL-M-38510/65201	8404501CA 5962-8685201CX
CD54HC/HCT42	BCD-to-decimal decoder (1-to-10)		5962-868210EA
CD54HC/HCT73	Dual J-K flip-flop w/reset		5962-8515301CA
CD54HC/HCT74	Dual D flip-flop w/set and reset		8405601CA 5962-8685301CX
CD54HC/HCT75	Quad bistable transparent latch		8407001EA
CD54HC/HCT85	4-bit magnitude comparator		8601301EA 5962-8867201EX
CD54HC/HCT86	Quad 2-input exclusive-OR gate		8404601CA
CD54HC/HCT93	4-bit binary ripple counter		
CD54HC/HCT107	Dual J-K flip-flop w/reset		5962-8515401CA
CD54HC/HCT109	Dual J-K flip-flop w/set and reset		8415001EA
CD54HC/HCT112	Dual J-K flip-flop w/set and reset		8408801EA 5962-8970201EA
CD54HC/HCT123	Dual retriggerable monostable multivibrator w/reset		5962-8684701EA
CD54HC/HCT125	Quad 3-state buffer		5962-8772101CA
CD54HC/HCT126	Quad 3-state buffer		5962-8684801CA
CD54HC/HCT132	Quad 2-input NAND Schmitt Trigger		5962-8984501CA
CD54HC/HCT137	3-to-8-line decoder w/ latch, inverting		
CD54HC/HCT138	3-to-8-line decoder/ emultiplexer, inverting		8406201EA 8550401EA
CD54HC/HCT139	Dual 2-of-4-line decoder/demultiplexer		8409201EA
CD54HC/HCT147	10-to-4-line priority encoder		8406401EA
CD54HC/HCT151	8-Input multiplexer		8412801EA
CD54HC/HCT153	Dual 4-input multiplexer		8409301EA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD54HC/HCT154	4-to-16-line decoder/ demultiplexer		5962-8682201JA 5962-8670101JX
CD54HC/HCT157	Quad 2-input multiplexer		5962-860610EA
CD54HC/HCT158	Quad 2-input multiplexer, inverting		5962-8682301EA
CD54HC/HCT160	Synchronous BCD decade counter, asynchronous reset		5962-8682401EA
CD54HC/HCT161	Synchronous 4-bit binary counter, asynchronous reset		8407501EA
CD54HC/HCT162	Synchronous BCD decade counter, synchronous reset		8409401EA 5962-8970501EA
CD54HC/HCT163	Synchronous 4-bit binary counter, synchronous reset		8407601EA
CD54HC/HCT164	8-bit serial-in parallel-out shift register		8416201CA 5962-8970401CA
CD54HC/HCT165	8-bit parallel-in serial-out shift register		8409501EA 5962-8685501EX
CD54HC/HCT166	8-bit parallel-in serial-out shift register		
CD54HC/HCT173	Quad D-type flip-flop, 3-state		5962-8682501EA 5962-8875901EA
CD54HC/HCT174	Hex D-type flip-flop w/ reset		8407301EA
CD54HC/HCT175	Quad D-type flip-flop w/reset		8408901EA 5962-8970101EA
CD54HC/HCT181	ALU		
CD54HC/HCT182	Carry generator		
CD54HC/HCT190	Presettable synchronous BCD decade up/down counter		
CD54HC/HCT191	Synchronous 4-bit binary up/down counter		5962-8689101EA 5962-8867101
CD54HC/HCT192	Synchronous BCD decade up/down counter		5962-8772401EA
CD54HC/HCT193	Synchronous 4-bit binary up/down counter		5962-8780801EA
CD54HC/HCT194	4-bit bidirectional universal shift register		5962-8682601EA
CD54HC/HCT195	4-bit parallel access shift register		5962-8682701EA
CD54HC/HCT221	Dual monostable multivibrator w/reset		5962-8780501EA
CD54HC/HCT237	3-to-8 line decoder		5962-8860601EA
CD54HC/HCT238	3-to-8 line decoder/ emultiplexer		5962-8688401EA 5962-8974501EA
CD54HC/HCT240	Octal buffer/line driver, 3-state, inverting		8407401RA 8550501RA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD54HC/HCT241	Octal buffer/line driver, 3-state		
CD54HC/HCT242	Quad bus transciever, 3-state, inverting		
CD54HC/HCT243	Quad bus transciever, 3-state		8409001CA
CD54HC/HCT244	Octal buffer/line driver, 3-state	MIL-M-38510/65701	8409601RA 8513001RA
CD54HC/HCT245	Octal bus transceiver, -state		8408501RA 8550601RA
CD54HC/HCT251	8-input multiplexer, 3-state		8512501EA
CD54HC/HCT253	Dual 4-input multiplexer, 3-state		
CD54HC/HCT257	Quad 2-input multiplexer, 3-state		8512401EA 5962-8970101EA
CD54HC/HCT258	Quad 2-line-to-4 line data selector		5962-8970701EA
CD54HC/HCT259	8-bit addressable latch		8551901EA
CD54HC/HCT273	Octal D-type flip-flop w/ reset		8409901RA
CD54HC/HCT280	9-bit odd/even parity generator/checker		8607701CA
CD54HC/HCT283	4-bit full adder w/fast carry		
CD54HC/HCT297	Digital phase-locked-loop filter		
CD54HC/HCT299	8-bit universal shift register, 3-state		5962-8780601RA
CD54HC/HCT354	8-input multiplexer/ register, 3-state		
CD54HC/HCT356	8-input multiplexer/ register, 3-state		
CD54HC/HCT365	Hex buffer/line driver, 3-state		8500101EA
CD54HC/HCT366	Hex buffer/line driver, 3-state, inverting		5962-8682801EA
CD54HC/HCT367	Hex buffer/line driver, 3-state		8500201EA
CD54HC/HCT368	Hex buffer/line driver, 3-state, inverting		5962-8681201EA
CD54HC/HCT373	Octal transparent latch, 3-state	MIL-M-38510/65403	8407201RA 5962-8686701RX
CD54HC/HCT374	Octal D-type flip-flop, -state		8407101RA 8550701RX
CD54HC/HCT377	Octal D-type flip-flop with data enable		5962-8780701RA
CD54HC/HCT390	Dual decade ripple counter		8600901EA
CD54HC/HCT393	Dual 4-bit binary ripple counter		8410001CA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD54HC/HCT423	Dual retriggerable monostable multivibrator with reset		
CD54HC/HCT533	Octal transparent latch, 3-state, inverting		5962-8681301RA
CD54HC/HCT534	Octal D-type flip-flop, 3-state, inverting		5962-8681401RA 5962-8984901RA
CD54HC/HCT540	Octal buffer/line driver, 3-state, inverting		
CD54HC/HCT541	Octal buffer/line driver, 3-state		
CD54HC/HCT563	Octal transparent latch, 3-state, inverting		5962-8606201RA
CD54HC/HCT564	Octal D-type flip-flop, 3-state, inverting		5962-8681501RA
CD54HC/HCT573	Octal transparent latch, 3-state		8512801RA 5962-8685601RX
CD54HC/HCT574	Octal D-type flip-flop, 3-state		
CD54HC/HCT583	4-bit full adder w/fast carry		
CD54HC/HCT597	8-bit shift register with I/P latch		5962-8681701EA 5962-8974101EA
CD54HC/HCT640	Octal bus transceiver, 3-state inverting		5962-8780901RA
CD54HC/HCT643	Octal bus transceiver, 3-state, true/inverting		
CD54HC/HCT646	Octal bus transceiver/ register, 3-state		5962-8688501JA
CD54HC/HCT648	Octal bus transceiver/ register, 3-state, inverting		
CD54HC/HCT670	4 x 4 register file, 3-state		
CD54HC/HCT688	8-bit magnitude comparator		5962-8681801RA 5962-8685701RX
CD54HC/HCT4002	Dual 4-input NOR gate		8404401CA
CD54HC/HCT4015	Dual 4-bit serial-in/ parallel-out shift register		
CD54HC/HCT4016	Quad bilateral switch		5962-8875801CA
CD54HC/HCT4017	Johnson decade counter w/10 decoded outputs		8601101EA
CD54HC/HCT4020	14-stage binary ripple counter		8500301EA
CD54HC/HCT4024	7-stage binary ripple counter		8601201CA
CD54HC/HCT4040	12-bit binary ripple counter		8500401EA
CD54HC/HCT4046	Phase-locked loop with VCO		5962-8960901EA
CD54HCT/HC4046A	Phase-locked loop with VCO hex inverting high-to-low level shifter, hex high-to-low level shifter		5962-8875701EA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD54HC/HCT4049	Hex inverting high-to-low level shifter		5962-8681901EA
CD54HC/HCT4050	Hex high-to-low level shifter		5962-8682001EA
CD54HC/HCT4051	8 channel analog multiplexer/ demultiplexer		
CD54HC/HCT4052	Dual 4 channel analog multiplexer/ demultiplexer		5962-8855601EA
CD54HC/HCT4053	Triple 2 channel analog multiplexer/ demultiplexer		5962-8775401EA
CD54HC/HCT4059	Programmable divided-by-"N" counter		5962-8862401JA
CD54HC/HCT4060	14-stage binary ripple counter w/oscillator		5962-8768001EA
CD54HC/HCT4066	Quad bilateral switch		5962-8950701CA
CD54HC/HCT4067	16 channel analog multiplexer/ demultiplexer		
CD54HC/HCT4075	Triple 3-input OR gate		5962-8772201CA
CD54HC/HCT4094	8-stage shift-and-store bus register		
CD54HC/HCT4316	Quad analog switch		
CD54HC/HCT4351	Analog multiplexer w/ latch		
CD54HC/HCT4352	Analog multiplexer w/ latch		
CD54HC/HCT4353	Analog multiplexer w/ latch		
CD54HC/HCT4510	Up/down counter, BCD		
CD54HC/HCT4511	BCD-to-7-segment latch/decoder/driver		5962-8773301EA
CD54HC/HCT4514	4-to-16-line decoder/ demultiplexer w/input latches		5962-8773301EA
CD54HC/HCT4515	4-to-16-line decoder with input latches		
CD54HC/HCT4516	Up/down counter, binary		
CD54HC/HCT4518	Dual synchronous BCD counter		
CD54HC/HCT4520	Dual 4-bit synchronous binary counter		
CD54HC/HCT4538	Dual precision monostable multivibrator		5962-8688601EA
CD54HC/HCT4543	BCD-to-7-segment latch/decoder/driver for LCDs		
CD54HC/HCT7266	Quad exclusive NOR		8404301CA
CD54HC/HCT40102	8-bit synchronous BCD down counter		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD54HC/HCT40103	8-bit binary down counter		
CD54HC/HCT40104	4-bit bidirectional universal shift register, 3-state		
CD54HC/HCT40105	4-bits x 16 Words FiFo register		
CD54HC/HCTU04	Hex inverter (unbuffered)		5962-861001CA
CD54HCS154	SOS 4-to- 16-line decoder/demultiplexer		
CD54HCS164	SOS 8-bit serial-in parallel-out shift register		
CD54HCS165	SOS 8-bit parallel-in serial-out shift register		
CD54HCS166	SOS 8-bit parallel-in serial-out shift register		
CD54HCS253	SOS Dual 4-input multiplexer, 3-state		
CD54HCS573	SOS Octal transparent latch, 3-state		
CD54HCS4538	SOS Dual precision monostable multivibrator		
CD54HCS/HCTS00	SOS Quad 2-input NAND gate		
CD54HCS/HCTS02	SOS Quad 2-input NOR gate		
CD54HCS/HCTS04	SOS Hex inverter		
CD54HCS/HCTS32	SOS Quad 2-input OR gate		
CD54HCS/HCTS74	SOS Dual D flip-flop w/ set and reset		
CD54HCS/HCTS109	SOS Dual J-K flip-flop w/set and reset		
CD54HCS/HCTS138	SOS 3-to-8 line decoder/demultiplexer, inverting		
CD54HCS/HCTS161	SOS Synchronous 4-bit binary counter, asynchronous reset		
CD54HCS/HCTS244	SOS Octal buffer/line driver, 3-state		
CD54HCS/HCTS245	SOS Octal bus transceiver, 3-state		
CD54HCS/HCTS373	SOS Octal transparent latch, 3-state		
CD54HCS/HCTS374	SOS Octal D-type flip-flop, 3-state		
CD54HCTS08	SOS Quad 2-input AND gate		
CD54HCTS10	SOS Triple 3-input NAND gate		
CD54HCTS11	SOS Triple 3-input AND gate		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CD54HCTS14	SOS Hex inverting Schmitt Trigger		
CD54HCTS20	SOS Dual 4-input NAND gate		
CD54HCTS21	SOS Dual 4-input AND gate		
CD54HCTS27	SOS Triple 3-input NOR gate		
CD54HCTS86	SOS Quad 2-input exclusive-OR gate		
CD54HCTS93	SOS 4-bit binary ripple counter		
CD54HCTS112	SOS Dual J-K flip-flop w/set and reset		
CD54HCTS139	SOS Dual 2-of-4-line decoder/demultiplexer		
CD54HCTS153	SOS Dual 4-input multiplexer		
CD54HCTS157	SOS Quad 2-input multiplexer		
CD54HCTS160	SOS Synchronous BCD decade counter, asynchronous reset		
CD54HCTS163	SOS Synchronous 4-bit binary counter, synchronous reset		
CD54HCTS191	SOS Synchronous 4-bit binary up/down counter		
CD54HCTS193	SOS Synchronous 4-bit binary up/down counter		
CD54HCTS240	SOS Octal buffer/line driver, 3-state, inverting		
CD54HCTS273	SOS Octal D-type flip-flop w/reset		
CD54HCTS299	SOS 8-bit universal shift register, 3-state		
CD54HCTS390	SOS Dual decade ripple counter		
CD54HCTS540	SOS Octal buffer/line driver, 3-state, inverting		
CD54HCTS574	SOS Octal D-type flip-flop, 3-state		
CD54HCU04			8601001CA
CDM5114C	1K x 4 SRAM		
CDM5332C	4K x 8 ROM		
CDM62256C	32K x 8 SRAM		
CDM6264	8K x 8 SRAM		
CDP1802	8 bit Microprocessor		
CDP1821	1K x 10 SRAM		
CDP1822	256 x 4 SRAM		
CDP1823	128 x 8 SRAM		
CDP1824	32 x 8 SRAM		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
CDP1831	512 x 8 ROM		
CDP1832	512 x 8 ROM		
CDP1833	1K x 8 ROM		
CDP1834	1K x 8 ROM		
CDP1852	I/O port		
CDP1853	Decoder		
CDP1854	UART		
CDP1857	Buffer/separator		
CGA10	2-micron CMOS gate array		
CGA100	1.5-micron CMOS gate array		
CMM5104	4K x 1 SRAM		
CMM5114	1K x 4 SRAM		
CMM6167	16 x 1 SRAM		
CMM6287	64K x 1 SRAM		
DG129	4-ch decoded JFET SW driver		7801401CA
DG181	Dual SPST 30 ohm hi-speed driver with JFET SW	JM38510/11101BCA	
DG182	Dual SPST 75 ohm hi-speed driver with JFET SW	JM38510/11102BCA	
DG184	Dual DPST 30 ohm hi-speed driver with JFET SW	JM38510/11103BEA	
DG185	Dual DPST 75 ohm hi-speed driver with JFET SW	JM38510/11104BEA	
DG187	SPDT 30 ohm hi-speed driver with JFET SW	JM38510/11105BCA	
DG188	SPDT 75 ohm hi-speed driver with JFET SW	JM38510/11106BCA	
DG190	Dual SPDT 30 ohm hi-speed driver with JFET SW	JM38510/11107BEA	
DG191	Dual SPDT 75 ohm hi-speed driver with JFET SW	JM38510/11108BEA	
DG201	Quad SPST CMOS analog SW	JM38510/12302BEA	
DG300A	TTL compatible CMOS analog SW	JM38510/11601BCA	
DG301A	TTL compatible CMOS analog SW	JM38510/11603BCA	
DG302A	TTL compatible CMOS analog SW	JM38510/11603BCA	
DG303A	TTL compatible CMOS analog SW	JM38510/11604BCA	
FRF6764	100V/38A power MOSFET		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
FRF6766	200V/30A power MOSFET		
FRK150D	100V/38A power MOSFET		
FRK160D	100V/62A power MOSFET		
FRK234D	250V/23A power MOSFET		
FRK250D	200V/30A power MOSFET		
FRK260D	200V/50A power MOSFET		
FRK264D	250V/34A power MOSFET		
FRK6764	100V/38A power MOSFET		
FRK6766	200V/30A power MOSFET		
FRK9150D	-100V/28A power MOSFET		
FRK9160D	-100V/40A power MOSFET		
FRK9250D	-200V/17A power MOSFET		
FRK9260D	-200V/24A power MOSFET		
FRL130D	100V/8A power MOSFET		
FRL230D	200V/5.5A power MOSFET		
FRL234D	250V/4.5A power MOSFET		
FRL430D	500V/2.5A power MOSFET		
FRL6796	100V/8A power MOSFET		
FRL6798	200V/5.5A power MOSFET		
FRL9130D	-100V/5A power MOSFET		
FRL9230D	-200V/3A power MOSFET		
FRL9430D	-500V/1A power MOSFET		
FRM130D	100V/14A power MOSFET		
FRM140D	100V/22A power MOSFET		
FRM230D	200V/9A power MOSFET		
FRM240D	200V/18A power MOSFET		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
FRM234D	250V/7.5A power MOSFET		
FRM244D	250V/12.5A power MOSFET		
FRM430D	500V/4.5A power MOSFET		
FRM440D	500V/8A power MOSFET		
FRM450D	500V/13A power MOSFET		
FRM460D	500V/23A power MOSFET		
FRM6756	100V/14A power MOSFET		
FRM6758	200V/9A power MOSFET		
FRM9130D	-100V/8A power MOSFET		
FRM9140D	-100V/15.5A power MOSFET		
FRM9230D	-200V/5A power MOSFET		
FRM9240D	-200V/9A power MOSFET		
FRM9430D	-500V/2A power MOSFET		
FRM9440D	-500V/4.5A power MOSFET		
FRM9450D	-500V/8A power MOSFET		
FRM9460D	-500V/11A power MOSFET		
FRS6756	100V/14A power MOSFET		
FRS6758	200V/9A power MOSFET		
GP001	General processor		
GP301	Mask-programmable ROM, 512 x 8		
GP302	Mask-programmable ROM, 256 x 16		
GP305	Mask-programmable ROM		
GP501	Emulating controller		
GP502	"2910" type controller		
GP503	Multiplier		
GP511	Voltage level converter and buffer		
GP514	Double address select unit		
GP515	Double register select unit		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
GP516	Bus interface unit		
GP517	Interrupt control unit		
GS105	½ bridge module		
GS205	AC line smart switch		
GS210	Dual DC source smart switch		
GS215	Dual DC sink smart switch		
GS600	½ bridge MOS driver HVIC		
GS601	½ bridge MOS driver HVIC		
HA1-2400	4-channel prog. op-amp		5962-8778301
HA1-2420	High speed sample and hold		8001601 8001601CA
HA1-2539	High slew rate wideband op-amp		5962-8778701
HA1-2540	Widenband fast settling op-amp		5962-8964801
HA1-2546	2 Quadrant video multiplier		
HA1-2547	Video multiplier		
HA1-4741	Quad operational amp		
HA1-4900	Precision quad comparator		
HA1-4902	Precision quad comparator		5962-8686001
HA1-5004	Video buffer-amplifier		
HA1-5033	Video buffer		5962-8963301
HA1-5104	Quad low noise hi-perf op-amp		5962-8850201
HA1-5114	Quad low noise hi-perf op-amp		5962-8963401
HA1-5134	Precision quad amp		
HA1-5144	Quad ultra low power amp		5962-8965603
HA1-5154	Quad low power amp		5962-8964903
HA1-5190	Wideband fast settling op-amp		5962-8778401
HA1-5330	High speed sample and hold		5962-8767701
HA2-2500	Precision high slew rate amp	JM38510/12204BGC	
HA2-2502	Precision high slew rate amp		
HA2-2510	High slew rate amp	JM38510/12205BGC	
HA2-2512	High slew rate amp		
HA2-2520	High slew rate (uncomp) amp	JM38510/12206BGC	

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HA2-2522	High slew rate (uncomp) amp		
HA2-2529	High output current op-amp		5962-8972101
HA2-2541	Wideband unity gain op-amp		5962-8778501
HA2-2542	High output current op-amp		5962-8964301
HA2-2544	Video op-amp		5962-8950201
HA2-2548	High slew rate wideband amp		
HA2-2600	Wideband high impedence amp	JM38510/12202BGC	
HA2-2602	Wideband high impedence amp		
HA2-2620	Wideband (uncomp) amp	JM38510/12203BGC	
HA2-2622	Wideband (uncomp) amp		
HA2-2640	High voltage op-amp		7800302
HA2-2650	Dual high performance amp		
HA2-5002	Current driver op-amp		5962-8963601
HA2-5033	Video buffer		5962-8963301
HA2-5101	Low noise hi-performance op-amp		5962-8963501
HA2-5102	Dual low noise hi-perf op-amp		5962-8954801
HA2-5111	Low noise hi-performance op-amp		5962-8963101
HA2-5112	Dual low noise hi-perf op-amp		5962-8963201
HA2-5127	Ultra low noise precision op-amp		5962-8962701
HA2-5130	Precision amp		
HA2-5135	Precision amp		
HA2-5137	Ultra low noise precision op-amp		5962-8962702
HA2-5141	Ultra low power op-amp		5962-8965601
HA2-5142	Dual ultra low power op-amp		5962-8965602
HA2-5144	Quad ultra lower power op-amp		5962-8965603
HA2-5147	Ultra low noise wideband op-amp		5962-8962703
HA2-5151	Low power op-amp		5962-8964901
HA2-5152	Dual low power op-amp		5962-8964902
HA2-5160	Wideband J-FET input amp		
HA2-5170	Precision J-FET input amp		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HA2-5177	Ultra-low offset voltage amp		
HA2-5180	Low bias current J-FET amp		
HA2-5190	Wideband fast settling op-amp		5962-8778401
HA2-5221	Single wideband amp		
HA4-2400	4-channel prog. op-amp		5962-8778301
HA4-2410	High slew rate amp		
HA4-2420	High speed sample and hold		8001601
HA4-2502	Precision high slew rate amp		
HA4-2512	High slew rate amp		
HA4-2522	High slew rate (uncomp) amp		
HA4-2529	High output current op-amp		5962-8972101
HA4-2539	High slew rate wideband op-amp		5962-8778701
HA4-2540	Wideband fast settling op-amp		5962-8964801
HA4-2544	Video op-amp		5962-8950201
HA4-2546	2 quadrant video multiplier		
HA4-2547	Video multiplier		
HA4-2548	High slew rate wideband amp		
HA4-2602	wideband high impedence amp		
HA4-2622	Wideband (uncomp) amp		
HA4-2640	High voltage op-amp		7800302
HA4-2650	Dual high performance amp		
HA4-4741	Quad operational amp		
HA4-4900	Precision quad comparator		
HA4-4902	Precision quad comparator		5962-8686001
HA4-5002	Current driver op-amp		5962-8963601
HA4-5004	Video buffer-amplifier		
HA4-5101	Low noise hi-performance op-amp		5962-8963501
HA4-5102	Dual low noise hi-perf op-amp		5962-8954801
HA4-5104	Quad low noise hi-perf op-amp		5962-8850201
HA4-5111	Low noise hi-performance op-amp		5962-8963101

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HA4-5112	Dual low noise hi-perf op-amp		5962-8963201
HA4-5114	Quad low noise hi-perf op-amp		5962-8963401
HA4-5127	Ultra low noise precision op-amp		5962-8962701
HA4-5134	Precision quad amp		
HA4-5135	Precision amp		
HA4-5137	Ultra low noise precision op-amp		5962-8962702
HA4-5141	Ultra low power op-amp		5962-8965601
HA4-5142	Dual ultra low power op-amp		5962-8965602
HA4-5144	Quad ultra low power op-amp		5962-8965603
HA4-5147	Ultra low noise wideband op-amp		5962-8962703
HA4-5151	Low power op-amp		5962-8964901
HA4-5152	Dual low power op-amp		5962-8964902
HA4-5154	Quad low power op-amp		5962-8964903
HA4-5170	Precision J-FET input amp		
HA4-5177	Ultra-low offset voltage amp		
HA4-5190	Wideband fast settling op-amp		5962-8778401
HA4-5221	Single wideband amp		
HA4-5222	Dual wideband amp		
HA4-5330	High speed sample and hold		5962-8767701
HA7-2500	Precision high slew rate amp		
HA7-2502	Precision high slew rate amp		
HA7-2510	High slew rate amp		
HA7-2512	High slew rate amp		
HA7-2520	High slew rate (uncomp) amp		
HA7-2522	High slew rate (uncomp) amp		
HA7-2529	High output current op-amp		5962-8972101
HA7-2544	Video op-amp		5962-8950201
HA7-2548	High slew rate wideband amp		
HA7-2600	Wideband high impedence amp		
HA7-2602	Wideband high impedence amp		
HA7-2620	Wideband (uncomp) amp		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HA7-2622	Wideband (uncomp) amp		
HA7-2640	High voltage op-amp		7800302
HA7-2650	Dual high performance amp		
HA7-5002	Current driver op-amp		5962-8963601
HA7-5101	Low noise hi-performance op-amp		5962-8963501
HA7-5102	Dual low noise hi-perf op-amp		5962-8954801
HA7-5111	Low noise hi-performance op-amp		5962-8963101
HA7-5112	Dual low noise hi-perf op-amp		5962-8963201
HA7-5127	Ultra low noise precision op-amp		5962-8962701
HA7-5130	Precision amp		
HA7-5135	Precision amp		
HA7-5137	Ultra low noise precision op-amp		5962-8962702
HA7-5141	Ultra low power op-amp		5962-8965601
HA7-5142	Dual ultra low power op-amp		5962-8965602
HA7-5144	Quad ultra low power op-amp		5962-8965603
HA7-5147	Ultra low noise wideband op-amp		5962-8962703
HA7-5151	Low power op-amp		5962-8964901
HA7-5152	Dual low power op-amp		5962-8964902
HA7-5170	Precision J-FET input amp		
HA7-5177	Ultra-low offset voltage amp		
HA7-5180	Low bias current J-FET amp		
HA7-5221	Single wideband amp		
HA7-5222	Dual wideband amp		
HC1-55564	CVSD		
HC4-55564	CVSD		
HD1-4702	Programmable bit rate generator		
HD1-6402	Universal asynchronous receiver transmitter		5962-9052501QA
HD1-15530	Manchester encoder-decoder		7802901JA
HD1-15531	Manchester encoder-decoder		5962-9054901QA
HD1-15531B	Manchester encoder-decoder		5962-9054902QA
HD4-15530	Manchester encoder-decoder		78029013A

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HD1-6409	Manchester encoder-decoder		
HFA1-0001	Ultra high speed op amp		
HFA2-0002	Wideband op amp		
HFA2-0005	High speed op amp		
HFA4-0001	Ultra high speed op amp		
HFA4-0002	Wideband op amp		
HFA4-0005	High speed op amp		
HFA7-0002	Wideband op amp		
HFA7-0005	High speed op amp		
HI1-562A	12 bit D to A converter		
HI1-565A	12 bit D to A converter		
HI1-574A	12 bit A to D converter		5962-8512704XA
HI1-674A	12 bit A to D converter		
HI1-774	12 bit A to D converter		
HI1-0200	Dual SPST CMOS analog sw		
HI1-0201	Quad SPST CMOS analog sw	JM38510/12302BEA	
HI1-0201HS	High speed quad SPST CMOS analog sw		5962-8671601EA
HI1-0222	Dual SPST CMOS analog sw		
HI1-0506	16 channel CMOS analog mux	JM38510/19001BXA	
HI1-0507	8 channel CMOS differential analog mux	JM38510/19003BXA	
HI1-0508	8 channel CMOS analog mux	JM38510/19007BEA	7705201EC
HI1-0509	4 channel CMOS differential analog mux	JM38510/19008BEA	
HI1-0546	16 channel CMOS analog mux	JM38510/19002BXA	5962-8513101XA
HI1-0547	8 channel CMOS differential analog mux	JM38510/19004BXA	5962-8513102XA
HI1-0548	8 channel CMOS analog mux	JM38510/19005BEA	7705202EA
HI1-0549	4 channel CMOS differential analog mux	JM38510/19006BEA	5962-8513103EA
HI1-1818A	8 channel CMOS analog mux		
HI1-1828A	4 channel CMOS differential analog mux		
HI1-5040	Single SPST CMOS analog sw		8100609EA
HI1-5041	Dual SPST CMOS analog sw		8100610EA
HI1-5042	Single SPDT CMOS analog sw		8100611EA
HI1-5043	Dual SPDT CMOS analog sw		8100612EA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HI1-5044	Single DPST CMOS analog sw		8100613EA
HI1-5045	Dual DPST CMOS analog sw		8100614EA
HI1-5046	Single DPDT CMOS analog sw		8100615EA
HI1-5046A	Single DPDT CMOS analog sw		8100617EA
HI1-5047	DPDT CMOS analog sw		8100616EA
HI1-5047A	DPDT CMOS analog sw		8100618EA
HI1-5048	Dual SPST CMOS analog sw		8100619EA
HI1-5049	Dual DPST CMOS analog sw		8100620EA
HI1-5050	SPDT CMOS analog sw		8100621EA
HI1-5051	Dual SPDT CMOS analog sw		8100622EA
HI1-DAC87V	12-Bit D to A converter		
HI2-0200	Dual SPST CMOS analog sw		
HI4-562A	12 bit D to A converter		
HI4-574A	12 bit A to D converter		5962-8512704YA
HI4-674A	12 bit A to D converter		
HI4-0201	Quad SPST CMOS analog sw		
HI4-0201HS	High speed quad SPST CMOS analog sw		5962-86716012A
HI4-0506	16 channel CMOS analog mux		
HI4-0507	8 channel CMOS differential analog mux		
HI4-0508	8 channel CMOS analog mux		
HI4-0509	4 channel CMOS differential analog mux		
HI4-0546	16 channel CMOS analog mux		5962-85131013A
HI4-0547	8 channel CMOS differential analog mux		5962-85131023A
HI4-0548	8 channel CMOS analog mux		77052022A
HI4-0549	4 channel CMOS differential analog mux		5962-85131032A
HI4-5043	Dual SPDT CMOS analog sw		81006122A
HI4-5045	Dual DPST CMOS analog sw		81006142A
HI4-5049	Dual DPST CMOS analog sw		81006202A
HI4-5051	Dual SPDT CMOS analog sw		81006222A
HI4-DAC87V	12-bit D to A converter		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HM-91M2	1m-bit asynchronous RAM module		
HM1-6504	4K x 1 synchronous RAM		8102405VA
HM1-6504B	4K x 1 synchronous RAM		8102403VA
HM1-6504S	4K x 1 synchronous RAM	M38510/24501BVA	8102401VA
HM1-6508	1K x 1 synchronous RAM		
HM1-6508B	1K x 1 synchronous RAM		
HM1-6514	1K x 4 synchronous RAM		8102406VA
HM1-6514B	1K x 4 synchronous RAM		8102404VA
HM1-6514S	1K x 4 synchronous RAM	M38510/24502BVA	8102402VA
HM1-6516	2K x 8 synchronous RAM	M38510/29102BJA	8403601JA
HM1-6516B	2K x 8 synchronous RAM		8403607JA
HM1-65162	2K x 8 asynchronous RAM	M38510/29104BJA	8403602JA
HM1-65162B	2K x 8 asynchronous RAM	M38510/29110BJA	8403606JA
HM1-65162C	2K x 8 asynchronous RAM		8403603JA
HM1-6518	1K x 1 synchronous RAM		
HM1-6518B	1K x 1 synchronous RAM		
HM1-65262	16K x 1 asynchronous RAM	M38510/29103BRA	8413201RA
HM1-65262B	16K x 1 asynchronous RAM	M38510/29109BRA	8413203RA
HM1-6551	256 x 4 synchronous RAM		
HM1-6551B	256 x 4 synchronous RAM		
HM1-6561	256 x 4 synchronous RAM		
HM1-6561B	256 x 4 synchronous RAM		
HM1-65642	8K x 8 asynchronous RAM		8552514XA
HM1-65642B	8K x 8 asynchronous RAM	M38510/29205BXA	
HM1-65642C	8K x 8 asynchronous RAM		
HM1-6617	2K x 8 fuse link PROM		8954001JA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HM1-6617B	2K x 8 fuse link PROM		8954002JA
HM1-6642	512 x 8 fuse link PROM		8869001JA
HM1-6642B	512 x 8 fuse link PROM		8869002JA
HM4-6516	2K x 8 synchronous RAM	M38510/29102BXA	8403601ZA
HM4-6516B	2K x 8 synchronous RAM		8403607ZA
HM4-65161B		M38510/29110BXA	8403606ZA
HM4-65162	2K x 8 asynchronous RAM	M38510/29104BXA	8403602ZA
HM4-65162C	2K x 8 asynchronous RAM		8403603ZA
HM4-65262	16K x 1 asynchronous RAM	M38510/29103BYA	8413201YA
HM4-65262B	16K x 1 asynchronous RAM	M38510/29109BYA	8413203YA
HM4-65642	8K x 8 asynchronous RAM		8552514YA
HM4-65642B	K x 8 asynchronous RAM	M38510/29205BYA	
HM4-65642C	8K x 8 asynchronous RAM		
HM4-6617	2K x 8 fuse link PROM		8954001XA
HM4-6617B	2K x 8 fuse link PROM		8954002XA
HM4-6642	512 x 8 fuse link PROM		88690013A
HM4-6642B	512 x 8 fuse link PROM		88690023A
HM5-6564	64K synchronous RAM module		
HM5-8808	8K x 8 asynchronous RAM modules		
HM5-8816H	16K x 8 asynchronous RAM module		
HM5-8832	32K x 8 asychronous RAM module		
HM5-8832B	32K x 8 asychronous RAM module		
HM5-92560	256K synchronous RAM module		
HM5-92570	256K buffered synchronous RAM module		
HM6-6617	2K x 8 fuse link PROM		8954001LA
HM6-6617B	2K x 8 fuse link PROM		8954002LA
HM6-6642	512 x 8 fuse link PROM		8869001LA
HM6-6642B	512 x 8 fuse link PROM		8869002LA
HR3N0187	Dual insulated gate FET		
HR3N0200	Dual insulated gate FET		
HR3N0205	Dual insulated gate FET		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HS-15530RH	Rad-hard CMOS Manchester encoder/ decoder		
HS-3374	Rad-hard CMOS/TTL bidirectional level shifter		
HS-3447	Cypher-1™ data encoder		
HS-54C138RH	Rad-hard 3-line to 8-line CMOS decoder/ demultiplexer		
HS-6504RH	Rad-hard 4K x 1 CMOS static RAM (synchronous)		
HS-6504RRH	SEU immune rad-hard 4K x 1 CMOS static RAM (synchronous)		
HS-6508RH	Rad-hard 1K x 1 CMOS static RAM (synchronous)		
HS-6514RH	Rad-hard 1K x 4 CMOS static RAM (synchronous)		
HS-6514RRH	SEU immune rad-hard 1K x 4 CMOS static RAM (synchronous)		
HS-6551RH	Rad-hard 256 x 4 CMOS static RAM (synchronous)		
HS-65643RH HS-65647RH			
HS-6564RH	Rad-hard 8K x 8 or 16K x 4 CMOS RAM module (synchronous)		
HS-65C162RH	Rad-hard 2K x 8 CMOS static RAM (asynchronous)		
HS-65C162RRH	SEU immune rad-hard 2K x 8 CMOS static RAM (asynchronous)		
HS-65C262RH	Rad-hard 16K x 1 CMOS static RAM (asynchronous)		
HS-65C262RRH	SEU immune rad-hard 16K x 1 CMOS static RAM (asynchronous)		
HS-65T162RRH	SEU immune rad-hard 2K x 8 CMOS static RAM (asynchronous)		
HS-65T262RRH	SEU immune rad-hard 16K x 1 CMOS static RAM (asynchronous)		
HS-6617RH	Rad-hard 2K x 8 CMOS PROM (synchronous)		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HS-80C85RH	Rad-hard 8-bit CMOS microprocessor		
HS-80C86RH	Rad-hard 16-bit CMOS microprocessor		
HS-81C55RH	Rad-hard 256 x 8 CMOS RAM with I/O ports and timer		
HS-81C56RH	Rad-hard 256 x 8 CMOS RAM with I/O ports and timer		
HS-82C08RH	Rad-hard 8-bit CMOS bus tranceiver		
HS-82C12RH	Rad-hard 8-bit CMOS I/O port		
HS-82C37ARH	Rad-hard CMOS programmable DMA controller		
HS-82C54RH	Rad-hard CMOS programmable interval timer		
HS-82C55RH	Rad-hard CMOS programmable peripheral interface		
HS-82C85RH	Rad-hard CMOS static clock controller/ generator		
HS83C55RH	Rad-hard 2K x 8 CMOS ROM with I/O ports		
HS1-1840RH	Rad-hard 16 channel analog multiplexer		
HS1-302RH	Rad-hard CMOS analog switches		
HS1-303RH	Rad-hard CMOS analog switches		
HS1-306RH	Rad-hard CMOS analog switches		
HS1-307RH	Rad-hard CMOS analog switches		
HS1-384RH	Rad-hard CMOS analog switches		
HS1-390RH	Rad-hard CMOS analog switches		
HS1-508ARH	Rad-hard 8 channel differential analog		
HS1-3182	ARINC 429 bus interface line driver		8687901EA
HS1-3282	ARINC 429 bus interface circuit		8688001QA
HS1-5104RH	Rad-hard Quad op amp		
HS2-3530RH	Rad-hard low power op amp		

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
HS4-3182	ARINC 429 bus interface line driver		86879013A
HS4-3282	ARINC 429 bus interface circuit		8688001XA
HS9-1840RH	Rad-hard 16 channel analog multiplexer		
HS9-3516RH	Rad-hard high slew rate op amp		
HS9-508ARH	Rad-hard 8 channel differential analog multiplexer		
HSC1000	CMOS cell library		
HSC1000RH	Rad-hard CMOS cell library		
ICL7667	Dual power MOSFET driver		5962-8766001
ICL8038	Waveform generator		5962-8877201
ICL8211	Voltage reference/ indicator		5962-8984201
ICL8212	Voltage reference/ indicator		5962-8984202
ICM7170MDG	Micro P-compatible real time clock		5462-8756301JA
ICM7555	CMOS 555 timer		5962-8950303
ICM7556	CMOS 556 dual timer		5962-8950304
IH5040MDE	SPST 75 ohm high-level CMOS analog switch	JM38510/10501BEA	
IH5040MJE	SPST 75 ohm high-level CMOS analog switch		8100601EA
IH5041MDE	Dual SPST 75 ohm high-level CMOS analog switch	JM38510/10502BEA	
IH5041MJE	Dual SPST 75 ohm high-level CMOS analog switch		8100602EA
IH5042MDE	SPDT 75 ohm high-level CMOS analog switch	JM38510/10503BEA	
IH5042MJE	SPDT 75 ohm high-level CMOS analog switch		8100603EA
IH5043MDE	Dual SPDT 75 ohm high-level CMOS analog switch	JM38510/10504BEA	
IH5043MDE	Dual SPDT 75 ohm high-level CMOS analog switch	JM38510/10504BEC	
IH5043MJE	Dual SPDT 75 ohm high-level CMOS analog switch		8100604EA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
IH5044MDE	DPST 75 ohm high-level CMOS analog switch	JM38510/10505BEA	
IH5044MJE	DPST 75 ohm high-level CMOS analog switch		8100605EA
IH5045MDE	Dual DPST 75 ohm high-level CMOS analog switch	JM38510/10506BEA	
IH5045MJE	Dual DPST 75 ohm high-level CMOS analog switch		8100606EA
IH5046MJE	DPDT 75 ohm high-level CMOS analog switch		8100607EA 8100615EA
IH5046MJE	DPDT 75 ohm high-level CMOS analog switch		8100615EA
IH5047MJE	4PST 75 ohm high-level CMOS analog switch		8100608EA 8100616EA
IH5047MJE	4PST 75 ohm high-level CMOS analog switch		8100616EA
IH5116MJI	16-Channel fault protected CMOS analog multiplexer		5962-8513104XA
IH5140MJE	SPST high-level CMOS analog switch		8100609EA
IH5141MJE	Dual SPST high-level CMOS analog switch		8100610EA
IH5142MJE	SPDT high-level CMOS analog switch		8100611EA
IH5143MJE	Dual SPDT high-level CMOS analog switch		8100612EA
IH5144MJE	DPST high-level CMOS analog switch		8100613EA
IH5145MJE	Dual DPST high-level CMOS analog switch		8100614EA
IH5148MJE	Dual SPST high-level CMOS analog switch		8100619EA
IH5149MJE	CMOS analog switch		8100620EA
IH5150MJE	CMOS analog switch		8100621EA 8100622
IH5208MJE	4-CH CMOS differential analog mux		5862-8513106EA
IH5216MJI	8-CH CMOS differential analog mux		5962-8513105XA
IH6108MDE	8-channel CMOS analog multiplexer		7705201EA
IH6108MJE	8-channel CMOS analog multiplexer		7705203EA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
IH6208MDE	4-channel CMOS analog multiplexer	JM3851019008BEA	
LM4250	Programmable op-amp		7703901
MD80C86	Static 16-bit microprocessor		8405201QA
MD80C86-2	Static 16-bit microprocessor		8405202QA
MD80C88	Static 8/16-bit microprocessor		5962-8601601QA
MD80C88-2	Static 8/16-bit microprocessor		5962-8601602QA
MD82C284	Clock driver		
MD82C288	Bus controller		
MD82C37A	High performance programmable DMA controller		
MD82C37A-5	High performance programmable DMA controller		
MD82C52	Serial controller interface		8501501XA
MD82C54	Programmable interval timer		8406501JA
MD82C55A	Programmable peripheral interface		8406602QA
MD82C55A-5	Programmable peripheral interface		8406601QA
MD82C59A	Priority interrupt controller		5962-8501602YA
MD82C59A-5	Priority interrupt controller		5962-8501601YA
MD82C82	Octal latching bus driver		8406701RA
MD82C83H	Octal latching inverting bus driver		8406702RA
MD82C84A	Clock generator driver		8406801VA
MD82C86H-5	Octal bus transceivers		5962-8757701RA
MD82C87H-5	Octal bus transceivers		5962-8757702RA
MD82C85	Static clock controller/ generator		
MD82C88	Bus controller		8406901RA
MD82C89	Bus arbiter		5962-8552801RA
MG80C286	Static 16-bit microprocessor		
MR80C86	Static 16-bit microprocessor		8405201XA
MR80C86-2	Static 16-bit microprocessor		8405202QA
MR80C88	Static 8/16-bit microprocessor		5962-8601601XA
MR80C88-2	Static 8/16-bit microprocessor		5962-8601602XA

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
MR82C37A	High performance programmable DMA controller		
MR82C37A-5	High performance programmable DMA controller		
MR82C52	Serial controller interface		85015013A
MR82C54	Programmable interval timer		84065013A
MR82C55A	Programmable peripheral interface		8406602XA
MR82C55A-5	Programmable peripheral interface		8406601XA
MR82C59A	Priority interrupt controller		5962-85016023A 85016023A
MR82C59A-5	Priority interrupt controller		5962-85016013A 85016013A
MR82C82	Octal latching bus driver		84067012A
MR82C83H	Octal latching inverting bus driver		8406702RA
MR82C84H	Clock generator driver		84068012A
MR82C85	Static clock controller/ generator		
MR82C86H-5	Octal bus transceivers		5962-87577012A
MR82C87H-5	Octal bus transceivers		5962-87577022A
MR82C88	Bus controller		84069012A
MR82C89	Bus arbiter		5962-85528012A
PA50000	3-micron DLM CMOS gate array		
SC3800	SOS rad-hard standard cells		
V8ZA1	8V MOV varistor		
V8ZA2	8V MOV varistor		
V12ZA1	12V MOV varistor		
V12ZA2	12V MOV varistor		
V22ZA1	22V MOV varistor		87063/002
V22ZA2	22V MOV varistor		87063/003
V22ZA3	22V MOV varistor		87063/004
V22ZA05	22V MOV varistor		87063/001
V24ZA50	24V MOV varistor		87063/005
V27ZA1	27V MOV varistor		87063/007
V27ZA2	27V MOV varistor		87063/008
V27ZA4	27V MOV varistor		87063/009
V27ZA05	27V MOV varistor		87063/006
V27ZA06	27V MOV varistor		87063/006
V27ZA60	27V MOV varistor		87063/010
V33ZA1	33V MOV varistor		87063/012
V33ZA2	33V MOV varistor		87063/013
V33ZA5	33V MOV varistor		87063/014

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
V33ZA05	33V MOV varistor		87063/011
V33ZA70	33V MOV varistor		87063/015
V36ZA80	36V MOV varistor		87063/016
V39ZA1	39V MOV varistor		87063/018
V39ZA3	39V MOV varistor		87063/019
V39ZA6	39V MOV varistor		87063/020
V39ZA05	39V MOV varistor		87063/017
V47ZA1	47V MOV varistor		87063/022
V47ZA3	47V MOV varistor		87063/023
V47ZA7	47V MOV varistor		87063/024
V47ZA05	47V MOV varistor		87063/021
V56ZA2	56V MOV varistor		87063/026
V56ZA3	56V MOV varistor		87063/027
V56ZA8	56V MOV varistor		87063/028
V56ZA05	56V MOV varistor		87063/025
V68ZA2	68V MOV varistor		87063/030
V68ZA3	68V MOV varistor		87063/031
V68ZA05	68V MOV varistor		87063/029
V68ZA10	68V MOV varistor		87063/032
V82ZA2	82V MOV varistor		87063/034
V82ZA4	82V MOV varistor		87063/035
V82ZA05	82V MOV varistor		87063/033
V82ZA12	82V MOV varistor		87063/036
V100ZA3	100V MOV varistor		87063/038
V100ZA4	100V MOV varistor		87063/039
V100ZA05	100V MOV varistor		87063/037
V100ZA15	100V MOV varistor		87063/040
V120ZA1	120V MOV varistor		87063/042
V120ZA4	12V MOV varistor		87063/043
V120ZA6	120V MOV varistor		87063/044
V120ZA05	120V MOV varistor		87063/041
V130LA2	130V MOV varistor		
V130LA10A	130V MOV varistor		
V130LA20A	130V MOV varistor		
V130LA20B	130V MOV varistor	M83530/1-2000B	
V150LA2	150V MOV varistor		
V150LA10A	150V MOV varistor		
V150LA20B	150V MOV varistor	M83530/1-2200D	
V150ZA1	150V MOV varistor		87063/046
V150ZA4	150V MOV varistor		87063/047
V150ZA8	150V MOV varistor		87063/048
V150ZA05	150V MOV varistor		87063/045
V180ZA05	180V MOV varistor		87063/049
V180ZA1	180V MOV varistor		87063/050
V180ZA5	180V MOV varistor		87063/051
V180ZA10	180V MOV varistor		87063/052
V250LA2CA	250V MOV varistor		
V250LA4	250V MOV varistor		
V250LA40B	250V MOV varistor		
V275LA40B	275 MOV varistor	M83530/1-4300E	

Hi-Rel Product Device Type Index

Device Type	Description	JAN No.	SMD/ DESC No.
V320LA40B	320V MOV varistor	M83530/1-5100E	
V420LA20A	420V MOV varistor		
V420LA40B	420V MOV varistor		
V480LA40A	480V MOV varistor		
V480LA80B	480V MOV varistor		
V510LA40A	510V MOV varistor		
V510LA80B	510V MOV varistor		

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
7702301EA	CD4520B	Dual binary up counter
7702501EA	CD4094B	8-stage shift-and-store bus register
7703201JA	CD4515B	4-bit latch/4-to-16-line decoder (outputs low)
7703701EA	CD4585B	4-bit magnitude comparator
7703901	LM4250	Programmable op-amp
7704402CA	CD4078B	8-bit NOR/OR Gate
7704602CA	CD4093B	Quad 2-input NAND Schmitt Trigger
7704701EA	CD4555B	Dual 1-of-4 decoder/demultiplexer (outputs high)
7704801EA	CD4556B	Dual 1-of-4 decoder/demultiplexer (outputs low)
7705201EA	IH6108MDE	8-channel CMOS analog multiplexer
7705201EC	HI1-0508	8 channel CMOS analog mux
7705202EA	HI1-0548	8 channel CMOS analog mux
77052022A	HI4-0548	8 channel CMOS analog mux
7705203EA	IH6108MJE	8-channel CMOS analog multiplexer
7800302	HA2-2640	High voltage op-amp
7800302	HA4-2640	High voltage op-amp
7800302	HA7-2640	High voltage op-amp
7800302GC	HA2-2640	High voltage op-amp
7801401CA	DG129	4-ch decoded JFET SW driver
78029013A	HD4-15530	Manchester encoder-decoder
7802901JA	HD1-15530	Manchester encoder-decoder
7901501EA	CD4052B	4 channel analog multiplexer/ demultiplexer
7901502EA	CD4052B	4 channel analog multiplexer/ demultiplexer
8001601	HA1-2420	High speed sample and hold
8001601	HA4-2420	High speed sample and hold
8001601CA	HA1-2420	High speed sample and hold
8100601EA	IH5040MJE	SPST 75 ohm high-level CMOS analog switch
8100602EA	IH5041MJE	Dual SPST 75 ohm high-level CMOS analog switch
8100603EA	IH5042MJE	SPDT 75 ohm high-level CMOS analog switch
8100604EA	IH5043MJE	Dual SPDT 75 ohm high-level CMOS analog switch
8100605EA	IH5044MJE	DPST 75 ohm high-level CMOS analog switch
8100606EA	IH5045MJE	Dual DPST 75 ohm high-level CMOS analog switch
8100607EA	IH5046MJE	DPDT 75 ohm high-level CMOS analog switch
8100608EA	IH5047MJE	4PST 75 ohm high-level CMOS analog switch
8100609EA	HI1-5040	Single SPST CMOS analog switch

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
8100609EA	IH5140MJE	SPST high-level CMOS analog switch
8100610EA	HI1-5041	Dual SPST CMOS analog switch
8100610EA	IH5141MJE	Dual SPST high-level CMOS analog switch
8100611EA	HI1-5042	Single SPDT CMOS analog switch
8100611EA	IH5142MJE	SPDT high-level CMOS analog switch
81006122A	HI4-5043	Dual SPDT CMOS analog switch
8100612EA	HI1-5043	Dual SPDT CMOS analog switch
8100612EA	IH5143MJE	Dual SPDT high-level CMOS analog switch
8100613EA	HI1-5044	Single SPST CMOS analog switch
8100613EA	IH5144MJE	DPST high-level CMOS analog switch
81006142A	HI4-5045	Dual DPST CMOS analog switch
8100614EA	HI1-5045	Dual DPST CMOS analog switch
8100614EA	IH5145MJE	Dual DPST high-level CMOS analog switch
8100615EA	HI1-5046	Single DPDT CMOS analog switch
8100615EA	IH5046MJE	DPDT 75 ohm high-level CMOS analog switch
8100616EA	HI1-5047	DPDT CMOS analog switch
8100616EA	IH5047MJE	4SPT 75 ohm high-level CMOS analog switch
8100617EA	HI1-5046A	Single DPDT CMOS analog switch
8100618EA	HI1-5047A	DPDT CMOS analog switch
8100619EA	HI1-5048	Dual SPST CMOS analog switch
8100619EA	IH5148MJE	Dual SPST high-level CMOS analog switch
8100620EA	HI1-5049	Dual DPST CMOS analog switch
8100620EA	IH5149MJE	Dual DPST high-level CMOS analog switch
8100621EA	HI1-5050	SPDT CMOS analog switch
8100621EA	IH5150MJE	CMOS analog switch
81006222A	HI4-5051	Dual SPDT CMOS analog switch
8100622EA	HI1-5051	Dual SPDT CMOS analog switch
8100622EA	IH5150MJE	CMOS analog switch
8101601EA	CD4029B	Presettable up/down counter
8101701EA	CD4035B	4-stage parallel in/parallel out shift register
8101801EA	CD4053B	Triple 2 channel analog multiplexer demultiplexer
8102001CA	CD4047B	Monostable/A-stable multivibrator
8102401VA	HM1-6504S	4K x 1 synchronous RAM
8102402VA	HM1-6514S	1K x 4 synchronous RAM
8102403VA	HM1-6504B	4K x 1 synchronous RAM
8102404VA	HM1-6514B	1K x 4 synchronous RAM
8102405VA	HM1-6504	4K x 1 synchronous RAM
8102406VA	HM1-6514	1K x 4 synchronous RAM

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
8403601JA	HM1-6516	2K x 8 synchronous RAM
8403601ZA	HM4-6516	2K x 8 synchronous RAM
8403602JA	HM1-65162	2K x 8 asynchronous RAM
8403602ZA	HM4-65162	2K x 8 asynchronous RAM
8403603JA	HM1-65162C	2K x 8 asynchronous RAM
8403603ZA	HM4-65162C	2K x 8 asynchronous RAM
8403606JA	HM1-65162B	2K x 8 asynchronous RAM
8403606ZA	HM4-65162B	2K x 8 asynchronous RAM
8403607JA	HM1-6516B	2K x 8 synchronous RAM
8403607ZA	HM4-6516B	2K x 8 synchronous RAM
8403701CA	CD54HC/HCT00	Quad 2-input NAND gate
8403801CA	CD54HC/HCT10	Triple 3-input NAND gate
8403901CA	CD54HC/HCT20	Dual 4-input NAND gate
8404001CA	CD54HC/HCT30	8-input NAND gate
8404101CA	CD54HC/HCT02	Quad 2-input NOR gate
8404201CA	CD54HC/HCT27	Triple 3-input NOR gate
8404301CA	CD54HC/HCT7266	Quad exclusive NOR
8404401CA	CD54HC/HCT4002	Dual 4-input NOR gate
8404501CA	CD54HC/HCT32	Quad 2-input OR gate
8404601CA	CD54HC/HCT86	Quad 2-input exclusive OR gate
8404701CA	CD54HC/HCT08	Quad 2-input AND gate
8404801CA	CD54HC/HCT11	Triple 3-input AND gate
8405201QA	MD80C86	Static 16-bit microprocessor
8405202QA	MD80C86-2	Static 16-bit microprocessor
8405202QA	MR80C86-2	Static 16-bit microprocessor
8405201XA	MR80C86	Static 16-bit microprocessor
8405601CA	CD54HC/HCT74	Dual D flip-flop w/set and reset
8406201EA	CD54HC/HCT138	3-to-8-line decoder/demultiplexer, inverting
8406401EA	CD54HC/HCT147	10-to-4-line priority encoder
84065013A	MR82C54	Programmable interval timer
8406501JA	MD82C54	Programmable interval timer
8406601QA	MD82C55A-5	Programmable peripheral interface
8406601XA	MR82C55A-5	Programmable peripheral interface
8406602QA	MD82C55A	Programmable peripheral interface
8406602XA	MR82C55A	Programmable peripheral interface
84067012A	MR82C82	Octal latching bus driver
8406701RA	MD82C82	Octal latching bus driver
8406702RA	MR82C83H	Octal latching inverting bus driver
8406702RA	MD82C83H	Octal latching inverting bus driver
84068012A	MR82C84H	Clock generator driver
8406801VA	MD82C84A	Clock generator driver
8406801VA	MD82C84A	Clock generator driver
84069012A	MR82C88	Bus controller
8406901RA	MD82C88	Bus controller
8407001EA	CD54HC/HCT75	Quad bistable transparent latch
8407101RA	CD54HC/HCT374	Octal D-type flip-flop, 3-state
8407201RA	CD54HC/HCT373	Octal transparent latch, 3-state
8407301EA	CD54HC/HCT174	Hex D-type flip-flop w/reset

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
8407401RA	CD54HC/HCT240	Octal buffer/line driver, 3-state, inverting
8407501EA	CD54HC/HCT161	Synchronous 4-bit binary counter, asynchronous reset
8407601EA	CD54HC/HCT163	Synchronous 4-bit binary counter, synchronous reset
8408501RA	CD54HC/HCT245	Octal bus tranceiver, 3-state
8408801EA	CD54HC/HCT112	Dual J-K flip-flop w/set and reset
8408901EA	CD54HC/HCT175	Quad D-type flip-flop w/reset
8409001CA	CD54HC/HCT243	Quad bus tranceiver, 3-state
8409101CA	CD54HC/HCT14	Hex inverting Schmitt Trigger
8409201EA	CD54HC/HCT139	Dual 2-of-4-line decoder/ demultiplexer
8409301EA	CD54HC/HCT153	Dual 4-input multiplexer
8409401EA	CD54HC/HCT162	Synchronous BCD decade counter, asynchronous reset
8409501EA	CD54HC/HCT165	8-bit parallel-in/serial-out shift register
8409601RA	CD54HC/HCT244	Octal buffer/line driver, 3-state
8409801CA	CD54HC/HCT04	Hex inverter
8409901RA	CD54HC/HCT273	Octal D-type flip-flop w/reset
8410001CA	CD54HC/HCT393	Dual 4-bit binary ripple counter
8412801EA	CD54HC/HCT151	8-Input multiplexer
8415001EA	CD54HC/HCT109	Dual J-K flip-flop w/set and reset
8416201CA	CD54HC/HCT164	8-bit serial-in/parallel-out shift register
8500101EA	CD54HC/HCT365	Hex buffer/line driver, 3-state
8500201EA	CD54HC/HCT367	Hex buffer/line driver, 3-state
8500301EA	CD54HC/HCT4020	14-stage binary ripple counter
8500401EA	CD54HC/HCT4040	12-bit binary ripple counter
85015013A	MR82C52	Serial controller interface
8501501XA	MD82C52	Serial controller interface
85016013A	MR82C59A-5	Priority interrupt controller
8501601YA	MD82C59A-5	Priority interrupt controller
85016023A	MR82C59A	Priority interrupt controller
8501602YA	MD82C59A	Priority interrupt controller
8512401EA	CD54HC/HCT257	
8512501EA	CD54HC/HCT251	8-input multiplexer, 3-state
8512801RA	CD54HC/HCT573	Octal transparent latch, 3-state
8513001RA	CD54HC/HCT244	Octal buffer/line driver, 3-state
5962-85131013A	HI4-0546	16 channel CMOS analog mux
5962-8513101XA	HI1-0546	16 channel CMOS analog mux
5962-85131023A	HI4-0547	8 channel CMOS differential analog mux
5962-8513102XA	HI1-0547	8 channel CMOS differential analog mux
5962-85131032A	HI4-0549	4 channel CMOS differential analog mux
5962-8513103EA	HI1-0549	4 channel CMOS differential analog mux

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
8550401EA	CD54HC/HCT138	3-to-8-line decoder/demultiplexer, inverting
8550501RA	CD54HC/HCT240	Octal buffer/line driver, 3-state, inverting
8550601RA	CD54HC/HCT245	Octal buffer tranceiver, 3-state
8550701RA	CD54HC/HCT374	Octal D-type flip-flop, 3-state
8551901EA	CD54HC/HCT259	8-bit addressable hatch
8552514XA	HM1-65642	8K x 8 asynchronous RAM
8552514YA	HM4-65642	8K x 8 asynchronous RAM
8600901EA	CD54HC/HCT390	Dual decade ripple counter
8601001CA	CD54HC/HCTU04	Hex inverter (unbuffered)
8601101EA	CD54HC/HCT4017	Johnson decade counter w/10 decoded outputs
8601201CA	CD54HC/HCT4024	7-stage binary ripple counter
8601301EA	CD54HC/HCT85	4-bit magnitude comparator
8607601EA	CD54HC/HCT163	Synchronous 4-bit binary counter, synchronous reset
8607701CA	CD54HC/HCT280	9-bit odd/even parity generator/ checker
86879013A	HS4-3182	ARINC 429 bus interface line driver
8687901EA	HS1-3182	ARINC 429 bus interface line driver
8688001QA	HS1-3282	ARINC 429 bus interface
8688001XA	HS4-3282	ARINC 429 bus interface
87063/001	V22ZA05	122V MOV varistor
87063/002	V22ZA1	122V MOV varistor
87063/003	V22ZA2	122V MOV varistor
87063/004	V22ZA3	122V MOV varistor
87063/005	V24ZA50	122V MOV varistor
87063/006	V27ZA05	27V MOV varistor
87063/007	V27ZA1	27V MOV varistor
87063/008	V27ZA2	27V MOV varistor
87063/009	V27ZA4	27V MOV varistor
87063/010	V27ZA60	27V MOV varistor
87063/011	V33ZA05	33V MOV varistor
87063/012	V33ZA1	33V MOV varistor
87063/013	V33ZA2	33V MOV varistor
87063/014	V33ZA5	33V MOV varistor
87063/015	V33ZA70	33V MOV varistor
87063/016	V36ZA80	36V MOV varistor
87063/017	V39ZA05	39V MOV varistor
87063/018	V39ZA1	39V MOV varistor
87063/019	V39ZA3	39V MOV varistor
87063/020	V39ZA6	39V MOV varistor
87063/021	V47ZA05	47V MOV varistor
87063/022	V47ZA1	47V MOV varistor
87063/023	V47ZA3	47V MOV varistor
87063/024	V47ZA7	47V MOV varistor
87063/025	V56ZA05	56V MOV varistor
87063/026	V56ZA2	56V MOV varistor
87063/027	V56ZA3	56V MOV varistor

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
87063/028	V56ZA8	56V MOV varistor
87063/029	V68ZA05	68V MOV varistor
87063/030	V68ZA2	68V MOV varistor
87063/031	V68ZA3	68V MOV varistor
87063/032	V68ZA10	68V MOV varistor
87063/033	V82ZA05	82V MOV varistor
87063/034	V82ZA2	82V MOV varistor
87063/035	V82ZA4	82V MOV varistor
87063/036	V82ZA12	82V MOV varistor
87063/037	V100ZA05	100V MOV varistor
87063/038	V100ZA3	100V MOV varistor
87063/039	V100ZA4	100V MOV varistor
87063/040	V100ZA15	100V MOV varistor
87063/041	V120ZA05	12V MOV varistor
87063/042	V120ZA1	12V MOV varistor
87063/043	V120ZA4	12V MOV varistor
87063/044	V120ZA6	12V MOV varistor
87063/045	V150ZA05	150V MOV varistor
87063/046	V150ZA1	150V MOV varistor
87063/047	V150ZA4	150V MOV varistor
87063/048	V150ZA8	150V MOV varistor
87063/049	V180ZA05	180V MOV varistor
87063/050	V180ZA1	180V MOV varistor
87063/051	V180ZA5	180V MOV varistor
87063/052	V180ZA10	180V MOV varistor
88690013A	HM4-6642	512 x 8 fuse link PROM
8869001JA	HM1-6642	512 x 8 fuse link PROM
8869001LA	HM6-6642	512 x 8 fuse link PROM
88690023A	HM4-6642B	512 x 8 fuse link PROM
8869002JA	HM1-6642B	512 x 8 fuse link PROM
8869002LA	HM6-6642B	512 x 8 fuse link PROM
89007	2N7123	100V/40A N-CH MOSFET
89007	2N7124	200V/30A N-CH MOSFET
89007	2N7125	400V/15A N-CH MOSFET
89007	2N7126	500V/13A N-CH MOSFET
89009	2N7119	100V/14A N-CH MOSFET
89009	2N7120	200V/9A N-CH MOSFET
89009	2N7121	400V/5.5A N-CH MOSFET
89025	2N7241	100V/14A N-CH MOSFET
89025	2N7242	200V/9A N-CH MOSFET
89025	2N7243	400V/5.5A N-CH MOSFET
89025	2N7244	500V/4.5A N-CH MOSFET
89026	2N7224	100V/30A N-CH MOSFET
89026	2N7225	200V/27A N-CH MOSFET
89026	2N7227	400V/14A N-CH MOSFET
89026	2N7227	500V/12A N-CH MOSFET
8954001JA	HM1-6617	2K x 8 fuse link PROM
8954001LA	HM6-6617	2K x 8 fuse link PROM
8954001XA	HM4-6617	2K x 8 fuse link PROM
8954002JA	HM1-6617B	2K x 8 fuse link PROM

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
9055701EA	CD4538B	Dual precision monostable multivibrator
9064002EA	CD4016B	Quad bilateral switch
5692-85016023A	MR82C59A	Priority interrupt controller
5692-8501602YA	MD82C59A	Priority interrupt controller
5962-85016013A	MR82C59A-5	Priority interrupt controller
5962-8501601YA	MD82C59A-5	Priority interrupt controller
5962-85016023A	MR82C59A	Priority interrupt controller
5962-8501602YA	MD82C59A	Priority interrupt controller
5962-8512704XA	HI1-574A	12 bit A to D converter
5962-8512704YA	HI4-574A	12 bit A to D converter
5962-85131013A	HI4-0546	16 channel CMOS analog mux
5962-8513101XA	HI1-0546	16 channel CMOS analog mux
5962-85131023A	HI4-0547	8 channel CMOS differential analog mux
5962-8513102XA	HI1-0547	8 channel CMOS differential analog mux
5962-85131032A	HI4-0549	4 channel CMOS differential analog mux
5962-8513103EA	HI1-0549	4 channel CMOS differential analog mux
5962-8513104XA	IH5116MJI	16-channel fault protected CMOS analog multiplexer
5962-8513105XA	IH5216MJI	8-channel differential fault protected CMOS analog multiplexer
5962-8513106EA	IH5208MJE	4-channel CMOS differential analog mux
5962-8515301CA	CD54HC/HCT73	Dual J-K flip-flop w/reset
5962-8515401CA	CD54HC/HCT107	Dual J-K flip-flop w/reset
5962-85528012A	MR82C89	Bus arbiter
5962-8552801RA	MD82C89	Bus arbiter
5962-8606101EA	CD54HC/HCT157	Quad 2-input multiplexer
5962-8606201RA	CD54HC/HCT563	Octal transparent latch, 3-state, inverting
5962-861001CA	CD54HC/HCTU04	Hex inverter (unbuffered)
5962-8670101JX	CD54HC/HCT154	4-to-16 line decoder/demultiplexer
5962-86716012A	HI4-0201HS	High speed quad SPST CMOS analog switch
5962-8671601EA	HI1-0201HS	High speed quad SPST CMOS analog switch
5962-8681201EA	CD54HC/HCT368	Hex buffer/line driver, 3-state, inverting
5962-8681301RA	CD54HC/HCT533	Octal transparent latch, 3-state, inverting
5962-8681401RA	CD54HC/HCT534	Octal D-type flip-flop, 3-state, inverting
5962-8681501RA	CD54HC/HCT564	Octal D-type flip-flot, 3-state, inverting
5962-8681701EA	CD54HC/HCT597	8-bit shift register with I/P latch
5962-8681801RA	CD54HC/HCT688	8-bit magnitude comparator
5962-8681901EA	CD54HC/HCT4049	Hex inverting HIGH-to-LOW level shifter

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
5962-8682001EA	CD54HC/HCT4050	Hex HIGH-to-LOW level shifter
5962-8682101EA	CD54HC/HCT42	
5962-8682201JA	CD54HC/HCT154	4-to-16 line decoder/demultiplexer
5962-8682301EA	CD54HC/HCT158	Quad 2-input multiplexer, inverting
5962-8682401EA	CD54HC/HCT160	Synchronous BCD decade counter, asynchronous reset
5962-8682501EA	CD54HC/HCT173	Quad D-type flip-flop, 3-state
5962-8682601EA	CD54HC/HCT194	4-bit bidirectional universal shift register
5962-8682701EA	CD54HC/HCT195	4-bit parallel access shift register
5962-8682801EA	CD54HC/HCT366	Hex buffer/line driver, 3-state, inverting
5962-8683101CX	CD54HC/HCT00	Quad 2-input NAND gate
5962-86684701EA	CD54HC/HCT123	Dual retriggerable monostable multivibrator w/reset
5962-8684801CA	CD54HC/HCT126	Quad 3-state buffer
5962-8685201CX	CD54HC/HCT32	Quad 2-input OR gate
5962-8685301CX	CD54HC/HCT74	Dual D flip-flop w/set and reset
5962-8685401EX	CD54HC/HCT161	Synchronous 4-bit binary counter, asynchronous reset
5962-8685501EX	CD54HC/HCT165	8-bit parallel-in serial-out shift register
5962-8685601RX	CD54HC/HCT573	Octal transparent latch, 3-state
5962-8685701RX	CD54HC/HCT688	8-bit magnitude comparator
5962-8686001	HA1-4902	Precision quad comparator
5962-8686001	HA4-4902	Precision quad comparator
5962-8686701RX	CD54HC/HCT373	Octal transparent latch, 3-state
5962-8688301CX	CD54HC/HCT08	Quad 2-input AND gate
5962-8688401EA	CD54HC/HCT238	3-to-8 line decoder/demultiplexer
5962-8688501JA	CD54HC/HCT646	Octal bus transceiver/register, 3-state
5962-8686001	HAI-4902	Precision quad comparator
5962-8688601EA	CD54HC/HCT4538	Dual precision monostable multivibrator
5962-8689001EX	CD54HC/HCT14	Hex inverting Schmitt Trigger
5962-8689101EA	CD54HC/HCT191	Synchronous 4-bit binary up/down counter
5962-8752501CA	CD54AC/ACT74	Dual D flip-flop w/set and reset
5962-8754901CA	CD54AC/ACT00	Quad 2-input NAND gate
5962-8755001RA	CD54AC/ACT240	Octal buffer line driver, 3-state, inverting
5962-8755101RA	CD54AC/ACT241	Octal buffer line driver, 3-state
5962-8755201RA	CD54AC/ACT244	Octal buffer line driver, 3-state
5962-8755301EA	CD54AC/ACT139	Dual 2-of-4 line decoder/demultiplexer
5962-8755501RA	CD54AC/ACT273	Octal D-type flip-flop w/reset
5962-8755601RA	CD54AC/ACT273	Octal D-type flip-flop w/reset
5462-8756301JA	ICM7170MDG	Micro P-compatible real time clock
5462-8756301JC	ICM7170MDG	Micro P-compatible real time clock
5962-87577012A	MR82C86H-5	Octal bus transceivers
5962-8757701RA	MD82C86H-5	Octal bus transceivers

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
5962-87577022A	MR82C87H-5	Octal bus transceivers
5962-8757702RA	MD82C87H-5	Octal bus transceivers
5962-8760901CA	CD54AC/ACT04	Hex inverter/buffer
5962-8761401CA	CA54AC/ACT32	Quad 2-input OR gate
5962-8761501CA	CD54AC/ACT08	Quad 2-input AND gate
5962-8762201EA	CD54AC/ACT138	3-to-8 line decoder/demultiplexer, inverting
5962-8762301EA	CD54AC/ACT139	Dual 2-of-4 line decoder/ demultiplexer
5962-8762601EA	CD54AC/ACT174	Hex D-type flip-flop w/reset
5962-8764701CA	CD54HC/HCT03	Quad 2-input NAND gate w/open collector
5962-8766001	ICL7667	Dual power MOS driver
5962-8766301RA	CD54AC/ACT245	Octal bus tranceiver, 3-state
5962-8767701	HA1-5330	High speed sample and hold
5962-8767701	HA4-5330	High speed sample and hold
5962-8768001EA	CD54HC/HCT4060	14-stage binary ripple counter w/ oscillator
5962-8769401RA	CD54AC/ACT374	Octal D flip-flop, 3-state
5962-8769501RA	CD54AC/ACT540	Octal buffer line driver, 3-state, inverting
5962-8769901CA	CD54AC/ACT00	Quad 2-input NAND gate
5962-8772101CA	CD54HC/HCT125	Quad 3-state buffer
5962-8772201CA	CD54HC/HCT4075	Triple 3-input OR gate
5962-8772401EA	CD54HC/HCT192	Synchronous BCD decade up/down counter
5962-8772401EX	CD54HC/HCT193	Synchronous 4-bit binary up/down counter
5962-8772501RX	CD54HC/HCT273	Octal D-type flip-flop w/reset
5962-8773301EA	CD54HC/HCT4511	BCD-to-7 segment latch/decoder/ driver
5962-8775401EA	CD54HC/HCT4053	Triple 2 channel analog multiplexer/ demultiplexer
5962-8775601RA	CD54AC/ACT273	Octal D-type flip-flop w/reset
5962-8775701EA	CD54AC/ACT174	Hex D-type flip-flop w/reset
5962-8775801RA	CD54AC/ACT245	Octal bus tranceiver, 3-state
5962-8775901RA	CD54AC/ACT240	Octal buffer line driver, 3-state, inverting
5962-8776001RA	CD54AC/ACT244	Octal buffer line driver, 3-state
5962-8778301	HA-2400	4 channel prog. op-amp
5962-8778301	HA1-2400	4 channel prog. op-amp
5962-8778301	HA4-2400	4 channel prog. op-amp
5962-8778401	HA-5190	Wideband fast setting op-amp
5962-8778401	HA1-5190	Wideband fast settling op-amp
5962-8778401	HA2-5190	Wideband fast settling op-amp
5962-8778401	HA4-5190	Wideband fast settling op-amp
5962-8778501	HA-2541	Wideband unity gain op-amp
5962-8778501	HA2-2541	Wideband unity gain op-amp
5962-8778701	HA-2539	High slew rate wideband op-amp
5962-8778701	HA1-2539	High slew rate wideband op-amp
5962-8778701	HA4-2539	High slew rate wideband op-amp

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
5962-8780501EA	CD54HC/HCT221	Dual monostable multivibrator w/ reset
5962-8780601RA	CD54HC/HCT299	8-bit universal shift register, 3-state
5962-8780701RA	CD54HC/HCT377	Octal D-type flip-flop with data enable
5962-8780901RA	CD54HC/HCT640	Octal bus transceiver, 3-state inverting
5962-8850201	HA-5104	Quad low noise hi-perf op-amp
5962-8850201	HA1-5104	Quad low noise hi-perf op-amp
5962-8850201	HA4-5104	Quad low noise hi-perf op-amp
5962-8852001CA	CD54AC/ACT74F	Dual D flip-flop w/set and reset
5962-8855601EA	CD54HC/HCT4052	Dual 4-channel analog multiplexer/ demultiplexer
5962-8857601CA	CD54HC/HCT21	Dual 4-input AND gate
5962-8860601EA	CD54HC/HCT237	3-to-8 line decoder
5962-8862401JA	CD54HC/HCT4059	Programmable divided-by-"N" counter
5962-8867101EA	CD54HC/HCT191	Synchronous 4-bit binary up/down counter
5962-8867201EX	CD54HC/HCT85	4-bit magnitude comparator
5962-8875001EA	IH5352MJE/883B	Quad video switch
5962-8875701EA	CD54HCT/HC4046A	Phase-locked loop with VCO hex inverting HIGH-to-LOW level shifter
5962-8875801CA	CD54HC/HCT4016	Quad bilateral switch
5962-8875901EA	CD54HC/HCT173	Quad D-type flip-flop, 3-state
5962-8877201	ICL8038	Waveform generator
5962-894601CA	CD54HC/HCT30	8-input NAND gate
5962-8950201	HA2-2544	Video op-amp
5962-8950201	HA4-2544	Video op-amp
5962-8950201	HA7-2544	Video op-amp
5962-8950303	ICM7555	CMOS 555 timer
5962-8950304	ICM7556	CMOS 556 dual timer
5962-8950701CA	CD54HC/HCT4066	Quad bilateral switch
5962-8954801	HA2-5102	Dual low noise hi-perf op-amp
5962-8954801	HA4-5102	Dual low noise hi-perf op-amp
5962-8954801	HA7-5102	Dual low noise hi-perf op-amp
5962-8960901EA	CD54HC/HCT4046	Phase-locked loop with VCO
5962-8962701	HA2-5127	Ultra low noise precision op-amp
5962-8962701	HA4-5127	Ultra low noise precision op-amp
5962-8962701	HA7-5127	Ultra low noise precision op-amp
5962-8962702	HA2-5137	Ultra low noise precision op-amp
5962-8962702	HA4-5137	Ultra low noise precision op-amp
5962-8962702	HA7-5137	Ultra low noise precision op-amp
5962-8962703	HA2-5147	Ultra low noise wideband op-amp
5962-8962703	HA4-5147	Ultra low noise wideband op-amp
5962-8962703	HA7-5147	Ultra low noise wideband op-amp
5962-8963101	HA-5111	Low noise hi-performance op-amp
5962-8963101	HA2-5111	Low noise hi-performance op-amp
5962-8963101	HA4-5111	Low noise hi-performance op-amp
5962-8963101	HA7-5111	Low noise hi-performance op-amp

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
5962-8963201	HA2-5112	Dual low noise hi-perf op-amp
5962-8963201	HA4-5112	Dual low noise hi-perf op-amp
5962-8963201	HA7-5112	Dual low noise hi-perf op-amp
5962-8963301	HA2-5033	Video buffer
5962-8963401	HA1-5114	Quad low noise hi-perf op-amp
5962-8963401	HA4-5114	Quad low noise hi-perf op-amp
5962-8963501	HA2-5101	Low noise hi-performance op-amp
5962-8963501	HA4-5101	Low noise hi-performance op-amp
5962-8963501	HA7-5101	Low noise hi-performance op-amp
5962-8963601	HA2-5002	Current driver op-amp
5962-8963601	HA4-5002	Current driver op-amp
5962-8963601	HA7-5002	Current driver op-amp
5962-8964301	HA2-2542	High output current op-amp
5962-8964801	HA1-2540	Wideband fast settling op-amp
5962-8964801	HA4-2540	Wideband fast settling op-amp
5962-8964901	HA2-5151	Low power op-amp
5962-8964901	HA4-5151	Low power op-amp
5962-8964901	HA7-5151	Low power op-amp
5962-8964902	HA2-5152	Dual low power op-amp
5962-8964902	HA4-5152	Dual low power op-amp
5962-8964902	HA7-5152	Dual low power op-amp
5962-8964903	HA1-5154	Quad low power op-amp
5962-8964903	HA4-5154	Quad low power op-amp
5962-8965601	HA2-5141	Ultra low power op-amp
5962-8965601	HA4-5141	Ultra low power op-amp
5962-8965601	HA7-5141	Ultra low power op-amp
5962-8965602	HA2-5142	Dual ultra low power op-amp
5962-8965602	HA4-5142	Dual ultra low power op-amp
5962-8965602	HA7-5142	Dual ultra low power op-amp
5962-8965603	HA2-5144	Quad ultra low power op-amp
5962-8965603	HA4-5144	Quad ultra low power op-amp
5962-8965603	HA7-5144	Quad ultra low power op-amp
5962-8970101EA	CD54HC/HCT175	Quad D-type flip-flop w/reset
5962-8970201EA	CD54HC/HCT112	Dual J-K flip-flop w/set and reset
5962-8970301CA	CD54HC/HCT27	Triple 3-input NOR gate
5962-8970401CA	CD54HC/HCT164	8-bit serial-in parallel-out shift register
5962-8970501EA	CD54HC/HCT257	Quad 2-input multiplexer, 3-state
5962-8970701EA	CD54HC/HCT162	Synchronous BCD decade counter, synchronous reset
5962-8970801EA	CD54HC/HCT258	Quad 2-line-to-4-line data selector
5962-8970901CA	CD54HC/HCT11	Triple 3-input AND gate
5962-8972101	HA2-2529	High output current op-amp
5962-8972101	HA4-2529	High output current op-amp
5962-8972101	HA7-2529	High output current op-amp
5962-8974101EA	CD54HC/HCT597	8-bit shift register with I/P latch
5962-8974501EA	CD54HC/HCT238	3-to-8 line decoder/demultiplexer
5962-8974701CA	CD54HC/HCT04	Hex inverter
5962-8975101EA	CD54HC/HCT02	Quad 2-input NOR gate

Hi-Rel Product SMD/DESC Number Index

SMD/DESC No.	Device Type	Product Description
5962-8984201	ICL8211	Voltage reference/indicator
5962-8984202	ICL8212	Voltage reference/indicator
5962-8984301CA	CD54HC/HCT10	Triple 3-input NAND gate
5962-8984501CA	CD54HC/HCT132	Quad 2-input NAND Schmitt Trigger
5962-8984901RA	CD54HC/HCT534	Octal D-type flip-flop, 3-state, inverting

Hi-Rel Product JAN Number Index

JAN No.	Device Type	Product Description
JM38510/10501BEA	IH5040MDE	SPST 75 ohm high-level CMOS analog switch
JM38510/10502BEA	IH5041MDE	Dual SPST 75 ohm high-level CMOS analog switch
JM38510/10503BEA	IH5042MDE	SPDT 75 ohm high-level CMOS analog switch
JM38510/10504BEA	IH5043MDE	Dual SPDT 75 ohm high-level CMOS analog switch
JM38510/10505BEA	IH5044MDE	DPST 75 ohm high-level CMOS analog switch
JM38510/10506BEA	IH5045MDE	Dual DPST 75 ohm high-level CMOS analog switch
JM38510/11101BAC	DG181AL	Dual SPST 30 ohm hi-speed driver with JFET SW
JM38510/11101BCA	DG181AP	Dual SPST 30 ohm hi-speed driver with JFET SW
JM38510/11101BIA	DG181AA	Dual SPST 30 ohm hi-speed driver with JFET SW
JM38510/11102BAC	DG182AL	Dual SPST 75 ohm hi-speed driver with JFET SW
JM38510/11102BCA	DG182AP	Dual SPST 75 ohm hi-speed driver with JFET SW
JM38510/11102BIA	DG182AA	Dual SPST 75 ohm hi-speed driver with JFET SW
JM38510/11103BAC	DG184AL	Dual DPST 30 ohm hi-speed driver with JFET SW
JM38510/11103BEA	DG184AP	Dual DPST 30 ohm hi-speed driver with JFET SW
JM38510/11104BAC	DG185AL	Dual DPST 75 ohm hi-speed driver with JFET SW
JM38510/11104BEA	DG185AP	Dual DPST 75 ohm hi-speed driver with JFET SW
JM38510/11105BAC	DG187AL	SPDT 30 ohm hi-speed driver with JFET SW
JM38510/11105BCA	DG187AP	SPDT 30 ohm hi-speed driver with JFET SW
JM38510/11105BIA	DG187AA	SPDT 30 ohm hi-speed driver with JFET SW
JM38510/11106BAC	DG188AL	SPDT 75 ohm hi-speed driver with JFET SW
JM38510/11106BCA	DG188AP	SPDT 75 ohm hi-speed driver with JFET SW
JM38510/11106BIA	DG188AA	SPDT 75 ohm hi-speed driver with JFET SW
JM38510/11107BAC	DG190AL	Dual SPDT 30 ohm hi-speed driver with JFET SW
JM38510/11107BEA	DG190AP	Dual SPDT 30 ohm hi-speed driver with JFET SW
JM38510/11108BAC	DG191AL	Dual SPDT 75 ohm hi-speed driver with JFET SW
JM38510/11108BEA	DG191AP	Dual SPDT 75 ohm hi-speed driver with JFET SW

Hi-Rel Product JAN Number Index

JAN No.	Device Type	Product Description
JM38510/11601BCA	DG300AAP	TTL compatible CMOS analog SW
JM38510/11602BCA	DG301AAP	TTL compatible CMOS analog SW
JM38510/11603BCA	DG302AAP	TTL compatible CMOS analog SW
JM38510/11604BCA	DG303AAP	TTL compatible CMOS analog SW
JM38510/12202BGC	HA2-2600	Wideband high impedence amp
JM38510/12203BGC	HA2-2620	Wideband (uncomp) amp
JM38510/12204BGC	HA2-2500	Precision high slew rate amp
JM38510/12205BGC	HA2-2510	High slew rate amp
JM38510/12206BGC	HA2-2520	High slew rate (uncomp) amp
JM38510/12302BEA	HI1-0201	Quad SPST CMOS analog switch
JM38510/12302BEA	DG201	Quad SPST CMOS analog SW
JM38510/19001BXA	HI1-0506	Single 16-Ch CMOS analog mux
JM35510/19002BXA	HI1-0546	Single 16-Ch CMOS analog mux
JM35510/19003BXA	HI1-0507	Differential 8-Ch CMOS analog mux
JM35510/19004BXA	HI1-0547	Differential 8-Ch CMOS analog mux
JM35510/19005BEA	HI1-0548	Single 8-Ch CMOS analog mux
JM38510/19006BEA	HI1-0549	Differential 4-Ch CMOS analog mux
JM38510/19007BEA	HI1-0508	8 channel CMOS analog mux
JM38510/19008BEA	HI1-0509	4 channel CMOS differential analog mux
MIL-R-83530/1-2000B	V130LA20B	130V MOV varistor
MIL-R-83530/1-2200D	V150LA20B	150V MOV varistor
MIL-R-83530/1-4300E	V275LA40B	250V MOV varistor
MIL-R-83530/1-5100E	V320LA40B	320V MOV varistor
MIL-M-38510/12702	AD7520UD	CMOS 10-bit multiplying D/A
MIL-M-38510/17001	CD4081B	Quad 2-input AND gate
MIL-M-38510/17002	CD4082B	Dual 4-input AND gate
MIL-M-38510/17003	CD4073B	Triple 3-input AND gate
MIL-M-38510/17101	CD4071B	Quad 2-input OR gate
MIL-M-38510/17102	CD4072B	Dual 4-input OR gate
MIL-M-38510/17103	CD4075B	Triple 3-input OR gate
MIL-M-38510/17201	CD4085B	Dual 2-wide, 2-input AND/OR/INVERT (AOI) gate
MIL-M-38510/17202	CD4086B	Expandable 4-wide, 2-input AND/OR/INVERT (AOI) gate
MIL-M-38510/17203	CD4070B	Quad exclusive-OR gate
MIL-M-38510/17204	CD4077B	Quad exclusive-NOR gate

Hi-Rel Product JAN Number Index

JAN No.	Device Type	Product Description
MIL-M-38510/17401	CD4069UB	Hex inverter
MIL-M-38510/17403	CD4502B	Strobed hex inverter/buffer
MIL-M-38510/17504	CD4098B	Dual monostable multivibrator
MIL-M-38510/17601	CD4099B	8-bit addressable latch
MIL-M-38510/24501BVA	HM1-6504S	4K x 1 synchronous RAM
MIL-M-38510/24502BVA	HM1-6514S	1K x 4 synchronous RAM
MIL-M-38510/29102BJA	HM1-6516	2K x 8 synchronous RAM
MIL-M-38510/29102BXA	HM4-6516	2K x 8 synchronous RAM
MIL-M-38510/29103BRA	HM1-65262	16K x 1 asynchronous RAM
MIL-M-38510/29103BYA	HM4-65262	16K x 1 asynchronous RAM
MIL-M-38510/29104BJA	HM1-65162	2K x 8 asynchronous RAM
MIL-M-38510/29104BXA	HM4-65162	2K x 8 asynchronous RAM
MIL-M-38510/29109BRA	HM1-65262B	16K x 1 asynchronous RAM
MIL-M-38510/29109BYA	HM4-65262B	16K x 1 asynchronous RAM
MIL-M-38510/29110BJA	HM1-65162B	2K x 8 asynchronous RAM
MIL-M-38510/29110BXA	HM4-65161B	
MIL-M-38510/29205BXA	HM1-65642B	8K x 8 asynchronous RAM
MIL-M-38510/29205BYA	HM4-65642B	8K x 8 asynchronous RAM
MIL-M-38510/05001	CD4011A	Quad 2-input NAND gate
MIL-M-38510/05002	CD4012A	Dual 4-input NAND gate
MIL-M-38510/05003	CD4023A	Triple 3-input NAND gate
MIL-M-38510/05051	CD4011B	Quad 2-input NAND gate
MIL-M-38510/05052	CD4012B	Dual 4-input NAND gate
MIL-M-38510/05053	CD4023B	Triple 3-input NAND gate
MIL-M-38510/05101	CD4013A	Dual "D" flip-flops with set/ reset capability
MIL-M-38510/05102	CD4027A	Dual "J-K" flip-flop with set/ reset capability
MIL-M-38510/05151	CD4013B	Dual "D" flip-flops with set/ reset capability
MIL-M-38510/05152	CD4027B	Dual "J-K" flip-flop with set/ reset capability
MIL-M-38510/05201	CD4000A	Dual 3 input NOR gate plus inverter
MIL-M-38510/05202	CD4001A	Quad 2 input NOR gate
MIL-M-38510/05203	CD4002A	Dual 4 input NOR gate
MIL-M-38510/05204	CD4025A	Triple 3-input NOR gate
MIL-M-38510/05251	CD4000B	Dual 3 input NOR gate plus inverter
MIL-M-38510/05252	CD4001B	Quad 2 input NOR gate
MIL-M-38510/05253	CD4002B	Dual 4 input NOR gate
MIL-M-38510/05254	CD4025B	Triple 3-input NOR gate
MIL-M-38510/05301	CD4007A	Dual complementary pair plus inverter
MIL-M-38510/05302	CD4019A	Quad AND/OR select gate
MIL-M-38510/05351	CD4007UB	Dual complementary pair plus inverter
MIL-M-38510/05352	CD4019B	Quad AND/OR select gate
MIL-M-38510/05401	CD4008A	

Hi-Rel Product JAN Number Index

JAN No.	Device Type	Product Description
MIL-M-38510/05451	CD4008B	4 Bit full adder with parallel carry out
MIL-M-38510/05503	CD4049A	Hex buffer/converter (inverting)
MIL-M-38510/05504	CD4050A	Hex buffer/converter (non-inverting)
MIL-M-38510/05553	CD4049UB	Hex buffer/converter (inverting)
MIL-M-38510/05554	CD4050B	Hex buffer/converter (non-inverting)
MIL-M-38510/05555	CD4041UB	Quad true/complement buffer
MIL-M-38510/05601	CD4017A	Decade counter/divider
MIL-M-38510/05603	CD4020A	14-stage binary ripple counter
MIL-M-38510/05604	CD4022A	Divide-by-8 counter/divider
MIL-M-38510/05605	CD4024A	7-stage binary ripple counter
MIL-M-38510/05651	CD4017B	Decode counter/divider
MIL-M-38510/05652	CD4018B	Presettable divide by "N" counter
MIL-M-38510/05653	CD4020B	14-stage binary ripple counter
MIL-M-38510/05654	CD4022B	Divide-by-8 counter/divider
MIL-M-38510/05655	CD4024B	7-stage binary ripple counter
MIL-M-38510/05701	CD4006A	18-stage static shift register
MIL-M-38510/05702	CD4014A	8-stage static shift register
MIL-M-38510/05703	CD4015A	Dual 4 stage static shift register
MIL-M-38510/05704	CD4021A	8-stage static shift register
MIL-M-38510/05705	CD4031A	64-stage static shift register
MIL-M-38510/05752	CD4014B	8-stage static shift register
MIL-M-38510/05753	CD4015B	Dual 4 stage static shift register
MIL-M-38510/05754	CD4021B	8-stage static shift register
MIL-M-38510/05852	CD4066B	Quad bilateral switch
MIL-M-38510/05951	CD4028B	BCD-to-decimal decoder
MIL-S-19500/368	2N3439	350V/1A, N-P-N
MIL-S-19500/368	2N3440	250V/1A, N-P-N
MIL-S-19500/384	2N3584	250V/2A, N-P-N
MIL-S-19500/384	2N3585	300V/2A, N-P-N
MIL-S-19500/439	2N5038	90V/20A, N-P-N hi-speed
MIL-S-19500/439	2N5039	75V/20A, N-P-N
MIL-S-19500/456	2N5302	60V/30A, N-P-N
MIL-S-19500/456	2N5303	80V/30A, N-P-N
MIL-S-19500/461	2N6211	-275V/-2A, P-N-P
MIL-S-19500/461	2N6212	-300V/-2A, P-N-P
MIL-S-19500/461	2N6213	-350V/-2A, P-N-P
MIL-S-19500/485	2N5415S	-200V/-1A, P-N-P
MIL-S-19500/485	2N5416S	-300V/-1A, P-N-P
MIL-S-19500/488	2N5671	90V/30A, N-P-N
MIL-S-19500/488	2N5672	120V/30A, N-P-N hi-speed

Hi-Rel Product JAN Number Index

JAN No.	Device Type	Product Description
MIL-S-19500/498	2N6306	250V/8A, N-P-N
MIL-S-19500/498	2N6308	350V/8A, N-P-N
MIL-S-19500/504	2N6283	80V/20A, N-P-N
MIL-S-19500/504	2N6284	100V/20A, N-P-N
MIL-S-19500/505	2N6286	-80V/-20A, P-N-P
MIL-S-19500/505	2N6287	-100V/-20A, P-N-P
MIL-S-19500/523	2N6383	40V/10A, N-P-N
MIL-S-19500/523	2N6384	60V/10A, N-P-N
MIL-S-19500/523	2N6385	80V/10A, N-P-N
MIL-S-19500/525	2N6546	300V/15A, N-P-N
MIL-S-19500/525	2N6547	400V/15A, N-P-N
MIL-S-19500/526	2N3879	75V/7A, N-P-N hi-speed
MIL-S-19500/527	2N6648	-40V/-10A, P-N-P
MIL-S-19500/527	2N6649	-60V/-10A, P-N-P
MIL-S-19500/527	2N6650	-80V/-10A, P-N-P
MIL-S-19500/528	2N6032	90V/50A, N-P-N
MIL-S-19500/528	2N6033	120V/50A, N-P-N
MIL-S-19500/536	2N6671	300V/10A, N-P-N hi-speed
MIL-S-19500/536	2N6673	400V/8A, N-P-N hi-speed
MIL-S-19500/537	2N6674	300V/20A, N-P-N hi-speed
MIL-S-19500/537	2N6675	400V/20A, N-P-N hi-speed
MIL-S-19500/538	2N6676	300V/20A, N-P-N hi-speed
MIL-S-19500/538	2N6678	400V/20A, N-P-N hi-speed
MIL-S-19500/542A	2N6756	100V/14A, N-CH MOSFET
MIL-S-19500/542A	2N6758	200V/9A, N-CH MOSFET
MIL-S-19500/542A	2N6760	400V/5.5A, N-CH MOSFET
MIL-S-19500/542A	2N6762	500V/4.5A, N-CH MOSFET
MIL-S-19500/543A	2N6764	100V/38A, N-CH MOSFET
MIL-S-19500/543A	2N6766	200V/30A, N-CH MOSFET
MIL-S-19500/543A	2N6768	400V/14A, N-CH MOSFET
MIL-S-19500/543A	2N6770	500V/12A, N-CH MOSFET
MIL-S-19500/555	2N6788	100V/6A, N-CH MOSFET
MIL-S-19500/555	2N6790	200V/3.5A, N-CH MOSFET
MIL-S-19500/555	2N6792	400V/2A, N-CH MOSFET
MIL-S-19500/555	2N6794	500V/1.5A, N-CH MOSFET
MIL-S-19500/556	2N6782	100V/3.5A, N-CH MOSFET
MIL-S-19500/556	2N6784	200V/2.25A, N-CH MOSFET
MIL-S-19500/556	2N6786	200V/2.25A, N-CH MOSFET
MIL-S-19500/557	2N6796	100V/8A, N-CH MOSFET

Hi-Rel Product JAN Number Index

JAN No.	Device Type	Product Description
MIL-S-19500/557	2N6798	100V/5.5A, N-CH MOSFET
MIL-S-19500/557	2N6800	400V/3A, N-CH MOSFET
MIL-S-19500/557	2N6802	500V/2.5A, N-CH MOSFET
MIL-S-19500/563	2N6849	100V/6.5A, P-CH MOSFET
MIL-S-19500/563	2N6851	200V/4A, P-CH MOSFET
MIL-S-19500/564	2N6849	100V/2.5A, P-CH MOSFET
MIL-S-19500/564	2N6851	200V/4A, P-CH MOSFET
MIL-S-19500/565	2N6895	100V/1.5A, P-CH MOSFET
MIL-S-19500/565	2N6896	100V/6A, P-CH MOSFET
MIL-S-19500/565	2N6897	100V/12A, P-CH MOSFET
MIL-S-19500/565	2N6898	100V/25A, P-CH MOSFET
MIL-S-19500/566	2N6901	100V/1.5A, N-CH MOSFET
MIL-S-19500/566	2N6902	100V/-12A, N-CH MOSFET
MIL-S-19500/566	2N6903	200V/1.5A, N-CH MOSFET
MIL-S-19500/566	2N6904	200V/-8A, N-CH MOSFET
MIL-S-19500/569	2N6966	100V/15A N-CH MOSFET
MIL-S-19500/569	2N6967	200V/13A N-CH MOSFET
MIL-S-19500/569	2N6968	400V/7.5A N-CH MOSFET
MIL-S-19500/569	2N6969	500V/16A N-CH MOSFET

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